An adiabatic superconductor 8-bit adder with 24 $k_\mathrm{B}T$ energy dissipation per junction

Naoki Takeuchi[1,2,*], Taiki Yamae[3], Christopher L. Ayala[1], Hideo Suzuki[1], and Nobuyuki Yoshikawa[1,3]

[1]*Institute of Advanced Sciences, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan*

[2]*PRESTO, Japan Science and Technology Agency, 4-1-8 Honcho, Kawaguchi, Saitama 332-0012, Japan*

[3]*Department of Electrical and Computer Engineering, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan*

[*]takeuchi-naoki-kx@ynu.jp

Abstract: Adiabatic quantum-flux-parametron (AQFP) logic is an energy-efficient superconductor logic family. In this paper, we conducted high-frequency operation and energy measurement of an AQFP circuit with more than 1,000 Josephson junctions in the experiment. We designed an 8-bit carry look-ahead adder (CLA) using AQFP gates and fabricated it using an advanced fabrication technology, the AIST 10 kA/cm^2 Nb high-speed standard process (HSTP). The correct operation of the 8-bit CLA was demonstrated at a 1-GHz clock frequency for a critical carry propagation test vector. The energy dissipation of the 8-bit CLA was measured by observing the power of excitation current. Our results showed that the energy dissipation per operation of the 8-bit CLA can be estimated to be approximately 1.5 aJ, or 24 $k_\mathrm{B}T$ per junction, where k_B is the Boltzmann's constant and T is the operating temperature.

Superconductor logic families[1-4] can operate with low power consumption and high clock frequencies due to their physical advantages: zero dc resistance, flux quantization, and the Josephson effect. The switching energy (energy dissipation per switching operation) of superconductor logic is given by $\sim I_c\Phi_0$, where I_c is the critical current of Josephson junctions and Φ_0 is a flux quantum. Assuming a practical I_c of 150 μA, $I_c\Phi_0$ gives 0.31 aJ, which indicates the high energy efficiency of superconductor logic families. Therefore, numerous superconductor digital circuits have been designed and demonstrated for applications such as energy-efficient microprocessors[5-7], readout electronics for cryogenic detectors[8-10], and interface circuits for superconductor quantum bits[11-13]. The performance of these superconductor digital circuits has been continuously improved by the advancement of Nb integrated-circuit fabrication technologies[14,15].

Adiabatic quantum-flux-parametron (AQFP)[16] logic is an energy-efficient superconductor logic family based on the quantum-flux-parametron (QFP)[17,18]. AQFP logic achieves high energy efficiency by adopting adiabatic switching[19,20], in which the potential energy profile evolves from a single well to a double well so that the logic state can change quasi-statically. Also, AQFP logic maximizes the benefit of adiabatic switching by using Josephson junctions with a small characteristic time[21], so that the switching energy (energy dissipation per switching event) of an AQFP gate ranges from 10^{-20} J to 10^{-21} J at 5 GHz operation, which is one to two orders of magnitude smaller than that of the original QFP. We have established a design environment for AQFP logic, such as a cell library[22] and digital simulation models[23], to develop energy-efficient microprocessors using AQFP logic. Using the established design environment, we have designed and demonstrated several AQFP circuits such as adders[22,24] and register files[25], which are important components for microprocessor design. These AQFP circuits were mainly fabricated using the AIST 2.5 kA/cm^2 Nb standard process (STP2)[26] and were operated at low

2

clock frequencies (~100 kHz). Also, the energy dissipation of these AQFP circuits were estimated by numerical simulation, rather than experiments.

In this paper, we conduct the high-frequency operation and energy measurement of an AQFP circuit with more than 1,000 Josephson junctions in experiments. We design an 8-bit carry look-ahead adder (CLA) using AQFP gates and fabricate it using an advanced fabrication technology, the AIST 10 kA/cm^2 Nb high-speed standard process (HSTP)[27]. In the AQFP gates for HSTP, the damping resistors for the Josephson junctions are removed to reduce the circuit area and improve the energy efficiency whereas the previous design for STP2 used critically damped junctions. First, we demonstrate the 8-bit CLA at a low clock frequency (100 kHz) using several test vectors, including critical carry propagation tests. Then, we demonstrate the 8-bit CLA at a high clock frequency (1 GHz). Finally, we measure the energy dissipation of the 8-bit CLA by observing the power of excitation current. Our results show that the energy dissipation of the 8-bit CLA is only 1.5 aJ per operation, or $24k_{B}T$ per junction, where k_{B} is the Boltzmann's constant and T is the operating temperature.

Figure 1(a) shows a micrograph of the fabricated 8-bit CLA, which is a Kogge-Stone adder. The schematic design of the CLA follows the design reported in the literature[24], in which majority gates are utilized to reduce the junction count and logic stages. For the physical layout design, the AQFP cell library adopting a minimalist design[22] was used; the AQFP logic gates in the library were built by arraying a few types of building blocks, the physical layout of which were designed through the use of inductance extraction via InductEx[28]. As mentioned above, the Josephson junctions in the AQFP gates are not damped by resistors; thus, the quality factor of the junctions is much higher than 1 (~180), which reduces the energy dissipation of AQFP gates significantly[21]. To check the logic functions of the 8-bit CLA, digital simulation was carried out by using the hardware description language (HDL) models for AQFP logic[23]. The entire circuit is

3

powered and clocked by a pair of ac excitation currents with a phase separation of 90° (I_{x1} and I_{x2}), the frequency of which corresponds to the clock frequency. The dc offset current I_d applies dc fluxes to the AQFP gates so that the entire circuit is powered using only two ac current sources. Figure 1(b) illustrates the distribution of the excitation currents. I_{x1}, I_{x2}, and I_d go through the entire circuit, including peripheral circuits, and are terminated by off-chip 50-Ω terminators. The AQFP gates in the circuit are powered in the form of serial flux biasing, i.e., the excitation currents apply magnetic flux to the AQFP gates via magnetic coupling. ϕ_1 through ϕ_4 in Fig. 1(b) show the excitation phases, along which logic operations are performed with a phase separation of 90°. More details regarding excitation methods in AQFP logic can be found in the literature[27]. Voltage drivers[29] with stacked dc superconducting quantum interference devices (dc-SQUIDs), which amplify the logic signals of the AQFP gates to mV-range voltage signals, are included to achieve good signal-to-noise ratios (SNRs) in the experiment. The junction count of the entire circuit is 1,638: 1,062 for the CLA and 576 for the peripheral circuits such as the voltage drivers.

Figure 2 shows the simulation results of the energy dissipation per operation of the 8-bit CLA as a function of clock frequencies. The markers represent calculation results, and the line represents a fitting curve: af^b+c, where f is the clock frequency in GHz, $a = 1.49\times10^{-19}$, $b = 1.27$, and $c = 2.93\times10^{-19}$. The energy dissipation was calculated by the Josephson circuit simulator, JSIM[30]. Since the energy dissipation of an AQFP gate depends on the input vectors[31], the energy dissipation shown in Fig. 2 is the average over the ten test vectors[24] shown in Table I; test numbers 5 and 7 are the critical carry propagation test vectors, where the least significant bit (LSB) generates the carry-out. As the clock frequency lowers, the energy dissipation decreases owing to adiabatic switching and approaches a non-zero energy bound (~0.29 aJ); this is because the 8-bit CLA is designed using conventional irreversible logic gates such as majority gates, so that the thermodynamic irreversibility of the circuit imposes an energy bound[31]. The energy dissipation

4

per operation of the 8-bit CLA is 1.4 aJ at 5 GHz. For comparison, the energy dissipation per operation of the previously designed 8-bit CLA[22,24], which was designed using STP2, was 12 aJ at 5 GHz. The difference in energy dissipation is mainly attributed to the difference in the damping conditions of Josephson junctions[21]: the junctions in HSTP are underdamped to reduce energy dissipation whereas the junctions in STP2 are critically damped by resistors.

First, we tested the fabricated 8-bit CLA at a low clock frequency (100 kHz). Figure 3 shows measurement waveforms at 4.2 K in liquid helium, where the input vectors shown in Table I are used. I_{b0} is the signal current applied to the LSB of input B; all the signal currents to inputs A and B were generated by a multi-channel digital pattern generator (Tektronix, DG2020A). V_{s0} through V_{s7} are the output voltages representing the sum from the least significant bit to the most significant bit, respectively. V_{cout} is the output voltage representing the carry-out. The figure shows the correct logic operations for all the input vectors (see Table I). The measured operating margins with regard to the excitation currents were 8.4 dB and 8.1 dB for I_{x1} and I_{x2}, respectively.

Then, we tested the 8-bit CLA at a high clock frequency (1 GHz). Due to the limitation in the experimental setup (e.g., we did not have a high-frequency multi-channel digital pattern generator or many high-frequency low-noise amplifiers), we used only the critical carry propagation test vector, and only the carry-out was observed. Dc signal currents were applied to inputs A and B, except for the LSB of input B, such that input A [7:0] was fixed to "11111111" and input B [7:1] was fixed to "0000000." A pseudorandom binary sequence (PRBS) was applied to the LSB of input B by a high-frequency digital pattern generator (Agilent, N4906B). In this input vector, the carry-out should be the same as the LSB of input B (see test number 5 in Table I); thus, we can test the critical carry propagation by comparing the LSB of input B and the carry-out. Figure 4 shows the measurement waveforms at 4.2 K in liquid helium. I_{b0} is the signal current applied to the LSB of input B, and V_{cout} is the output voltage representing the carry-out. The figure

5

shows the correct logic operation because the sequence of V_{cout} is equal to that of I_{b0}. Unfortunately, V_{cout} was not stable (i.e., error rates were high) beyond 1 GHz; at this moment, it is not clear if the unstable operation is attributed to the voltage drivers or the CLA, which will be investigated in future work.

Finally, we measured the energy dissipation of the 8-bit CLA at 4.2 K in liquid helium by observing the power of the excitation currents. In the experiment, I_{x1} and I_{x2} go through the AQFP chip in liquid Helium and are terminated by off-chip 50-Ω terminators located in a room temperature stage. The AQFP gates on the chip are powered by I_{x1} and I_{x2} via magnetic coupling; thus, I_{x1} and I_{x2} do not touch the ground plane of the chip. The power of I_{x1} and I_{x2} at the off-chip terminators depends on the operation of the 8-bit CLA on the chip: the terminated power decreases when the 8-bit CLA works because some of the power of I_{x1} and I_{x2} is dissipated by the AQFP gates in the CLA. Therefore, the power dissipation of the 8-bit CLA can be measured by the change in the terminated power of I_{x1} and I_{x2} when the CLA works. Figure 5(a) and (b) show the measurement results of the power of I_{x1} and I_{x2} at the off-chip terminators at 5 GHz, which were measured by a spectrum analyzer (Anritsu, MS2830A). In this power measurement, inputs A and B were fixed to "11111111" and "00000001," respectively. The red markers represent the power when the 8-bit CLA is working. On the other hand, the blue makers represent the power when the 8-bit CLA is not working, where I_d is not applied so that the AQFP gates in the CLA do not perform switching operations. The differences between the red and blue markers show the power dissipated by the entire AQFP circuit, including peripheral circuits, on the chip. The reason why power dissipation is different between I_{x1} and I_{x2} is because the number of the AQFP gates coupled to I_{x1} is different from that coupled to I_{x2}. The measured power dissipation of the entire circuit P_{meas} is 97 nW, which agrees well with the simulated power dissipation of 95 nW. According to numerical simulation, the power dissipation of the 8-bit CLA is 7.7% of that of the entire circuit;

thus, a P_{meas} of 97 nW indicates that the power dissipation of the 8-bit CLA is 7.5 nW. Therefore, the energy dissipation per operation of the 8-bit CLA is 1.5 aJ, i.e., the average switching energy dissipation per junction is only 1.4 zJ, or 24 $k_B T$, which is much smaller than the switching energy of conventional superconductor logic (~300 zJ).

We conducted the above power measurement at 5 GHz (rather than 1 GHz, where we confirmed correct operations) to ensure large changes in I_{x1} and I_{x2}; otherwise, the accuracy of the power measurement is more difficult to validate as the switching energy at 1 GHz is too small. Although the error rates of the 8-bit CLA were high at frequencies beyond 1 GHz, all the AQFP gates in the 8-bit CLA were expected to be performing switching operations during power measurement because the excitation currents supply magnetic flux equally to all the gates owing to serial flux biasing. Also, the data dependence of the energy dissipation of the 8-bit CLA is not large; numerical simulation showed that at 5 GHz the minimum, maximum, and average of the energy dissipation per operation between the ten test vectors shown in Table I are 1.31×10^{-18} J, 1.47×10^{-18} J, and 1.44×10^{-18} J, respectively. Therefore, we assumed that errors do not affect significantly the power measurement, and that the power measurement at 5 GHz was carried out with sufficient accuracy.

In conclusion, we conducted high-frequency operation and energy measurement of an 8-bit CLA that was designed using AQFP gates and fabricated by HSTP. The correct operation of the 8-bit CLA was demonstrated at 1 GHz for the critical carry propagation test vector. The energy measurement showed that the energy dissipation per operation of the 8-bit CLA can be estimated to be approximately 1.5 aJ, which corresponds to 24 $k_B T$ per junction. Our measurement results indicate the high energy efficiency of AQFP logic.

Acknowledgements

References

1. K.K. Likharev and V.K. Semenov, IEEE Trans. Appl. Supercond. **1**, 3 (1991).

2. O.A. Mukhanov, IEEE Trans. Appl. Supercond. **21**, 760 (2011).

3. Q.P. Herr, A.Y. Herr, O.T. Oberg, and A.G. Ioannidis, J. Appl. Phys. **109**, 103903 (2011).

4. M. Tanaka, M. Ito, A. Kitayama, T. Kouketsu, and A. Fujimaki, Jpn. J. Appl. Phys. **51**, 053102 (2012).

5. M. Tanaka, A. Kitayama, M. Okada, T. Kouketsu, T. Takinami, M. Ito, and A. Fujimaki, IEICE Trans. Electron. **E97.C**, 166 (2014).

6. A.Y. Herr, Q.P. Herr, O.T. Oberg, O. Naaman, J.X. Przybysz, P. Borodulin, and S.B. Shauck, J. Appl. Phys. **113**, 033911 (2013).

7. A.F. Kirichenko, I. V. Vernik, J.A. Vivalda, R.T. Hunt, and D.T. Yohannes, IEEE Trans. Appl. Supercond. **25**, 1300505 (2015).

8. S. Miki, H. Terai, T. Yamashita, K. Makise, M. Fujiwara, M. Sasaki, and Z. Wang, Appl. Phys. Lett. **99**, 111108 (2011).

9. K. Sano, Y. Takahashi, Y. Yamanashi, N. Yoshikawa, N. Zen, and M. Ohkubo, Supercond. Sci. Technol. **28**, 074003 (2015).

10. N. Takeuchi, T. Yamashita, S. Miyajima, S. Miki, N. Yoshikawa, and H. Terai, Opt. Express **25**, 32650 (2017).

11. M.W. Johnson, P. Bunyk, F. Maibaum, E. Tolkacheva, a J. Berkley, E.M. Chapple, R. Harris, J. Johansson, T. Lanting, I. Perminov, E. Ladizinsky, T. Oh, and G. Rose, Supercond. Sci. Technol. **23**, 065004 (2010).

12. N. Takeuchi, D. Ozawa, Y. Yamanashi, and N. Yoshikawa, Phys. C Supercond. Its Appl. **470**, 1550 (2010).

13. R. McDermott and M.G. Vavilov, Phys. Rev. Appl. **2**, 014007 (2014).

14. S. Nagasawa, K. Hinode, T. Satoh, M. Hidaka, H. Akaike, A. Fujimaki, N. Yoshikawa, K.

Takagi, and N. Takagi, IEICE Trans. Electron. **E97.C**, 132 (2014).

15. S. Tolpygo, V. Bolkhovsky, T. Weir, A. Wynn, D. Oates, L. Johnson, and M. Gouker, IEEE Trans. Appl. Supercond. **26**, 1100110 (2016).

16. N. Takeuchi, D. Ozawa, Y. Yamanashi, and N. Yoshikawa, Supercond. Sci. Technol. **26**, 035010 (2013).

17. K. Loe and E. Goto, IEEE Trans. Magn. **21**, 884 (1985).

18. M. Hosoya, W. Hioe, J. Casas, R. Kamikawai, Y. Harada, Y. Wada, H. Nakane, R. Suda, and E. Goto, IEEE Trans. Appl. Supercond. **1**, 77 (1991).

19. K. Likharev, IEEE Trans. Magn. **13**, 242 (1977).

20. J.G. Koller and W.C. Athas, in *Work. Phys. Comput.* (IEEE, 1992), pp. 267–270.

21. N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, Phys. Rev. Appl. **4**, 034007 (2015).

22. N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, J. Appl. Phys. **117**, 173912 (2015).

23. Q. Xu, C.L. Ayala, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, IEEE Trans. Appl. Supercond. **26**, 1301805 (2016).

24. C.L. Ayala, N. Takeuchi, Y. Yamanashi, T. Ortlepp, and N. Yoshikawa, IEEE Trans. Appl. Supercond. **27**, 1300407 (2017).

25. N. Tsuji, Y. Yamanashi, N. Takeuchi, C. Ayala, and N. Yoshikawa, in *2017 16th Int. Supercond. Electron. Conf.* (IEEE, 2017).

26. S. Nagasawa, Y. Hashimoto, H. Numata, and S. Tahara, IEEE Trans. Appl. Supercond. **5**, 2447 (1995).

27. N. Takeuchi, S. Nagasawa, F. China, T. Ando, M. Hidaka, Y. Yamanashi, and N. Yoshikawa, Supercond. Sci. Technol. **30**, 035002 (2017).

28. C.J. Fourie, IEEE Trans. Appl. Supercond. **25**, 1 (2015).

29. N. Takeuchi, H. Suzuki, and N. Yoshikawa, Appl. Phys. Lett. **110**, 202601 (2017).

30. E. Fang and T. Van Duzer, in *1989 Int. Supercond. Electron. Conf. (ISEC '89)* (Tokyo, 1989), pp. 407–410.

31. N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, Sci. Rep. **7**, 75 (2017).
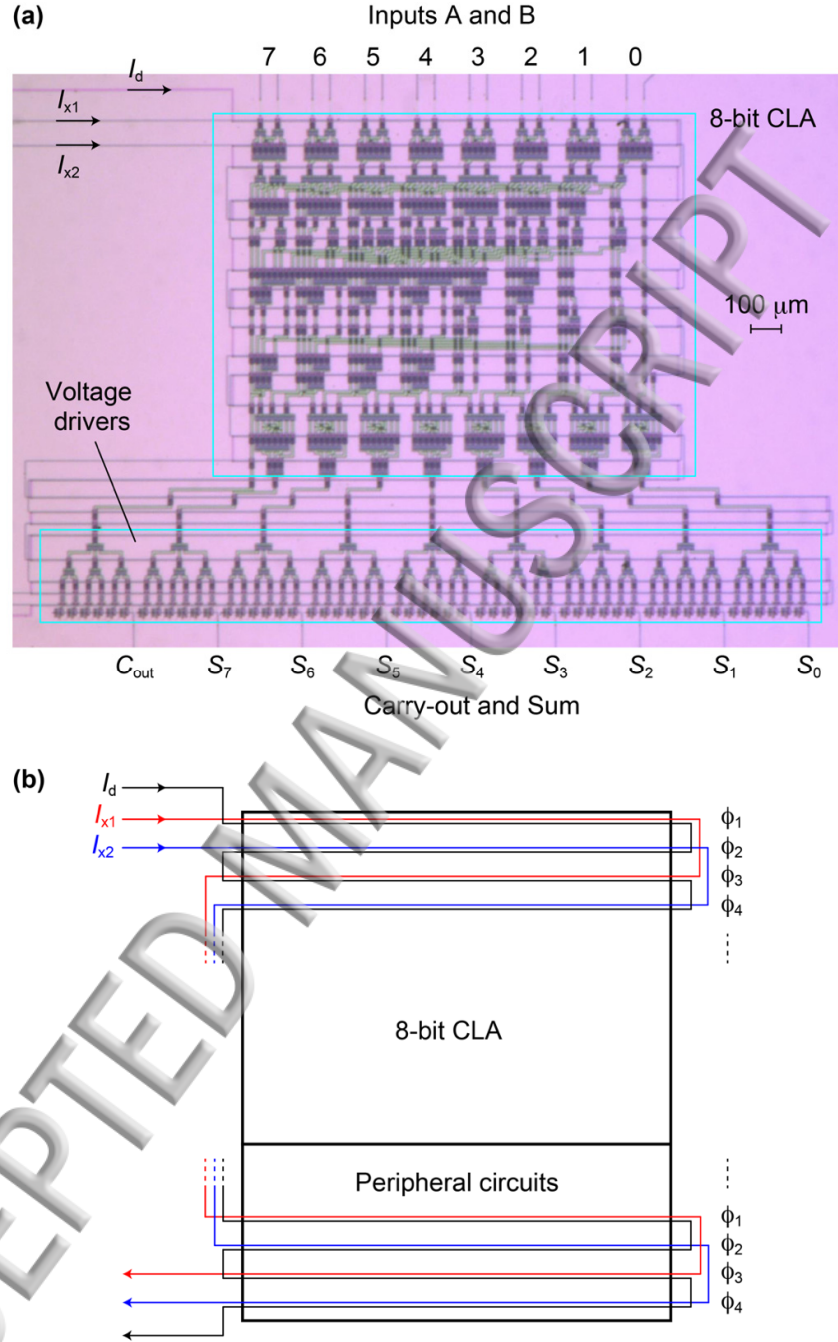
Fig. 1   8-bit CLA that was designed using AQFP gates and fabricated by HSTP. (a) Micrograph. The junction count

of the entire circuit is 1,638: 1,062 for the CLA and 576 for the peripheral circuits such as the voltage drivers. (b)
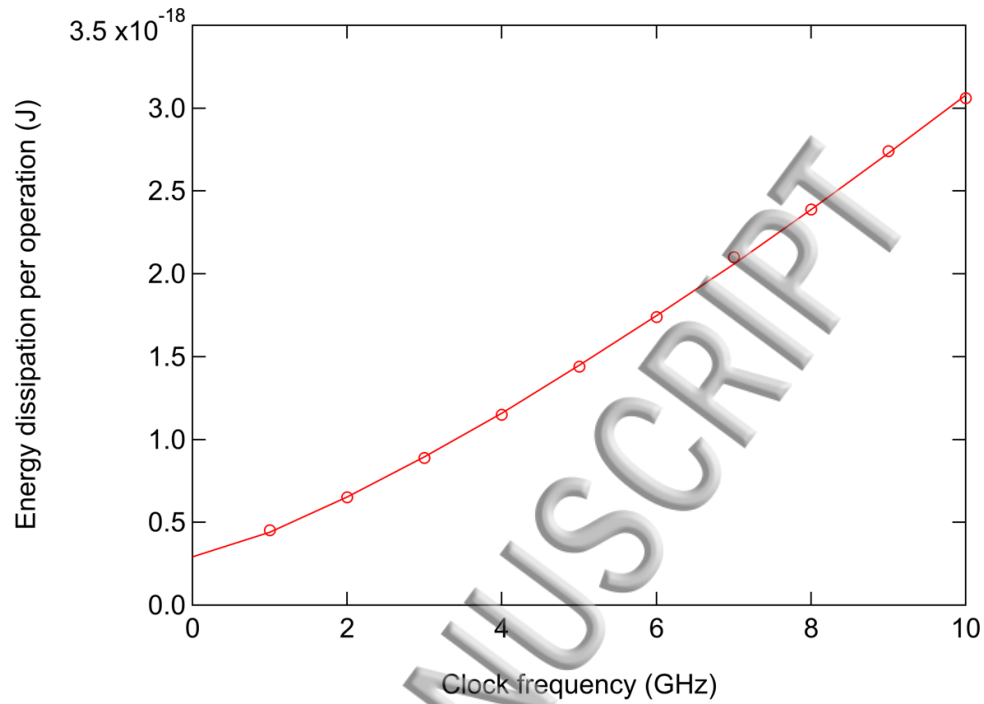
Excitation current distribution.

Fig. 2   Simulation of the energy dissipation per operation. The values of the energy dissipation are the averages over

the ten input vectors shown in Table I. The energy dissipation is 1.4 aJ at 5 GHz.

Table I   Input vectors and expected outputs.

| Test number	Input A [7:0]	Input B [7:0]	Carry-out and Sum [7:0]
1	00000000	11111111	011111111
2	11111111	00000000	011111111
3	11110000	00001111	011111111
4	00001111	11110000	011111111
5	11111111	00000001	100000000
6	01100111	10011001	100000010
7	00000001	11111111	100000000
8	01011001	10111100	100010101
9	11111111	11111111	111111110
10	01111001	11010100	101001101
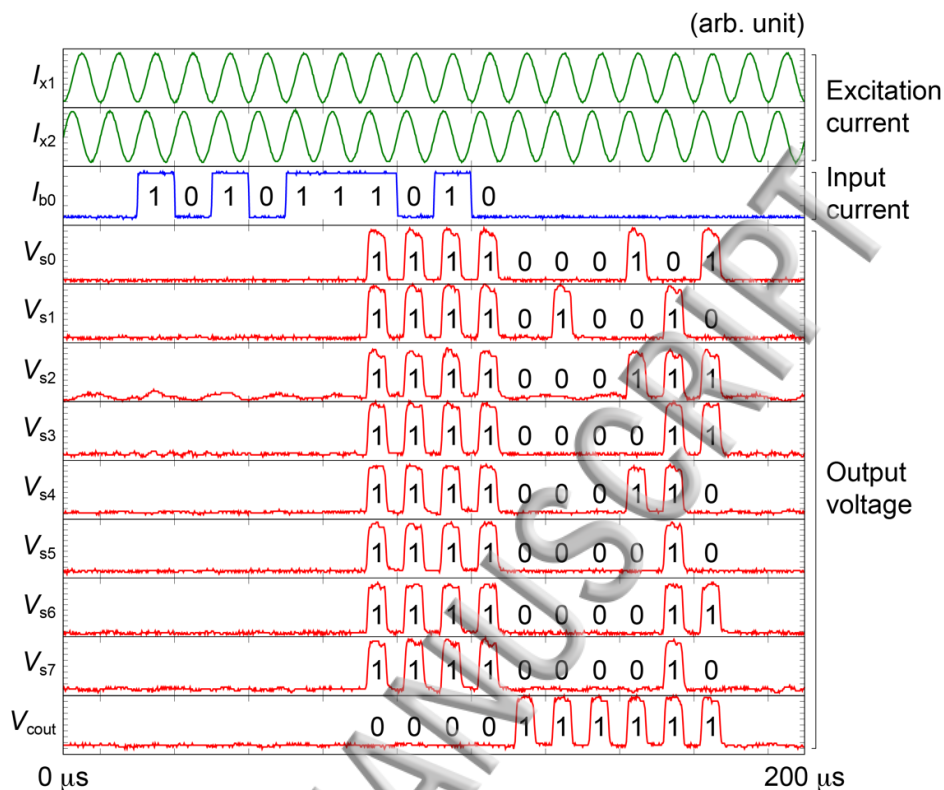
Fig. 3   Low-frequency demonstration at 100 kHz. The figure shows the correct operations for all the test vectors shown
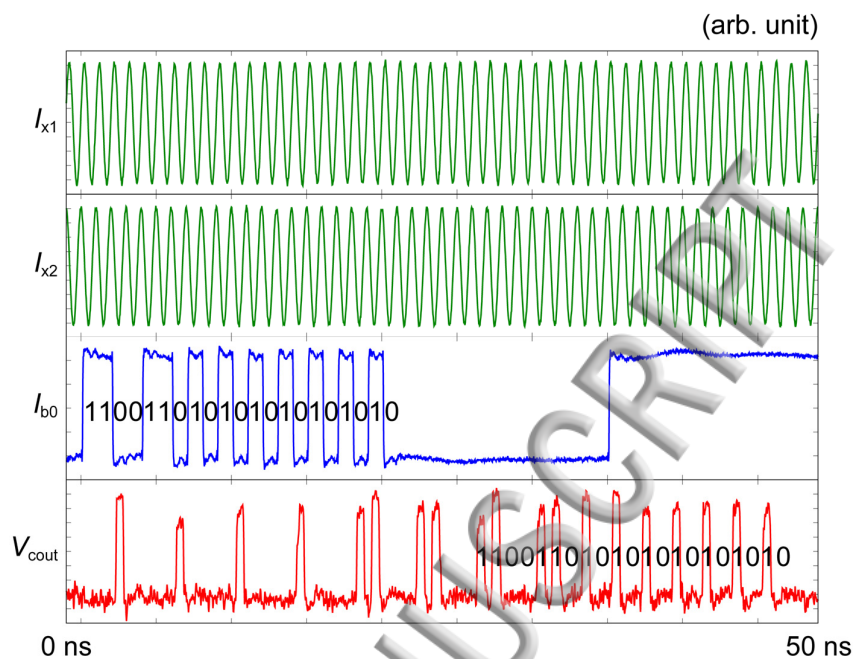
in Table I.

13

Fig. 4   High-frequency demonstration at 1 GHz. The figure shows the correct operation for the critical carry propagation test because the carry-out (V_{cout}) corresponds to the LSB of input B (I_{b0}).
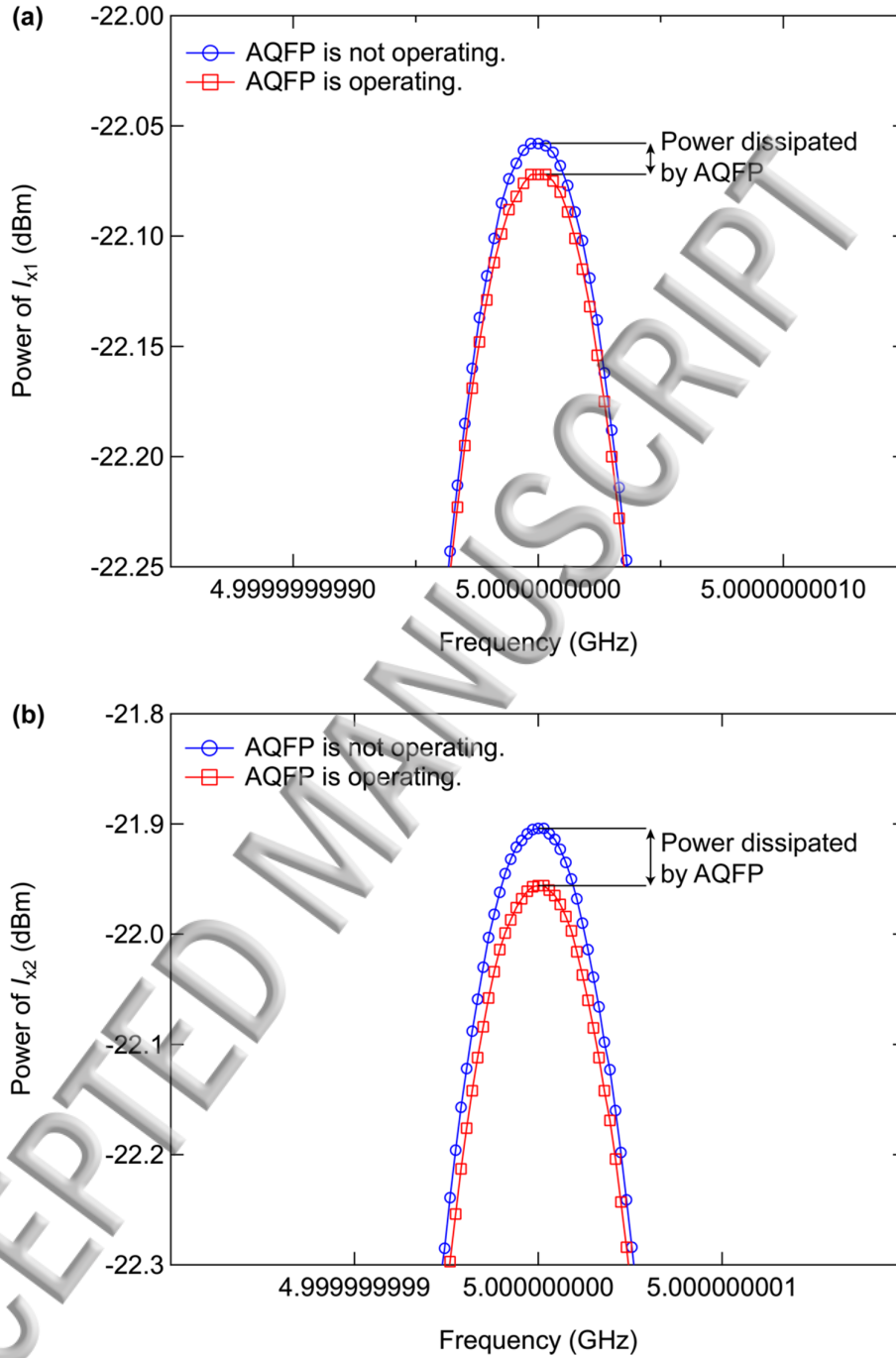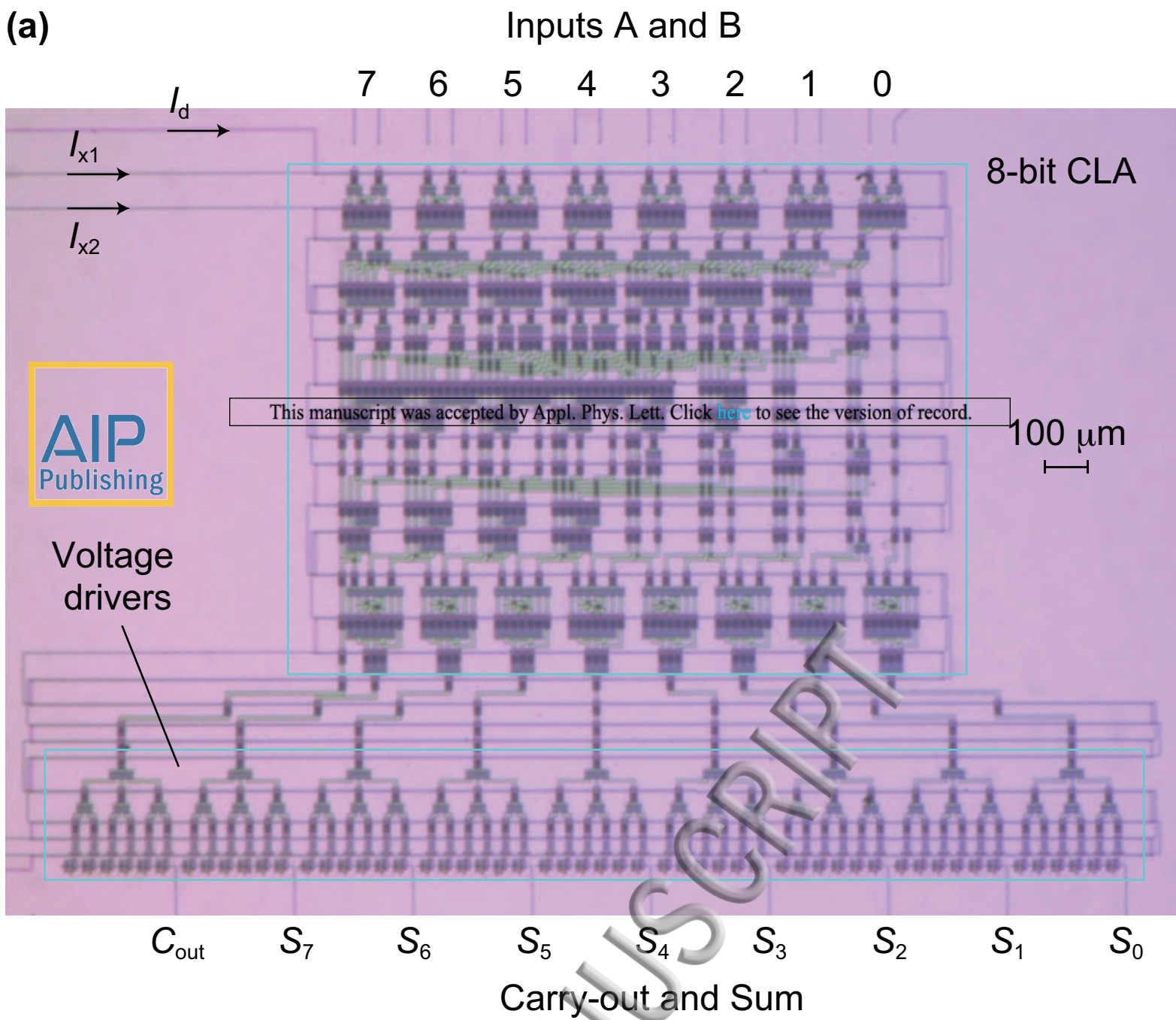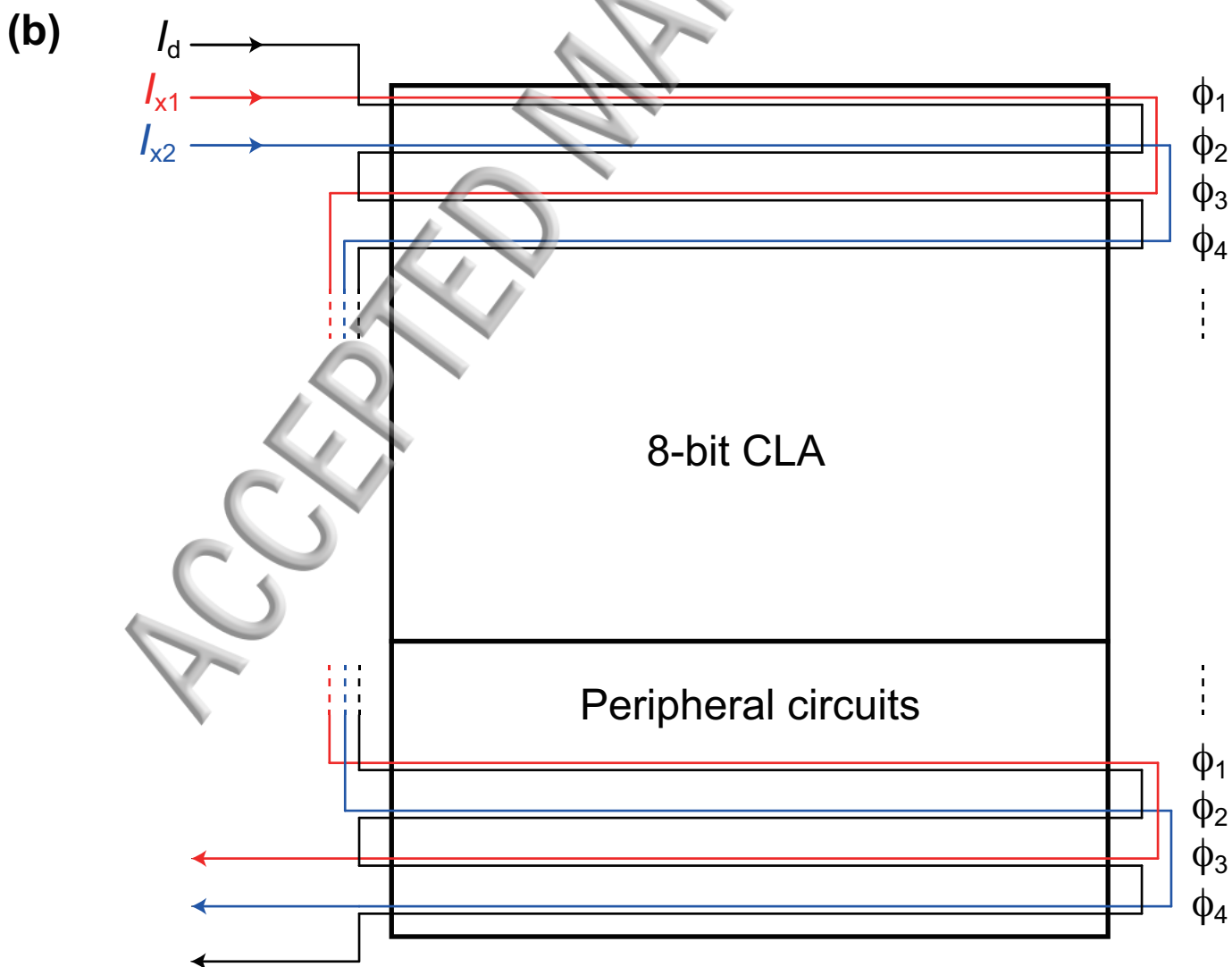
14

(a)

(b)

Fig. 5   Power measurement of (a) I_{x1} and (b) I_{x2} at 5 GHz. The red markers show the terminated power when the AQFP

circuit is operating whereas the blue markers show the terminated power when the AQFP circuit is not operating. The

differences between the red and blue markers show the power dissipated by the entire AQFP circuit on the chip.

15

(a)

Inputs A and B

7   6   5   4   3   2   1   0

I_d

I_{x1}

I_{x2}

8-bit CLA

100 µm

Voltage drivers

C_{out} S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0

Carry-out and Sum

(b)

I_d

I_{x1}

I_{x2}

ϕ_1
ϕ_2
ϕ_3
ϕ_4

8-bit CLA

Peripheral circuits

ϕ_1
ϕ_2
ϕ_3
ϕ_4

Energy dissipation per operation (J) vs **Clock frequency (GHz)**

y-axis: Energy dissipation per operation (J), scale 3.5×10^{-18}, marked 0.0, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5

x-axis: Clock frequency (GHz), marked 0, 2, 4, 6, 8, 10

(arb. unit)

I_{x1}

I_{x2}

I_{b0}

1100110101010101010101010

V_{cout}

1100110101010101010101010

0 ns   50 ns

(a)

Power of I_{x1} (dBm)

Legend:
- AQFP is not operating.
- AQFP is operating.

Power dissipated by AQFP

Frequency (GHz)

(b)

Power of I_{x2} (dBm)

Legend:
- AQFP is not operating.
- AQFP is operating.

Power dissipated by AQFP

Frequency (GHz)