Dead Time Compensation for Three-level Flying Capacitor Inverter with Phase Shift PWM

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***Abstract*—Multilevel inverter can obtain low distortion output voltage and current wave. However, dead time causes an output voltage error in the phase of inverter. Dead time error causes nonlinearity of output voltage and phase currents ripples with 5th and 7th order ripples of fundamental frequency. Current ripple decreases motor control performance. This paper presents dead time compensation for three-level flying capacitor inverter which is operated by phase shift pulse width modulation. This method is focused on the fact that power switching devices, which cause voltage error by dead time, depend on current polarities. The algorithm is simple, and the dead time is inserted at the instant of turning-on and turning-off of switching devices so as not to affect output voltage. The simulation result shows that high order harmonics which caused by dead time effect are eliminated using this method.**

***Index Terms*—Dead time compensation, Three-level inverter, Phase Shift PWM**

I. Introduction

Dead time is a switching delay of turning-on of a switching device until another device in the same leg is fully turning-off, which is used to prevent short circuit. In generally, dead time is inserted in pulse width modulation (PWM) signal. However, the dead time causes an output voltage error in the phase of inverter, which depends on output phase current polarity. Dead time error causes nonlinearity of output voltage and phase current ripples with 5th and 7th order ripples of fundamental frequency. This current ripple causes the motor torque ripple. During dead time period, power switching devices in the same leg are turning-off. Then output voltage is out of control, and the output phase voltage is affected by its phase currents. Subsequently, motor torque is also out of control and deviates from commanded value. These issues decrease motor control performance. Hence, dead time compensation is needed to realize high performance for a motor drive system.

Many reports have focused on dead time analysis and proposed compensation method for two level inverter. As reported previously [1]–[5], dead time effect can be eliminated by pulse based compensation. PWM signal is adjusted based on current polarity, and current detection as a resuly is important. In particular, accurate current measurement around zero crossing is required for high accuracy compensation. As reported in references [6] [7], dead time voltage error is considered as disturbance one, which and it is eliminated by taking a compensation on the command voltage to offset disturbance voltage which is caused by dead time. Hoffman et al. adopted current based dead time compensation using Kalman filter for space vector PWM [8].

Multilevel inverter can obtain low distortion output voltage and current wave by output changing multi stage. Therefore, motor control for high performance using multilevel inverter has been widely reported [9]–[11]. Low distortion output waveform using multi-level inverter has been confirmed to contribute to the reduction in motor torque ripple. However, dead time effect appears in a multi-level invertet as long as PWM performs the inverter. Dead time compensation for multi level inverter are proposed as same as two-level inverter. The current based pulse width compensation is reported previously [12]–[14]. Another report performed the change in the giving pattern of dead time and elimination of voltage error by dead time is elminated [15]. The value of dead time is adjusted online by the value of corresponding output current [16], [17]. The deviations of voltage vectors caused by dead time are directly compensated to three phase reference voltages. Usage of disturbance observer as torque ripple suppresser caused by dead time was also reprted [18].

In this paper, a PWM method without the voltage error by dead time [15] was applied for three-level adopted phase shift PWM. Here, dead time was inserted in PWM signal of switching devices which are determined by polarities of output phase currents. Subsequently voltage error of dead time was eliminated essentially. Simulation results indicated that this method improved the output waveform.

II. Three level Flying Capacitor Inverter

TABLE I
OPERATING MODE OF THREE LEVEL FLYING CAPACITOR INVERTER

	S_1	S_2	S_3	S_4	$i_o > 0$	$i_o < 0$
Mode1	ON	ON	OFF	OFF	V_{DC}	V_{DC}
Mode2	ON	OFF	ON	OFF	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$
Mode3	OFF	ON	OFF	ON	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$
Mode4	OFF	OFF	ON	ON	0	0

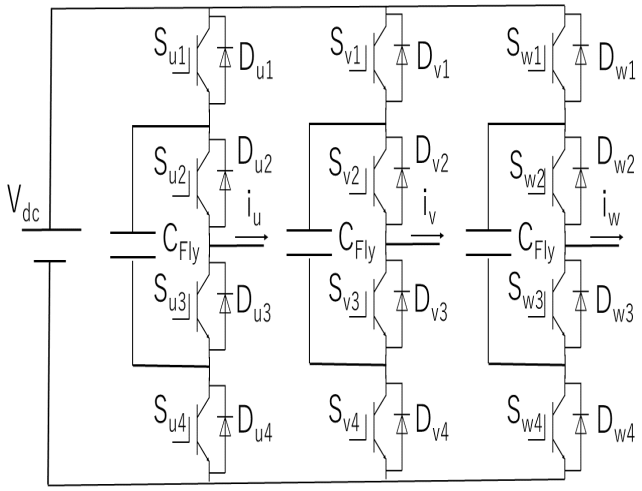

Fig. 1. Toopology of Three level Flying Capacitor Inverter

Fig.1 shows one phase of three-level Flying Capacitor type voltage source inverter topology. Four power switching devices are connected in series to form one leg of the inverter. In this topology, floating capacitor C_{Fly} is connected between the series power switching devices. The capacitor is charged to half of DC-link voltage of this inverter. Changing power switching devices states, DC-link voltage and the capacitor connected in different ways. And, line-to-ground output voltage can produce three-level output.

The mode of three-level flying capacitor inverter is shown in Table I. The top and bottom switches as well as the two middle ones are complimentary. When S_{u1} and S_{u2} are turning-on and other switches are turning-off, output voltage becomes V_{DC}. When S_{u3} and S_{u4} are tuning on and other switches are turning-off, output voltage becomes 0. In addition, when S_{u1} and S_{u3} are tuning on and other switches are turning-off, or S_{u2} and S_{u4} are tuning on and other switches are turning-off, output voltage becomes $\frac{V_{DC}}{2}$. In mode 2 and mode 3, the output current pass the capacitor. Therefore, the capacitor is charged or discharged according to the output current polarity. If the current has positive polarity, mode2 is that the capacitor is charged and mode3 is that the capacitor is discharged. If the current has negative polarity, mode 2 is that the capacitor is discharged and mode3 is that the capacitor is charged. In order to obtain three-level output, the voltage of capacitor must be maintained at $\frac{V_{DC}}{2}$ in this process.

PWM and capacitor voltage balancing are performed using phase-shift PWM method (PSMWM). In three-level inverter,two carrier waves which have phase difference by 180 degrees were used. PWM signal of S_{u1} and S_{u4} ,or S_{u2} and S_{u3} is generated independently by each carrier wave. Using PSPWM, the period of capacitor charging and the one of capacitor discharging appear the same rate in one carrier cycle. Hence, if switching frequency is high enough, the capacity voltage is balanced without additional circuit or control method.

III. Dead Time Effect of Three leve Fling Capacitor Inverter

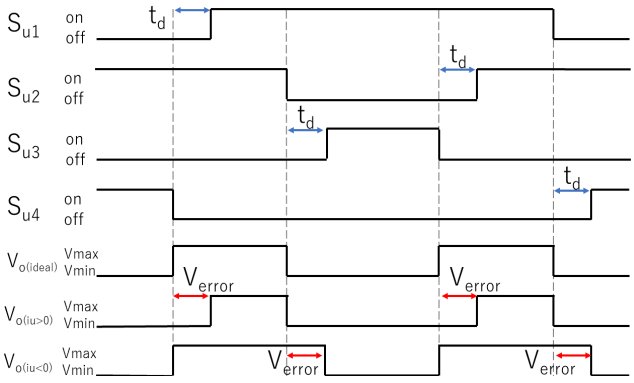

Fig. 2. PWM gate signals and dead tiem error

Dead time effect can be explained using one leg of the inverter shown in Fig.1. The dead time is used to prevent a short circuit in DC-link, and dead time T_d is inserted to PWM signals. As dead time presents, output phase voltages are not controlled by power switching devices which are in dead time period. During dead time, output phase voltages are determined by polarities of output phase currents. The current is continuous because of inductive load.

Fig.2 shows PWM gate signals and dead time error. If the load current has positive polarity (current flowing toward the load), voltage error is caused by dead time of S_{u1} or S_{u2}. Flywheel diode of D_{u3} or D_{u4} conducts during dead time period of each complementary power switching devices S_{u1} or S_{u2}. Output voltage becomes $\frac{V_{DC}}{2}$. On the contary, if load current has negative pplarity(current flowing from load), voltage error is caused by dead time of S_{u3} or S_{u4}. Flywheel diode of D_{u1} and D_{u2} conducts during dead time period of S_{u3} or S_{u4}. Output voltage becomes $\frac{V_{DC}}{2}$. Here V_o^{max} and V_o^{min} defines the maximum and minimum values of output voltage [18]. When output current polarity is positive during dead time, output voltage becomes V_o^{min}. Subsquently, V_o^{max} and V_o^{min} in the three-level inverters are given as follows:

$$V_o^{max} = \begin{cases} V_{DC} & (0 \le v_{ref} \le 1) \\ \frac{V_{DC}}{2} & (-1 \le v_{ref} < 0) \end{cases} \quad (1)$$

$$V_o^{min} = \begin{cases} \frac{V_{DC}}{2} & (0 \le v_{ref} < 1) \\ 0 & (-1 \le v_{ref} < 0) \end{cases} \quad (2)$$

where V^{ref} is the reference wave of PSPWM and here this value range from 1 to 0. The error of output voltage is the same to voltage variation width by power devices switching. Here, The dead time voltage error of three-level inverter is given as follows:

$$V_{error} = |V_o^{max} - V_o^{min}| f_s T_d sgn(i_u) \quad (3)$$

$$= \frac{V_{DC}}{2} f_s T_d sgn(i_u) \quad (4)$$

where V_{dc} is DC link voltage , Td is dead time period, and f_s is carrier frequency , sgn(i_u) is sign function and given as (5).

$$sgn(i_u) = \begin{cases} 1 & (i_u > 0) \\ 0 & (i_u = 0) \\ -1 & (i_u < 0) \end{cases} \quad (5)$$

Eq.(4) shows that the voltage error and switching frequency are in proportion in three-level inverter.

IV. Dead Time Compensation

As shown in Fig. 2, switching devices which affect output voltage because of dead time is differed by current polarity. And switching of S_{u3} and S_{u4} does not affect output voltage as dead time voltage error when current has positive polarity. Similarly, output voltage is not affected by switching S_{u1} and S_{u2} when the current has negative polarity . Therefore, dead time is not inserted in PWM signal of switching devices which affect the output voltage, but is inserted in turning-on and turning-off in PWM signals for switching device without affecting output voltage.

Dead time compensation when current polarity has positive is shown in Fig.3(a). Dead time is not inserted in PWM signals for S_{u1} and S_{u2}, but is inserted in turning-on and turning-off of S_{u3} and S_{u4}. Dead time compensation when current has negative polarity is shown in Fig.3(b). Dead time is not inserted in PWM signals for S_{u3} and S_{u4}, but is inserted in turning-on and turning-off of S_{u1} and S_{u2}.

In Flying capacitor multilevel inverter which is performed by PSPWM, the flying capacitor charging time and discharging time are the same in carrier one cycle. Therefore the capacitor voltage is balancing without additional circuit or special control method. In the case of applying this method, time for charging and discharging the capacitor is reduced by the same amount. Therefore, period of charging and discharging the capacitor is equal in carrier one cycle, and the capacitor voltage is balancing.

V. Simulation

TABLE II
Simulation Parameters

DC link Voltage V_{DC}[V]	50
Modulation	Phase Shift PWM
Modulation rate	0.8
Flying Capacitor Capacitance C_{Fly} [μF]	66
Switching Frequency f_{sw} [kHz]	100
Dead Time T_d[μsec]	1
Output Frequency f_{sw} [Hz]	200
Load Resistancce R [Ω]	2
Load Inductance L [μF]	240

Simulations are carried out in PSIM. The simulation results are used to evaluate the dead time compensation method. The simulation parameters are shown in Table II. The switching devices act as ideal ones which are zero time for turning-on and turning-off.

Fig.4 and Fig.5 shows the waveform of output phase voltage and the flying capacitor voltage. In the case of applying the compensation method, the capacitor voltage was balancing around 25 V and the output voltage became three-level output. These results shows that the distortion of the output phase curret is removed using dead time compensation. And the capacitor voltage balancing function still remains.

The output current waveforms without and with compensation are shown in Fig.6, and Fig.7 shows their FFT diagrams. In the case of without compensation, the 5th and 7th order harmonics appeared in FFT diagram, which are caused by the dead time effect. And applying the compensation, the 5th and 7th order harmonics were eliminated. Here, the total harmonics distortion (THD) of the phase current without compensation became 4.07%, which was reduced to 0.43% for the one with compensation. The THD of the phase current with compensation is approximately equal to the one without dead time which is the ideal THD

Fig.8 shows the change in THD with respect to the frequency when white noise with amplitude of ± 250 mV is applied to the value acquired by the current sensor assuming the presence or absence of dead time compensation and the actual environment. It is confirmed that the THD of phase current with compensation is approximately equal to the one without dead time which is ideal THD. And dead time compensation is effective in a wide frequency band,and even in the presence of noise.

VI. Conclusion

This paper presents dead time compensation for three-level flying capacitor inverter which is performed by PSPWM. This method is focused on the fact that power switching devices, which cause voltage error by dead time, depend on current polarities. The algorithm is simple, and dead time is inserted at the instant of turning-on and turning-off of switching devices so as to avoid the effect on output voltage. The simulation result shows that the high order harmonics which is caused from the dead time effect are eliminated using this method.

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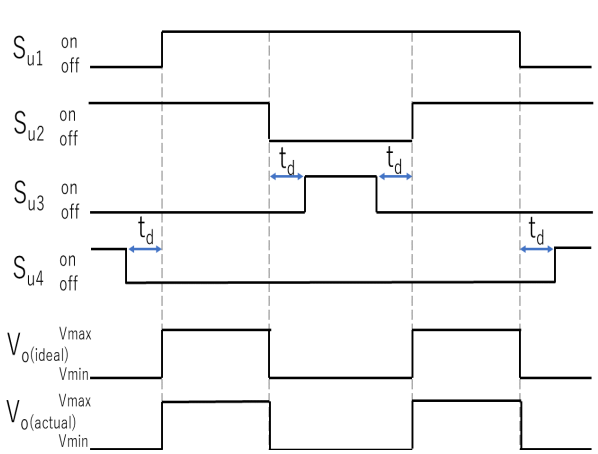
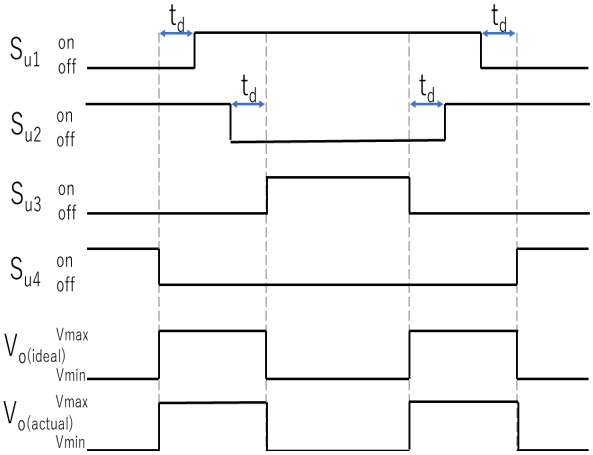


(a)Dead time compensation for positive polarity current



(b)Dead time compensation for negative polarity current

Fig. 3. Deadtime compensation

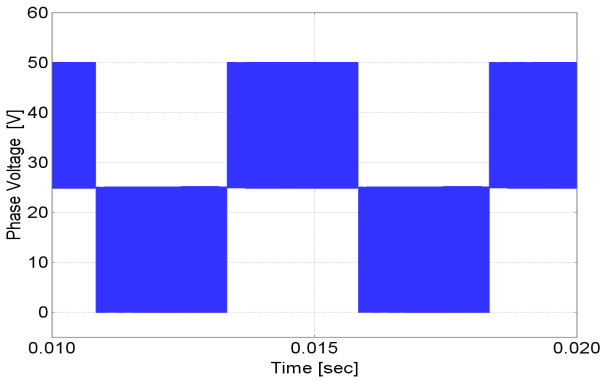


Fig. 4. Phase voltage

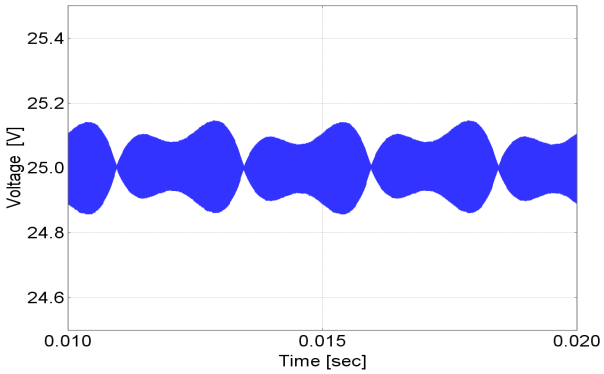
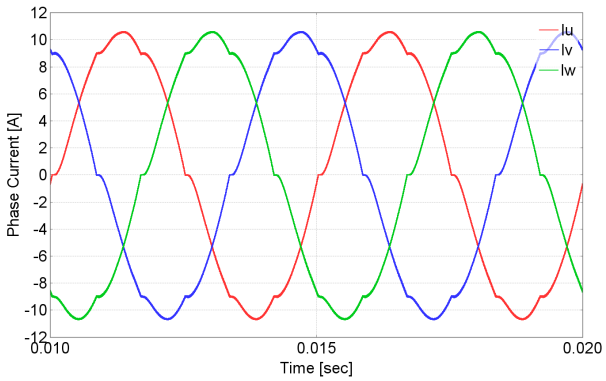
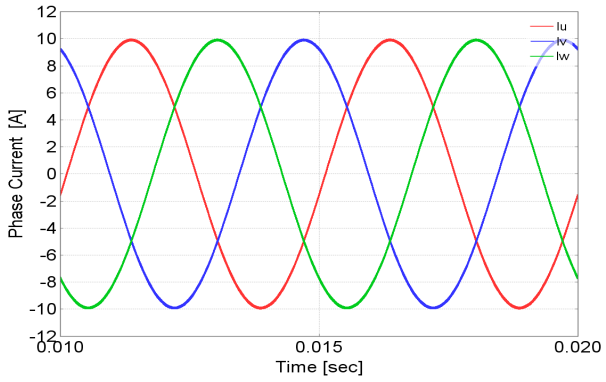


Fig. 5. Flying Capacitor Voltage



(a)without Compesation



(b)with Copmensation

Fig. 6. Phase currents

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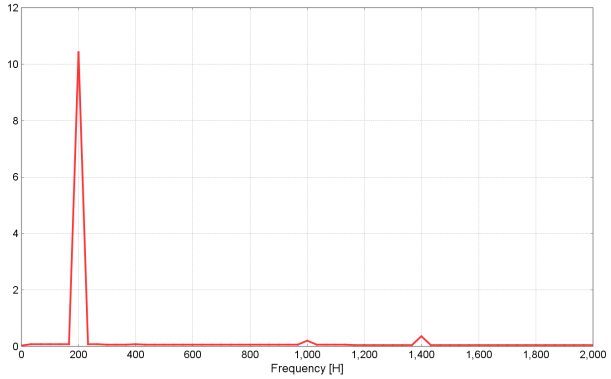
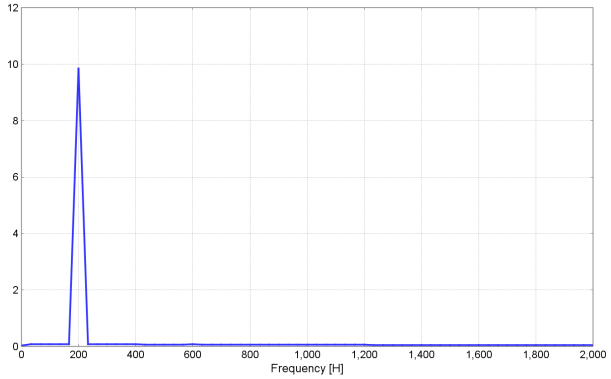


(a)without Compesation



(b)With Copmensation

Fig. 7. FFT diagram

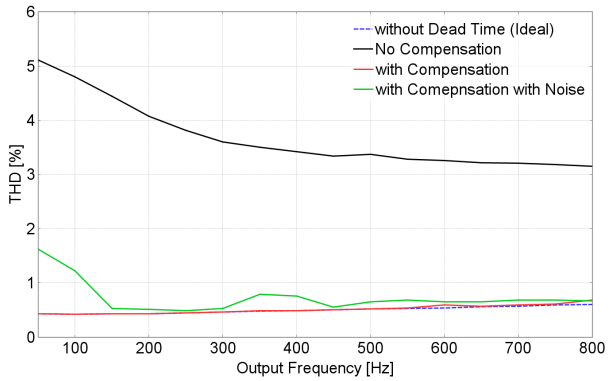


Fig. 8. THD of phase output current

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