IEICE TRANS. ELECTRON., VOL.E93–C, NO.4 APRIL 2010

PAPER Special Section on Frontiers of Superconductive Electronics

100 GHz Demonstrations Based on the Single-Flux-Quantum Cell Library for the 10 kA/cm^2 Nb Multi-Layer Process

Yuki YAMANASHI[†a)], ***Member***, **Toshiki KAINUMA**[†], ***Nonmember***, **Nobuyuki YOSHIKAWA**[†], ***Member***, **Irina KATAEVA**[††], ***Nonmember***, **Hiroyuki AKAIKE**[††], **Akira FUJIMAKI**[††], **Masamitsu TANAKA**[†††], **Naofumi TAKAGI**[†††], **Shuichi NAGASAWA**[††††], ***and*** **Mutsuo HIDAKA**[††††], ***Members***

SUMMARY A single flux quantum (SFQ) logic cell library has been developed for the 10 kA/cm^2 Nb multi-layer fabrication process to efficiently design large-scale SFQ digital circuits. In the new cell library, the critical current density of Josephson junctions is increased from 2.5 kA/cm^2 to 10 kA/cm^2 compared to our conventional cell library, and the McCumber-Stwart parameter of each Josephson junction is increased to 2 in order to increase the circuit operation speed. More than 300 cells have been designed, including fundamental logic cells and wiring cells for passive interconnects. We have measured all cells and confirmed they stably operate with wide operating margins. On-chip high-speed test of the toggle flip-flop (TFF) cell has been performed by measuring the input and output voltages. The TFF cell at the input frequency of up to 400 GHz was confirmed to operate correctly. Also, several fundamental digital circuits, a 4-bit concurrent-flow shift register and a bit-serial adder have been designed using the new cell library, and the correct operations of the circuits have been demonstrated at high clock frequencies of more than 100 GHz.

key words: *single flux quantum circuit, Josephson junction, cell library, adder*

1. Introduction

Single flux quantum (SFQ) circuits [1] are expected to play important roles in future high-end information processing systems because of their high-speed operation and ultra low power consumption. A cell-based design methodology and the digital circuit simulation [2] are very suitable for designing large-scale SFQ digital circuits. We have developed an SFQ logic cell library, called the CONNECT cell library [3], for the Superconductivity Research Laboratory (SRL) 2.5 kA/cm^2 Nb process [4]. We have demonstrated high-speed operations of several important digital circuits using the CONNECT cell library [5], [6]. The maximum operating frequency of the SFQ cross-bar switch was 50 GHz [6].

The operating speed of the SFQ circuit is proportional to the square root of critical current density (J_C) of Josephson junctions. Recently, the SRL has developed a new fabrication process that has the critical current density of 10 kA/cm^2 [7], [8].

In this study, we have developed a new cell library for the SRL 10 kA/cm^2 Nb multi-layer process and demonstrated the high-speed operations of fundamental circuits designed using the new cell library.

2. Cell Library for the 10 kA/cm^2 Nb Multi-Layer Process

The SRL 10 kA/cm^2 Nb multi-layer process has eight superconductive wiring layers including a ground plane. Though 10 superconductive layers were originally available in the SRL 10 kA/cm^2 Nb multi-layer process [8], we have adopted the 8-layer structure to shorten the fabrication process and to improve the circuit yield.

The lowest layer is used to supply the bias currents and is called the dc power layer (DCP). Middle four layers are used for passive transmission line (PTL) wiring [9]. The upper two layers are used for implementing active circuits containing Josephson junctions. Also, a thick ground plane prevents the active circuits from magnetic coupling to bias currents flowing in the DCP [10].

In the new cell library, the critical current density of Josephson junction is increased from 2.5 kA/cm^2 to 10 kA/cm^2 compared to our conventional process. Moreover, the McCumber-Stwart parameter (β_C) of Josephson junctions is increased to 2. Therefore, the operating speed of cells in the new cell library becomes higher than that of the conventional cells. Figure 1 shows the comparison of SFQ pulses in the new and conventional cells. The SFQ pulse in the new cell library becomes sharp and a higher speed operation can be expected.

In the SRL 10 kA/cm^2 Nb multi-layer process, the design rule is modified and we can use resistor layers underneath Josephson junctions as shunt resistors due to the process improvements. Because of decrease of the Josephson junction area decreasing and the design rule being modified, we could reduce the unit cell size to 30 μm × 30 μm, while it was 40 μm × 40 μm in the conventional cell library. Figure 2 shows the mask layout and an equivalent circuit of the Josephson transmission line (JTL) cell consisting of two Josephson junctions with the β_C of 2.

The standard value of supplied bias voltage is 2.5 mV. The bias currents are supplied to active circuits, which are implemented using upper two layers, from the DCP via ver-

Manuscript received July 31, 2009.
Manuscript revised October 22, 2009.

[†]The authors are with the Department of Electrical and Computer Engineering, Yokohama National University, Yokohama-shi, 240-8501, Japan.
[††]The authors are with the Department of Quantum Engineering, Nagoya University, Nagoya-shi, 464-8603 Japan.
[†††]The authors are with the Department of Information Science, Nagoya University, Nagoya-shi, 464-8603 Japan.
[††††]The authors are with Superconductivity Research Laboratory, International Superconductivity Technology Center, Tsukuba-shi, 305-8501 Japan.
a) E-mail: yamanasi@ynu.ac.jp
DOI: 10.1587/transele.E93.C.440

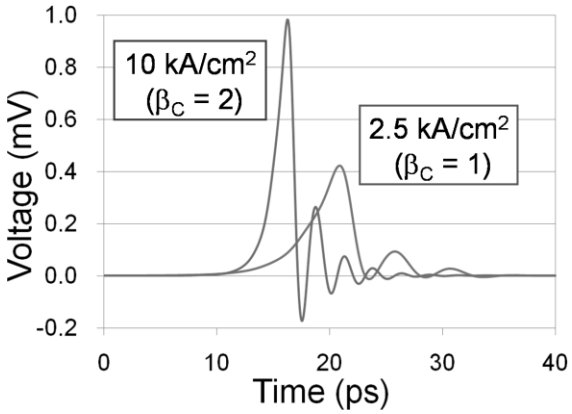


Fig. 1 Comparison of SFQ pulses of the 10 kA/cm^2 Nb advanced process and conventional 2.5 kA/cm^2 process.

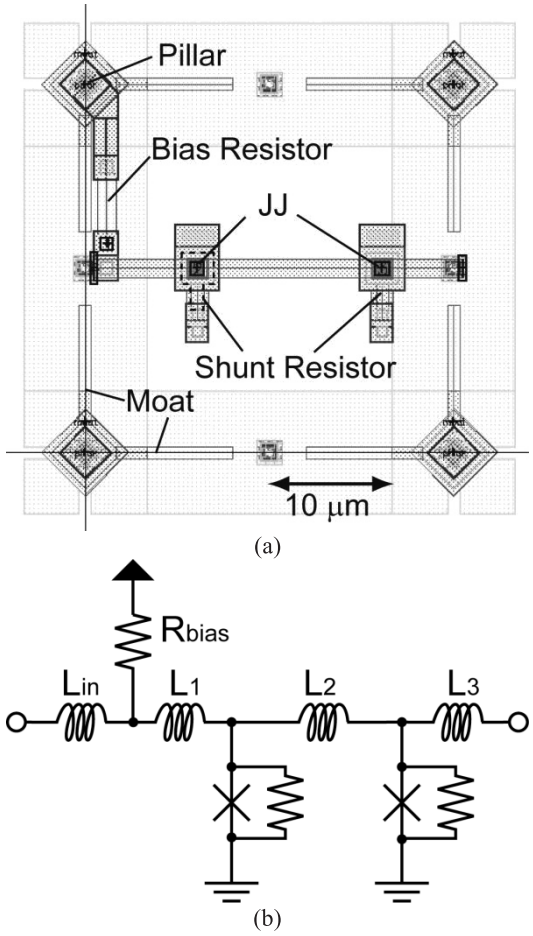


Fig. 2 The mask layout (a) and the equivalent circuit (b) of the JTL cell consisting of two Josephson junctions. The critical current of Josephson junctions is 216 μA. Josephson junctions are resistively shunted so that the β_C becomes 2. Shunt registers are 5.2 Ω. The pillar in the mask layout corresponds to vertically stacked contacts for bias supply. L_{in} = 0.29 pH, L_1 = 2.27 pH, L_2 = 4.53 pH, L_3 = 1.98 pH and R_{bias} = 8.35 Ω.

tically stacked contacts, called bias pillars. The bias pillars are located at the corners of each cell. The DCP lines are located at the periphery of each cell. Therefore the DCP lines

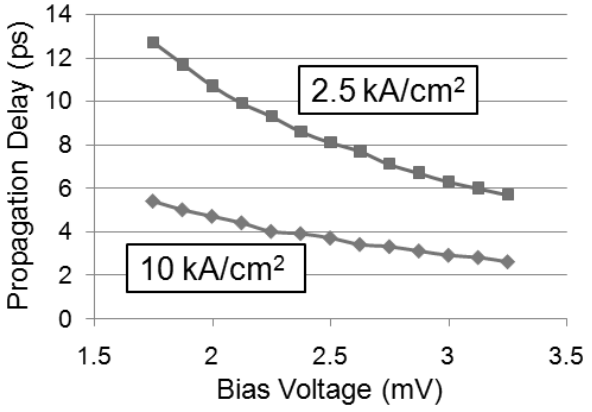


Fig. 3 Comparison of the simulated delay time of JTL cells of the conventional and new cell libraries.

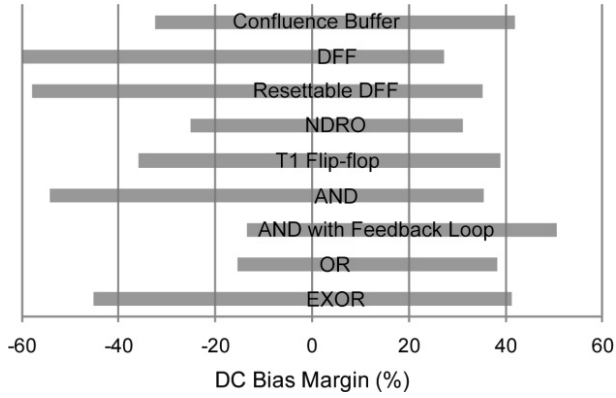


Fig. 4 Measured dc bias margins of fundamental logic cells of the new cell library. The dc bias margins are normalized by the designed bias voltage (2.5 mV). The DFF and NDRO mean a delay flip-flop cell and a non-destructive read out flip-flop cell respectively.

compose meshed lines in the circuit designed by using the new cell library. Every cell is surrounded by moats penetrating eight layers to avoid the effects of trapped flux on circuit operations. The effective moat structure for the multi-layer Nb process is adopted on the bases of experimental results obtained by Fujiwara et al. [11].

Figure 3 shows the dependences of simulated delay time of JTL cells consisting of two Josephson junctions of the new cell library and our previous cell library. As one can see, the delay time of the new JTL cell is more than two times faster than the previous one because of the high critical current density of Josephson junctions and the increase in β_C.

We have designed more than 300 cells, including fundamental logic cells and wiring cells for passive interconnects. The cells for passive interconnects are composed of strip lines and the PTLs can be overlapped with logic circuits because the logic circuits and PTLs are fabricated using different superconducting layers. Therefore, the wiring has become much more flexible [12].

We have measured dc bias margins of all cells at low speed. Figure 4 summarizes the measured dc bias margins

of fundamental logic cells. All logic cells have the widths of dc bias margins of more than 40%, and dc bias margins of wiring cells were more than 60%.These operating margins are as wide as margins of our conventional cell library [3].

3. High-Speed Test of Fundamental Circuits

We have also performed an on-chip high-speed test of a toggle flip-flop (TFF) cell by measuring input and output voltages [13]. Figure 5 shows high-speed test results of the TFF cell. In the correct operation region, the measured output voltage is exactly equal to twice the input voltage because the output frequency of the TFF is half the input signal frequency. From the measurement results, the maximum operating frequency of the TFF cells reaches 400 GHz. This maximum frequency agrees well with the circuit simulation assuming the critical current density of 10 kA/cm^2 and β_C of 2.

We have designed and tested several fundamental SFQ digital circuits, a 4-bit concurrent-flow shift register and a bit serial adder [14]. These circuits have been designed on the basis of a digital simulation by a hardware description language, Verilog-HDL. When we design digital circuits using the digital simulation, only the tables of timing parameters of cells, extracted by an analog simulation, were used to design the circuits. The used timing information was the propagation delay for every internal state of the cells, the setup time, and the hold time.

The 4-bit shift register was composed of JTL cells, splitter cells, and delay flip-flop (DFF) cells. Figure 6 shows the dependence of the measured dc bias margin on the clock frequency. The measured maximum operating frequency of the 4-bit concurrent-flow shift register was 120 GHz.

The bit serial adder was composed of two AND cells, two EXOR cells and various wiring cells. Figure 7 shows the microphotograph of the test circuit of the bit-serial adder. Several circuits were implemented to perform the on-chip high-speed test [15]. The number of Josephson junctions of the test circuits was 582. The Power consumption of the test circuits was 188 μW. Figure 8 shows the dependence of the measured dc bias margin of the bit-serial adder. The measured maximum operation frequency was 89 GHz. The dependence of measured dc bias margin agrees well with the simulated results. Moreover, the feedback loop of the carry signal restricts the maximum operation frequency in the simulation. The dependence of the measured dc bias margin indicated that the feedback loop restricted the operation frequency, which is in good agreement with simulated results. These results indicate that the simulated results using the digital simulation for the new cell library are very valid.

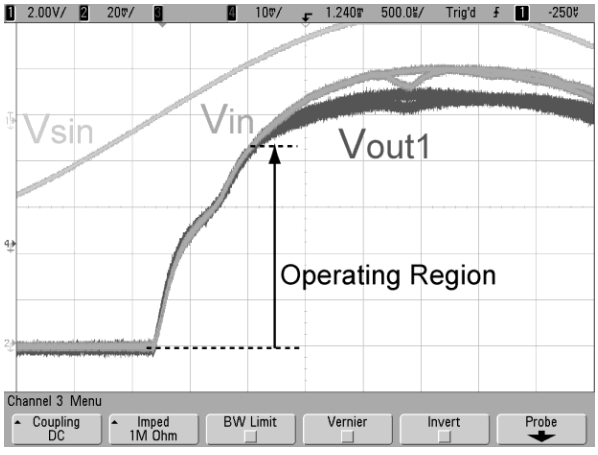


Fig. 5 High-speed test result of the toggle flip-flop (TFF) cell. Vsin corresponds to current supplied to Josephson junction located at the input port of the TFF cell. Vin and Vout1 are the average input voltage and output voltage, respectively. The scale of the supplied sinusoidal voltage (Vsin) is 2 V/div. and the sinusoidal current is supplied to a Josephson junction located at the input port via a resister of 10 kΩ. The scale of the input voltage (Vin) is 200 μV/div., which corresponds to 96.7 GHz/div. The scale of the output voltage (Vout) is 100 μV/div. From these measurements, the maximum operating frequency of the TFF cell is 400 GHz. In the correct operation region, the input voltage is equal to twice the output voltage (Vout1).

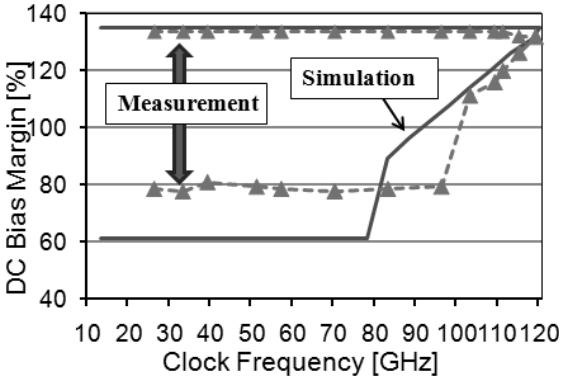


Fig. 6 Dependence of dc bias margin of the 4-bit concurrent-flow shift register. The solid line shows simulated result and the dashed line corresponds to measured results. The maximum operating frequency is 120 GHz.

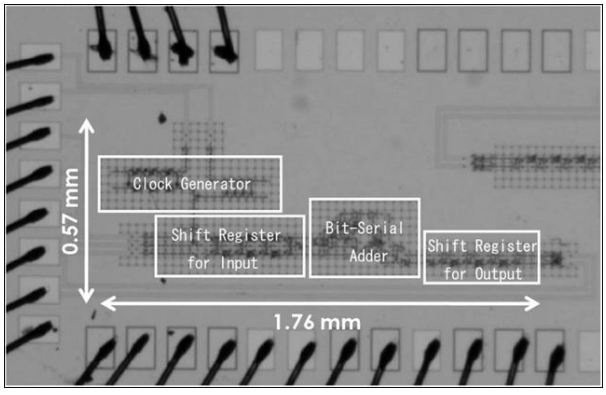


Fig. 7 Microphotograph of the tested bit-serial adder including some peripheral circuit for the on-chip high-speed test. The number of Josephson junctions of the test circuit is 582.

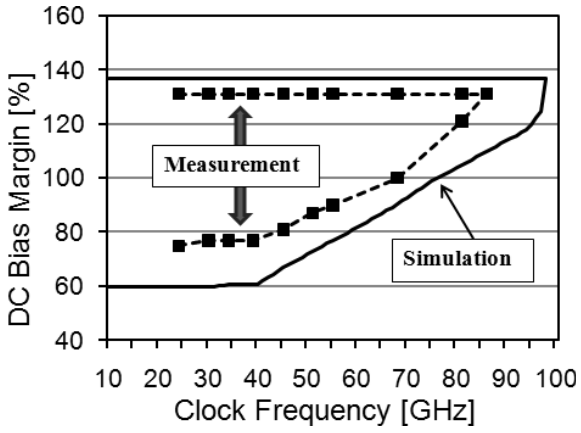


Fig. 8 Dependences of measured and simulated dc bias margins of the bit-serial adder on the clock frequency. The solid line corresponds to simulated result. The dashed line corresponds to the measured result.

4. Conclusion

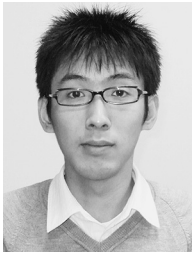
We have developed the SFQ cell library for the SRL 10 kA/cm^2 Nb multi-layer process. In the new cell library the critical current density and McCumber-Stwart parameter are increased to enhance the operating frequency. The integration level is improved compared to our previous cell library due to the reduced unit cell size. We have designed and tested more than 300 cells and confirmed the stable operation of all cells. We have performed a high-speed test of the toggle flip-flop (TFF) cell and confirmed the correct operation at the input frequency of up to 400 GHz. We have demonstrated the high-speed operation of several fundamental circuits. We have experimentally confirmed that our shift resister circuit can operate correctly with clock frequencies of more than 100 GHz. Furthermore, we have also demonstrated the validity of digital circuit simulation for the new cell library.

Acknowledgments

The authors would like to thank all the CONNECT members: SRL-ISTEC, Nagoya University and Yokohama National University.

References

[1] K.K. Likharev and V.K. Semenov, "RSFQ logic/memory family: A new Josephson-junction technology for sub-terahertz-clock-frequency digital systems," IEEE Trans. Appl. Supercond., vol.1, no.1, pp.3–28, 1991.
[2] N. Yoshikawa and K. Koshiyama, "Top-Down RSFQ logic design based on a binary decision diagram," IEEE Trans. Appl. Supercond., vol.11, no.1, pp.1098–1101, 2001.
[3] S. Yorozu, Y. Kameda, H. Terai, A. Fujimaki, T. Yamada, and S. Tahara, "A single flux quantum standard logic cell library," Physica C, vol.378–381, pp.1471–1474, 2002.
[4] S. Nagasawa, Y. Hashimoto, H. Numata, and S. Tahara, "A 380 ps, 9.5 mW Josephson 4-kbit RAM operated at a high bit yield," IEEE Trans. Appl. Supercond., vol.5, no.2, pp.2447–2452, 1995.
[5] Y. Yamanashi, M. Tanaka, A. Akimoto, H. Park, Y. Kamiya, N. Irie, N. Yoshikawa, A. Fujimaki, H. Terai, and Y. Hashimoto, "Design and implementation of a pipelined bit-serial SFQ microprocessor, CORE1beta," IEEE Trans. Appl. Supercond., vol.17, no.2, pp.474–477, 2007.
[6] Y. Kameda, S. Yorozu, Y. Hashimoto, H. Terai, A. Fujimaki, and N. Yoshikawa, "High-speed demonstration of single-flux-quantum cross-bar switch up to 50 GHz," IEEE Trans. Appl. Supercond., vol.15, no.1, pp.6–10, 2005.
[7] T. Satoh, K. Hinode, S. Nagasawa, Y. Kitagawa, and M. Hidaka, "Improvement of fabrication process for 10-kA/cm^2 multi-layer Nb integrated circuits," IEEE Trans. Appl. Supercond., vol.17, no.2, pp.169–172, 2007.
[8] S. Nagasawa, T. Satoh, K. Hinode, Y. Kitagawa, M. Hidaka, H. Akaike, A. Fujimaki, K. Takagi, N. Takagi, and N. Yoshikawa, "New Nb multi-layer fabrication process for large-scale SFQ circuits," Physica C, vol.469, pp.1578–1584, 2009.
[9] Y. Hashimoto, S. Yorozu, Y. Kameda, and V.K. Semenov, "A design approach to passive interconnects for single flux quantum logic cells," IEEE Trans. Appl. Supercond., vol.13, no.2, pp.535–538, 2003.
[10] H. Akaike, A. Fujimaki, S. Nagasawa, Y. Kitagawa, and M. Hidaka, "Effects of the film thickness of a ground plane in the SFQ circuits with a dc-power layer," Supercond. Sci. Technol., vol.20, pp.S336–340, Oct. 2007.
[11] K. Fujiwara, S. Nagasawa, Y. Hashimoto, M. Hidaka, N. Yoshikawa, M. Tanaka, H. Akaike, A. Fujimaki, K. Takagi, and N. Takagi, "Research on effective moat configuration for Nb multi-layer device structure," IEEE Trans. Appl. Supercond., vol.19, no.3, pp.603–606, 2009.
[12] K. Takagi, M. Tanaka, S. Iwasaki, R. Kasagi, I. Kataeva, S. Nagasawa, T. Satoh, H. Akaike, and A. Fujimaki, "SFQ propagation properties in passive transmission lines based on a 10-Nb-layer structure," IEEE Trans. Appl. Supercond., vol.19, no.3, pp.617–620, 2009.
[13] W. Chen, A.V. Rylyakov, V. Patel, J.E. Lukens, and K.K. Likharev, "Superconductor digital frequency divider operating up to 750 GHz," Appl. Phys. Lett., vol.73, pp.2817–2819, 1998.
[14] T. Kainuma, H. Park, K. Taketomi, H. Hara, Y. Yamanashi, N. Yoshikawa, M. Tanaka, Y. Ito, A. Fujimaki, N. Takagi, K. Takagi, and S. Nagawasa, "Design and high-speed tests of component circuits of an SFQ half-precision floating-point adder using 10 kA/cm^2 Nb process," Int. Supercond. Elect. Conf., Fukuoka, Japan, June 2009.
[15] Z.J. Deng, N. Yoshikawa, S.R. Whiteley, and T. Van Duzer, "Data-driven self-timed RSFQ high-speed test system," IEEE Trans. Appl. Supercond., vol.7, no.4, pp.3830–3833, 1997.



Yuki Yamanashi received the B.S., M.E., and Ph.D. degrees in electrical and computer engineering from Yokohama National University, in 2003, 2005, and 2007, respectively. Since 2007, he has been with Interdisciplinary Research Center, Yokohama National University. His current research is on a novel application of superconductive circuit. He is a member of the Japan Society of Applied Physics.

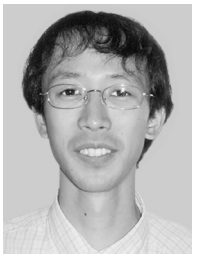
Toshiki Kainuma received the B.S. degree in electrical and computer engineering from Yokohama National University, in 2009, respectively. Since 2009, he has been with the graduate school, Yokohama National University. His current research is on a novel digital application of superconductive circuit. He is a member of the Institute of Electrical and Electronics Engineering.

Nobuyuki Yoshikawa received the B.E., M.E., and Dr.Eng. degrees in electrical and computer engineering from Yokohama National University, Japan, in 1984, 1986, and 1989, respectively. Since 1989, he has been with the Department of Electrical and Computer Engineering, Yokohama National University, where he is currently a Professor. His research interests include superconductive devices and their applications to digital and analog circuits. He is also interested in single-electron-tunneling devices and quantum computing devices. Prof. Yoshikawa is a member of the Japan Society of Applied Physics, and the Institute of Electrical Engineering of Japan.

Irina Kataeva received the M.Sc. degree in physics from Moscow State University and Ph.D. degree in Microtechnology and Nanoscience from Chalmers University of Technology in 2003 and 2007, respectively. Since 2007, she has been with Department of Quantum Engineering, Nagoya University. Her current research is on Single Flux Quantum logic and its applications to high-end computing.

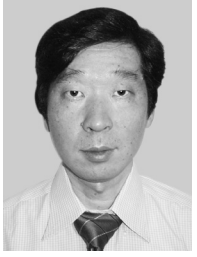
Hiroyuki Akaike received the B.E., M.E., and Ph.D. degrees in electronic engineering from Nagoya University in 1990, 1992, and 1995, respectively. Since 1995, he has been with Nagoya University. In 2003, he stayed in Superconductivity Research Laboratory, ISTEC to be engaged in the development of Nb advanced fabrication process for a year. He has been involved in the research of superconducting devices and fabrication processes. He is a member of the Japan Society of Applied Physics.

Akira Fujimaki received his B.E., M.E., and Dr.Eng. degrees from Tohoku University in 1982, 1984, and 1987, respectively. He was a Visiting Assistant Research Engineer at the University of California, Berkeley, in 1987. Since 1988, he has been working on superconductor devices and circuits at the School of Engineering, Nagoya University, Nagoya, Japan, where he is currently a professor. His current research interests include single-flux-quantum circuits and their applications based on low- and high-temperature superconductors.



Masamitsu Tanaka received the M.E. and Ph.D. degrees in electronics and information electronics from Nagoya University, Nagoya, Japan, in 2003 and 2006, respectively. He was a JSPS Research Fellow from 2005 to 2007 at Department of Quantum Engineering, and joined Department of Information Engineering, Nagoya University in 2007. His research interests include the ultra-fast computing using single-flux-quantum circuits and logic design methodologies. He is a member of the IEEE and the Japan Society of Applied Physics.

Naofumi Takagi received the B.E., M.E., and Ph.D. degrees in information science from Kyoto University, Kyoto, Japan, in 1981, 1983, and 1988, respectively. He joined Department of Information Science, Kyoto University, as an instructor in 1984 and was promoted to an associate professor in 1991. He moved to Department of Information Engineering, Nagoya University, Nagoya, Japan, in 1994, where he has been a professor since 1998. His current interests include computer arithmetic, hardware algorithms, and logic design. He received Japan IBM Science Award and Sakai Memorial Award of the Information Processing Society of Japan in 1995.



Shuichi Nagasawa received the M.S. and Dr.Eng. degrees from Nagoya University, Japan, in 1983 and 1998. He has been engaged in the research of superconducting integrated circuits, especially on Josephon RAMs since he joined NEC Corporation in 1983. Since 1998, he is working at Superconducting Research Laboratory, ISTEC, Japan, where he has been engaged in the research of single flux quantum (SFQ) circuits and the development of their fabrication process. Dr. Nagasawa is a member of the Japan Society of Applied Physics.

Mutsuo Hidaka received his M.E. in applied physics from Kyushu University in 1982. He also received his Ph.D. in 1998 in electronics engineering from the University of Tokyo. He joined NEC Corporation in 1982, where he worked on various research projects on superconducting digital electronics. He was at Arizona State University as a visiting scientist from 1990 to 1991. In 2002, he temporarily transferred to ISTEC, where he has been working on the research and development of Nb-based single flux quantum (SFQ) circuits. Dr. Hidaka is a member of the Japan Society of Applied Physics.