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Superconductive Combinational Logic Circuit Using Magnetically Coupled SQUID Array

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Abstract

In this paper, we propose the development of superconductive combinational logic circuits. One of the difficulties in designing superconductive single-flux-quantum (SFQ) digital circuits can be attributed to the fundamental nature of the SFQ circuits, in which all logic gates have latching functions and are based on sequential logic. The design of ultralow-power superconductive digital circuits can be facilitated by the development of superconductive combinational logic circuits in which the output is a function of only the present input. This is because superconductive combinational logic circuits do not require determination of the timing adjustment and clocking scheme. Moreover, semiconductor design tools can be used to design digital circuits because CMOS logic gates are based on combinational logic. The proposed superconductive combinational logic circuits comprise a magnetically coupled SQUID array. By adjusting the circuit parameters and coupling strengths between neighboring SQUIDs, fundamental

combinational logic gates, including the AND, OR, and NOT gates, can be built. We have verified the accuracy of the operations of the fundamental logic gates by analog circuit simulations.

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1. Introduction

Logic circuits comprising superconductive devices are promising candidates for use in high-performance computational systems because they have high-speed response and low power consumption. Several superconductive logic circuits such as the superconductive latching logic circuit [1] and the quantum flux parametron [2] have been proposed and developed. Among them, the superconductive single-flux-quantum (SFQ) logic circuit [3], which uses flux quanta in superconductive rings containing Josephson junctions as carriers of information, can operate at a clock frequency of above 100 GHz under ultralow power consumption conditions. High-speed operations of several important digital circuits have been experimentally demonstrated so far [4, 5].

However, it is considerably more difficult to design the SFQ logic circuits than it is to design semiconductor CMOS logic circuits. This can be attributed to the fact that the SFQ logic gates are based on sequential logic, where the output depends not only on the present input but also on the internal state of the gate. Although this characteristic of the SFQ logic circuits makes it suitable for deep pipelining [6], designers of the SFQ circuits are required to adjust the timing of signals and clock inputs to all logic gates very precisely. The precision of the clock supplied to all logic gates is particularly important, and sophisticated clocking schemes for the SFQ logic circuits have been developed to optimally design high-speed SFQ logic circuits [7]. Because of these reasons, there are only a few professional designers who can design large-scale SFQ logic circuits.

In this paper, we propose superconductive combinational logic circuits comprising a SQUID array whose output is a function of only the present input. The design of ultralow-power superconductive digital circuits is facilitated by the development of the

superconductive combinational logic circuits because such circuits do not require the determination of the timing adjustment and a complicated clocking scheme. Moreover, conventional circuit design tools developed for the design of semiconductor CMOS circuits can be used to design the superconductive combinational logic circuits because logic gates of the semiconductor circuits are based on combinational logic. In this paper, we describe the design of the superconductive combinational logic circuit and present the simulation results obtained for the fundamental logic gates to verify their operation.

2. Superconductive Combinational Logic Circuit

The proposed superconductive combinational logic circuit consists of regularly placed basic cells, which store and transmit data. Fig. 1 shows an equivalent circuit of the basic cell. The basic cell consists of two coupled radio frequency SQUIDs. The logic signal is expressed as the existence of an output current flowing through the output inductor L_{out}. This circuit structure is very similar to that of the quantum flux parametron (QFP) [2]; however, this structure does not include a clock current. The input signal is magnetically supplied via mutual inductance of K_{in}. The external current I_{enable} is used to apply an appropriate magnetic field, which is slightly lower than the threshold field, to the SQUID loops to enhance the sensitivity for the input current.

In the initial state, no output current is obtained. However, when the sum of an appropriate bias magnetic field induced by I_{enable} and a magnetic field induced by the input current I_{in} exceeds the threshold value of the SQUID, the Josephson junction J_1 switches, and one flux quantum is then stored in the SQUID loop composed of J_1, L_1, and L_{out}; thus, an output current is obtained. This output current is transmitted to the neighboring SQUID via mutual inductance. This structure is similar to that of the

quantum cellar automata (QCA), in which the logic function is realized in regularly placed cells [8, 9]. Therefore, the proposed circuit can also be applied to asynchronous QCA systems.

Fig. 2 shows the input-output current characteristics of the basic cell. Simulations were performed using circuit parameters in a 2.5 kA/cm^2 Nb standard process used at the Superconductivity Research Laboratory (SRL) [10]. The characteristics were calculated using a superconductive circuit simulator, the Josephson simulator (JSIM) [11]. All the results of circuit simulations reported in this paper were calculated using the JSIM assuming the SRL 2.5 kA/cm^2 Nb standard process. The circuit parameters were determined such that the hysteresis of the characteristics of the SQUID became small. Fig. 2 indicates that the output current becomes larger than the input current when the input current exceeds 49 μA. This implies that an input current greater than 49 μA can be propagated to a neighboring cell when the logic state of the cell changes from "0" to "1." On the other hand, when the logic state of the cell changes from "1" to "0," then the output current falls below in the region of input currents of less than 29 μA at which the output becomes smaller than the input again. Hence, an input current of less than 29 μA is attenuated, and thus, cannot be propagated to the next stage. Therefore, in the case of this superconductive combinational logic circuit, a logic state of "1" implies an input current of more than 49 μA, and a logic state of "0" implies an input current of less than 29 μA.

Fig. 3 shows an equivalent circuit of the magnetically coupled basic cells for signal propagation and the corresponding simulation results. The simulation indicates that the signal can be propagated to the neighboring basic cell, and that the propagation delay

between the basic cells is about 25 ps. I_{enable} can be supplied from an external source as the clock of the CMOS integrated circuit, where processors are composed of combinational logic circuit blocks and pipeline buffers; the clock, supplied to all combinational logic circuit blocks, is kept to be high until the data are processed by the combinational logic circuit blocks and are then received by the pipeline buffers [12].

The superconductive combinational logic circuit consumes extremely low power on a chip because it does not comprise any on-chip bias resistors. In contrast, in the case of the SFQ logic circuits, the power is mainly dissipated by on-chip bias resistors to provide the bias currents to each Josephson junction. The low power consumption is the most attractive feature of the superconductive combinational circuit.

It should be noted that similar circuits were proposed by Okabe and Hodaka [13]. However, the logic circuit proposed by them requires on-chip bias resistors to provide bias currents to the circuit; thus, our circuit is superior to that of Okabe and Hodaka in terms of power consumption.

3. Simulation Results for Fundamental Logic Gates

Fundamental combinational logic gates can be implemented by adjusting the circuit parameters and coupling strengths between neighboring SQUIDs. In this study, we simulated fundamental logic gates including AND, OR, and NOT gates. A buffer circuit, the basic cell shown in Fig. 1, was used to connect distant logic gates. We verified that the logic circuits composed of multiple logic gates operated correctly by inserting at least one stage of the buffer circuit. Further, the specialized buffer circuit, which has a fan-out of 2, can be realized by optimizing the circuit parameters. Fig. 4 shows an equivalent circuit of the buffer circuit with a fan-out of 2. The driving capacity is

enhanced by making the critical currents of the Josephson junctions higher than those of the buffer circuit shown in Fig. 1; however, in this case, the power consumption of the circuit becomes slightly large.

Fig. 5 shows an equivalent circuit of the AND and OR gates. Though the circuit structures are identical, the circuit parameters are different. For the AND gate, the output inductance is adjusted such that an output current of more than 55 μA is obtained when two input currents are supplied. On the other hand, for the OR gate, the output inductance is adjusted to be larger than that of the AND gate, and an output current is obtained even when only one input current is supplied.

Fig. 6 shows the input-output characteristics and the simulation results for the AND gate. Although the output current smaller than the threshold is observed in the simulation for the (1, 0) input, the current is attenuated during propagation. It should be noted that the output of the AND logic gate depends on only the input currents I_{in1} and I_{in2}, which indicates that this gate follows combinational logic. The delay time of the AND gate is 42 ps.

Fig. 7 shows the input-output characteristics and the simulation results of the OR gate. The output signal is obtained from one input. The delay time of the OR gate is 26 ps. Fig. 8 shows an equivalent circuit and the simulation results for the NOT gate. The output is inverted by applying a dc current I_{bias} to the basic cells. The propagation delay of the NOT gate is 25 ps.

4. Conclusion

In this paper, we have proposed a superconductive combinational logic circuit that would enable us to design ultralow-power digital circuits easily. The proposed

superconductive combinational logic gates are composed of magnetically coupled SQUID arrays, and the logic operations are performed by transmitting the output currents to a neighboring SQUID. We have performed simulations of the fundamental logic gates including the NOT, AND, and OR gates. Consequently, we have confirmed that the outputs of the gates depend on only the present inputs. This study confirms that complicated superconductive digital circuits can be effectively designed using superconductive combinational logic circuits.

Acknowledgement

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Figure Captions

Fig. 1. Equivalent circuit of basic cell. All Josephson junctions are resistively shunted to adjust the McCumber parameters of junctions (β_C) to ~1. L_{in} = 5 pH, $L_1 = L_2$ = 0.7 pH, $L_3 = L_4$ = 10 pH, L_5 = 9.64 pH, L_{out} = 7.5 pH, $J_1 = J_2$ = 100 μA, K_{in} = 0.4, and $K_1 = K_2$ = 0.2.

Fig. 2. Input-output current characteristics of the basic cell shown in Fig. 1 when the external current I_{enable} of 1.3 mA is applied. I_{enable} is used to apply an appropriate magnetic field and to adjust the input-output current characteristics to the arbitrary logic function.

Fig. 3. Simulation results of signal propagation. (a) Equivalent circuit and (b) simulated waveform. The two basic cells shown in Fig. 1 are magnetically coupled by mutual inductances with a coupling factor of 0.2. The input is cancelled when I_{enable} is not supplied.

Fig. 4. Equivalent circuit of buffer circuit with a fan-out of 2. L_{in} = 5 pH, $L_1 = L_2$ = 0.7 pH, $L_3 = L_4$ = 10 pH, L_5 = 9.64 pH, L_{out1} = 7.5 pH, L_{out2} = 7.5 pH, $J_1 = J_2$ = 140 μA, K_{in} = 0.4, and $K_1 = K_2$ = 0.2.

Fig. 5. Equivalent circuit of AND and OR gates.

Fig. 6. (a) Input-output characteristics and (b) simulation results for AND gate. $L_{in1} = L_{in2}$ = 5 pH, $L_1 = L_2$ = 0.7 pH, $L_3 = L_4$ = 10 pH, $L_5 = L_6$ = 9.64 pH, L_{out} = 5 pH, $J_1 = J_2$ =

100 μA, $K_{in1} = K_{in2} = 0.4$, and $K_1 = K_2 = 0.2$.

Fig. 7. (a) Input-output characteristics and (b) simulation results of OR gate. $L_{in1} = L_{in2} = 5$ pH, $L_1 = L_2 = 0.7$ pH, $L_3 = L_4 = 10$ pH, $L_5 = L_6 = 9.64$ pH, $L_{out} = 3$ pH, $J_1 = J_2 = 100$ μA, $K_{in1} = K_{in2} = 0.4$, and $K_1 = K_2 = 0.2$.

Fig. 8. (a) Equivalent circuit and (b) simulation results of NOT gate. $K_1 = K_2 = 0.2$, $L_{bias} = 5$ pH, and $K_{bias} = -0.2$. Other circuit parameters are the same as those of the basic circuit shown in Fig. 1. The input is inverted by applying another dc bias I_{bias}.

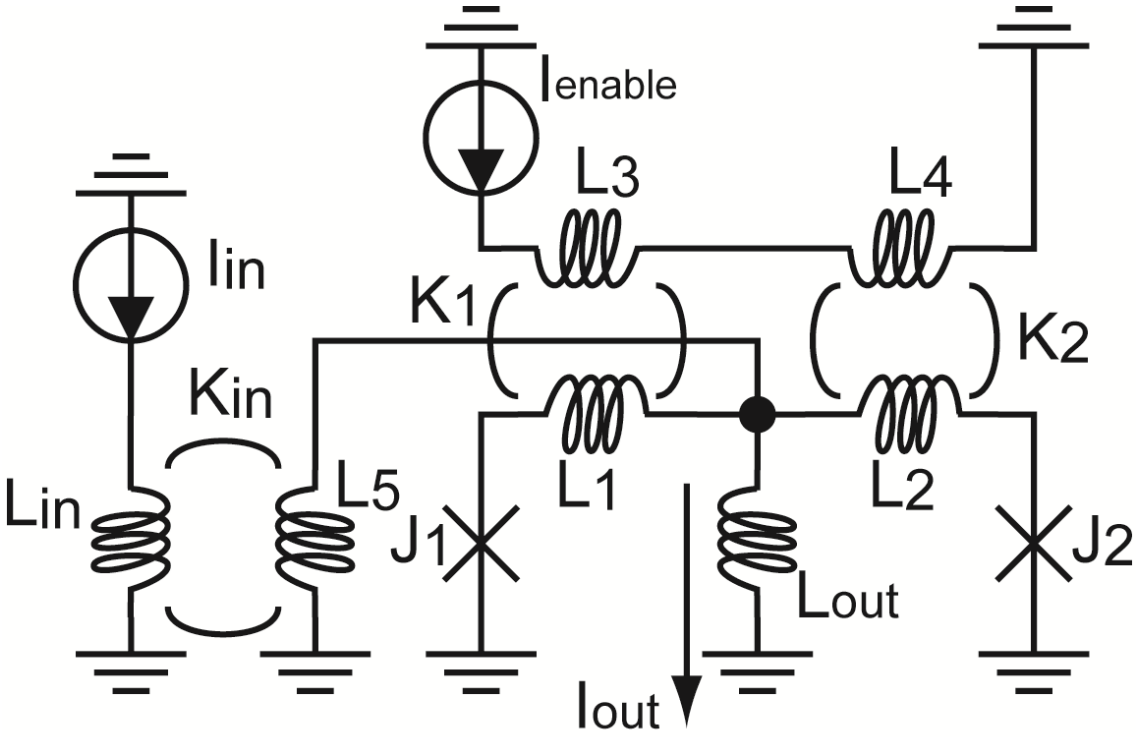


Fig. 1

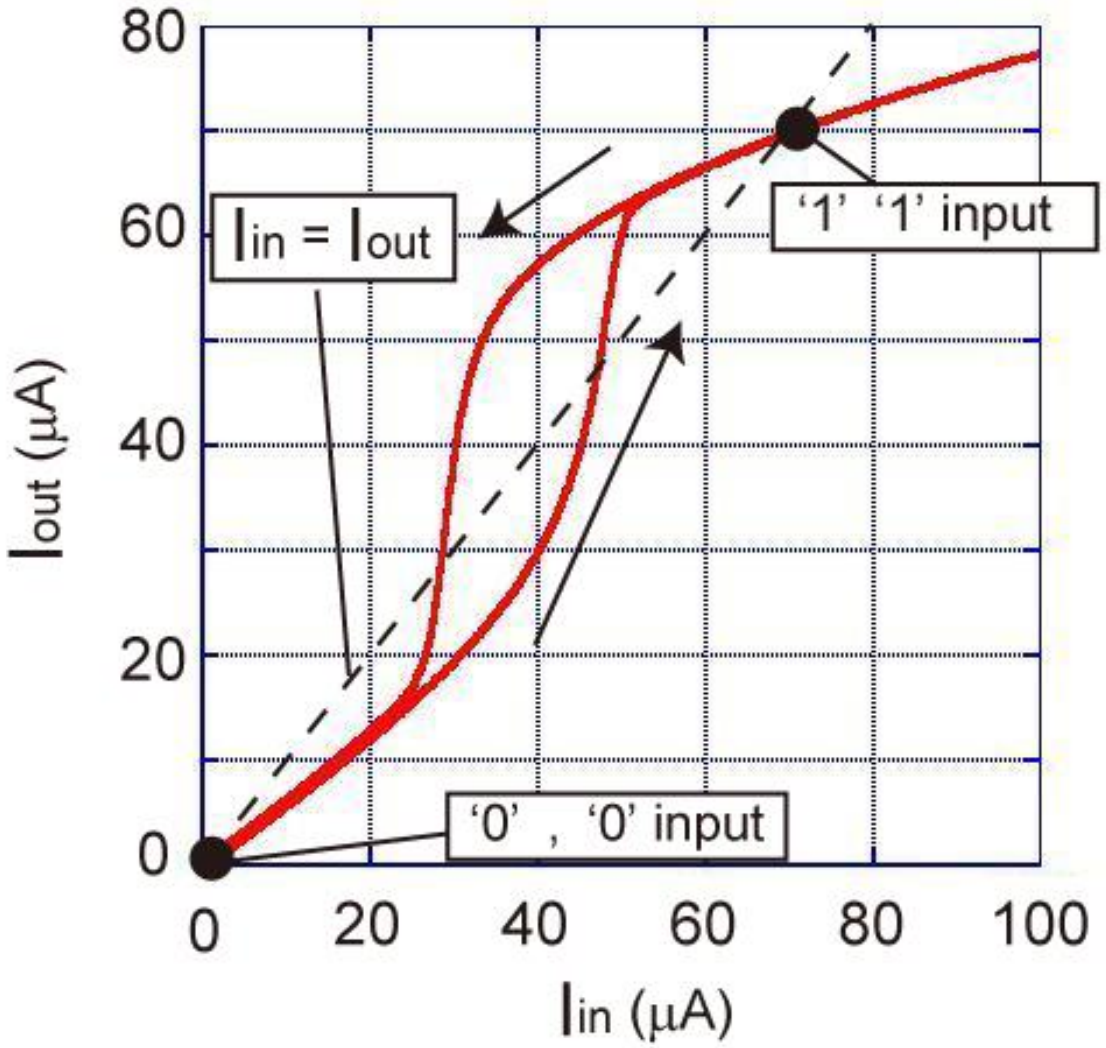
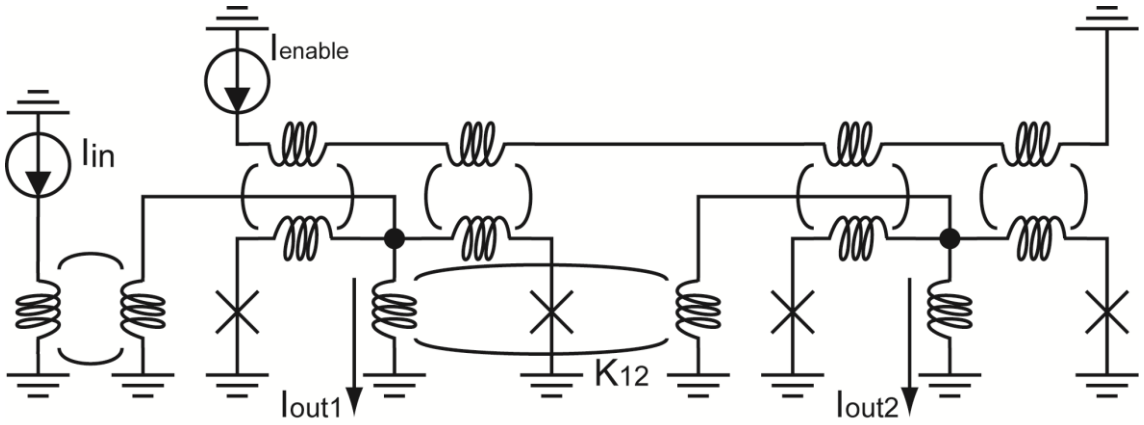
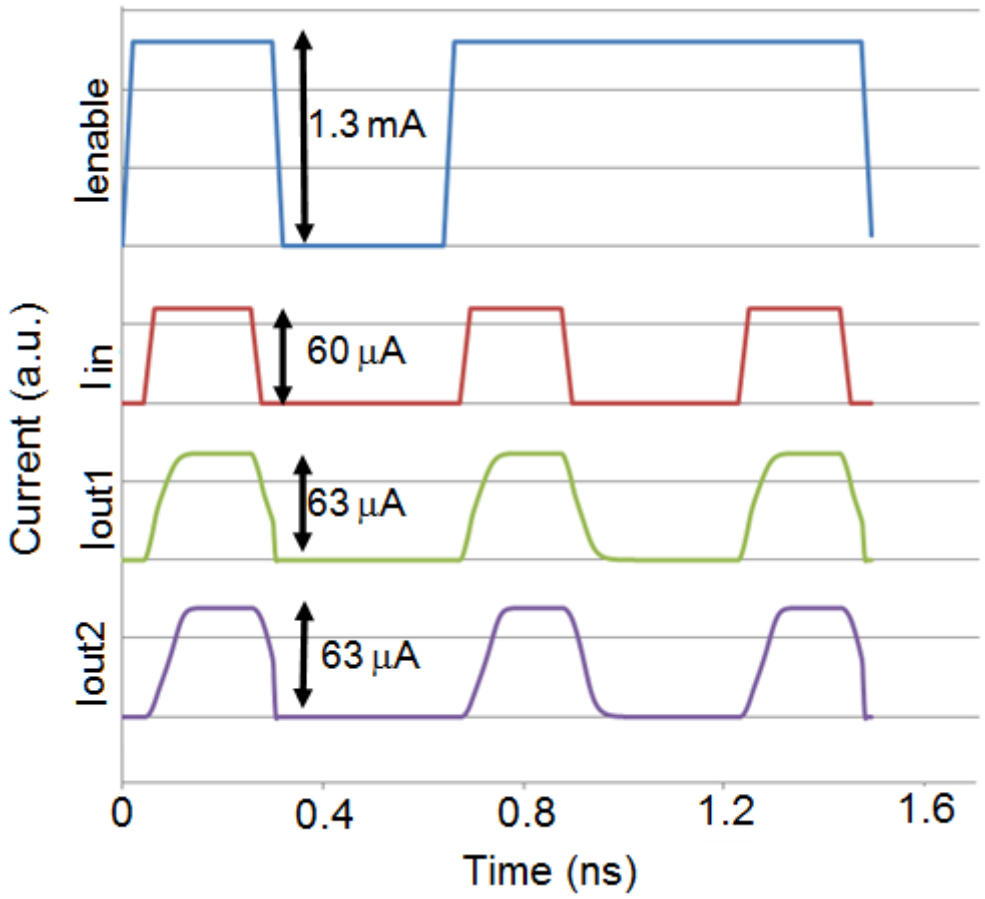

80
60
40
20
0
0
20
40
60
80
100
Iout (μA)
Iin (μA)
Iin = Iout
'1' '1' input
'0' , '0' input

Fig. 2


Ienable
Iin
Iout1
K12
Iout2

(a)


Ienable
1.3 mA
Iin
60 µA
Iout1
63 µA
Iout2
63 µA
Current (a.u.)
0
0.4
0.8
1.2
1.6
Time (ns)

(b)

Fig. 3

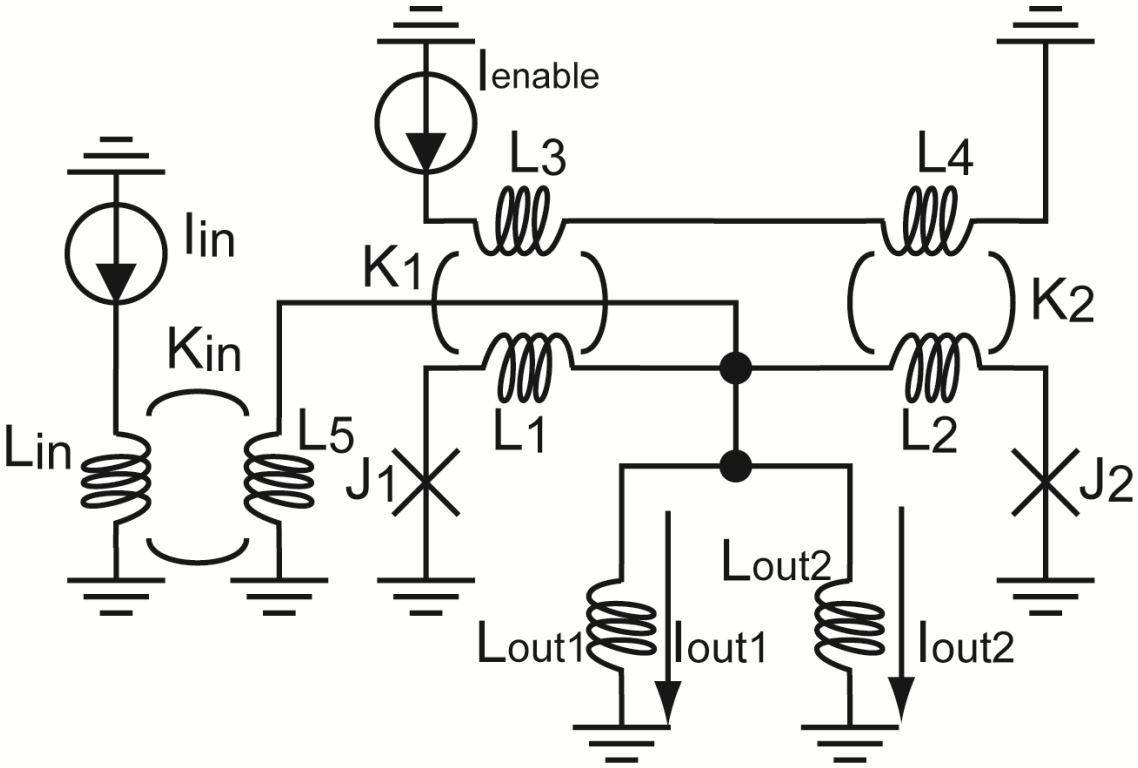

Ienable
L3
L4
Iin
K1
K2
Kin
Lin
L5
J1
L1
L2
J2
Lout2
Lout1
Iout1
Iout2

Fig. 4

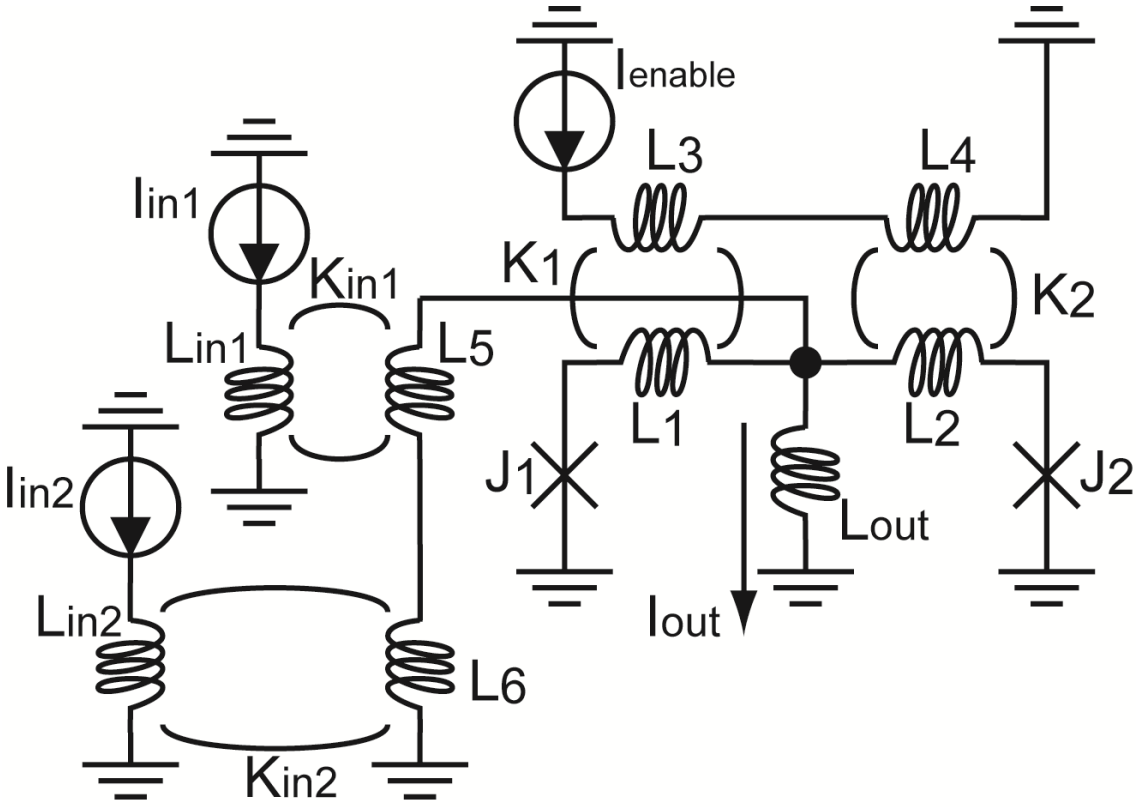
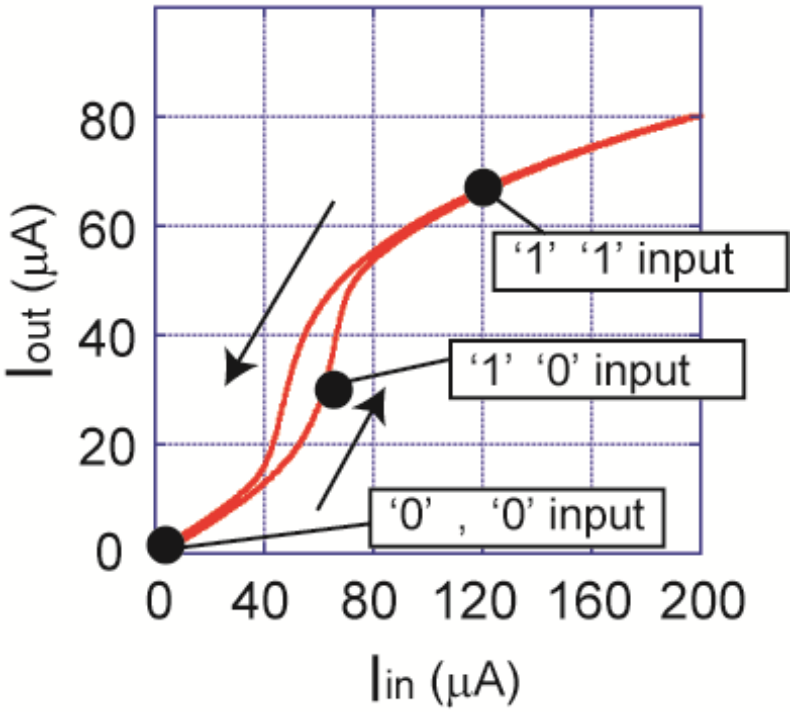
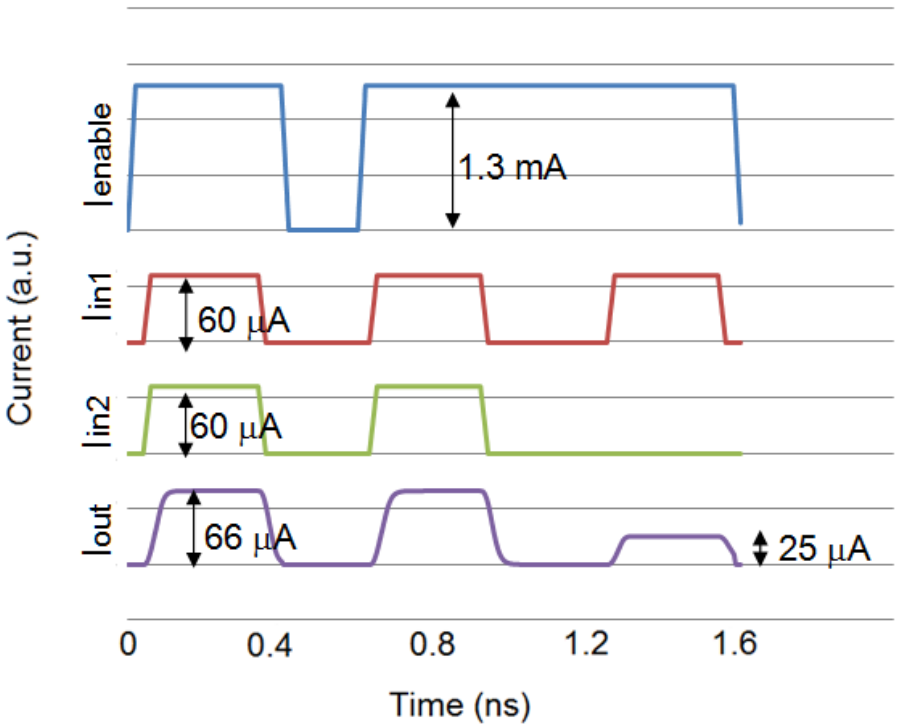

Ienable
L3
L4
Iin1
Kin1
K1
K2
Lin1
L5
L1
L2
J1
J2
Lout
Iin2
Iout
Lin2
L6
Kin2

Fig. 5

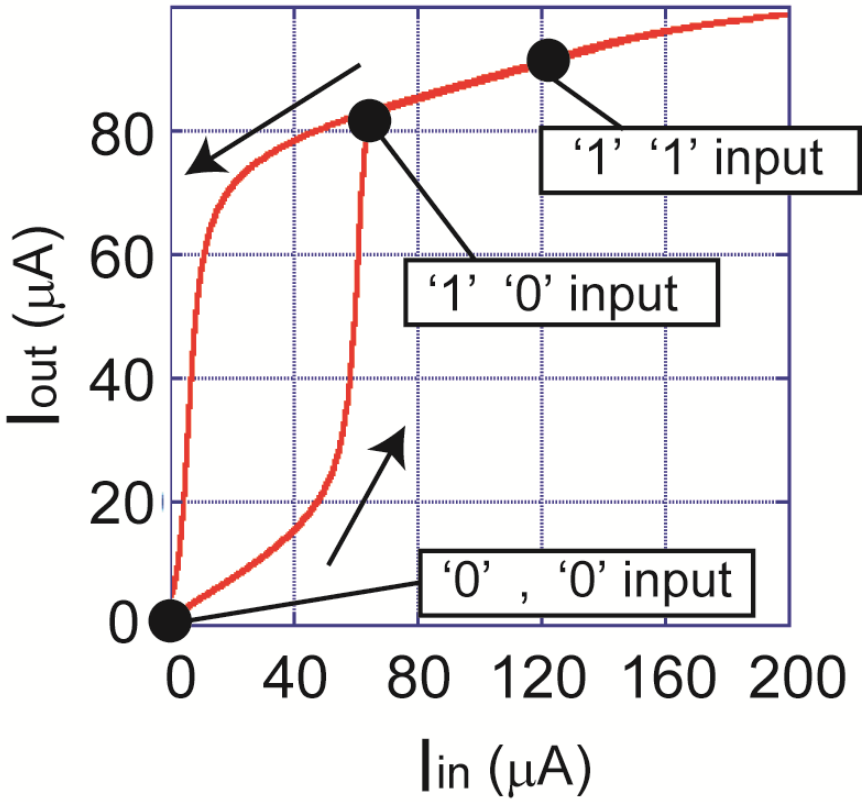

80
60
40
20
0
Iout (μA)
0
40
80
120
160
200
Iin (μA)
'1' '1' input
'1' '0' input
'0' , '0' input

(a)

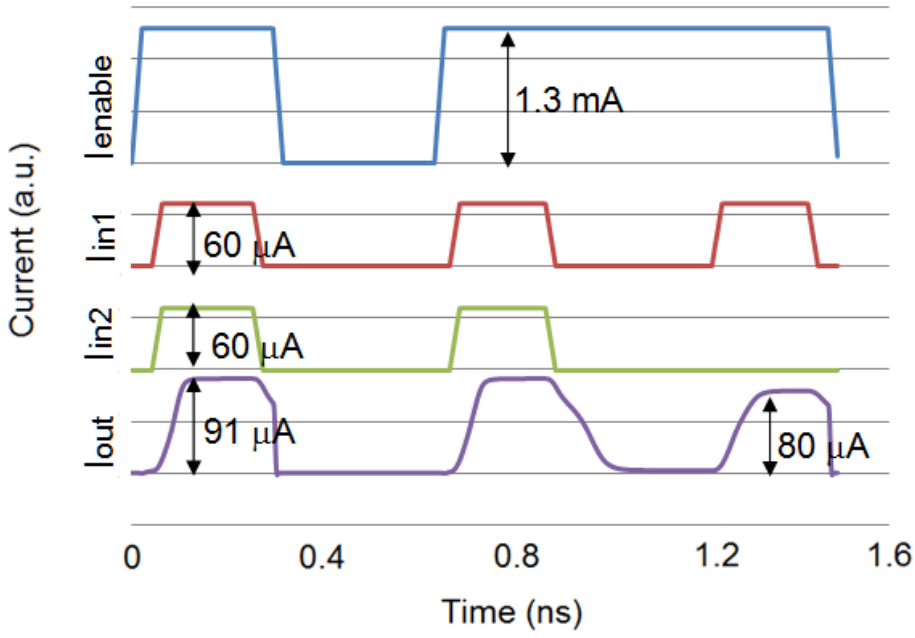

Ienable
1.3 mA
Iin1
60 μA
Iin2
60 μA
Iout
66 μA
25 μA
Current (a.u.)
0
0.4
0.8
1.2
1.6
Time (ns)

(b)

Fig. 6

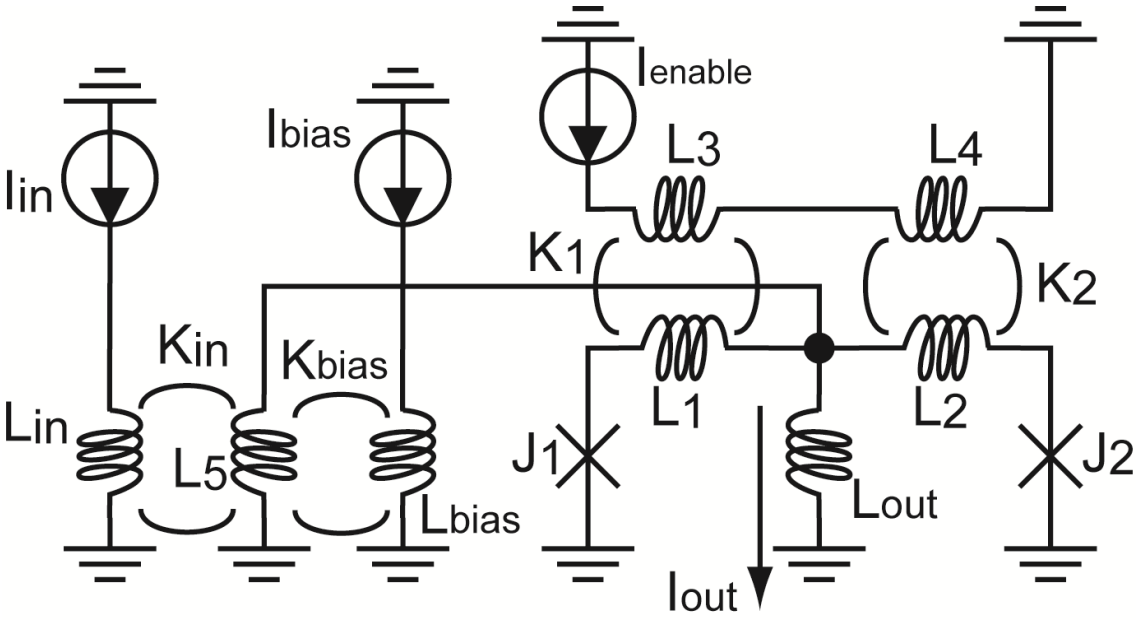

80
60
40
20
0
Iout (μA)
0
40
80
120
160
200
Iin (μA)
‘1’ ‘1’ input
‘1’ ‘0’ input
‘0’ , ‘0’ input

(a)

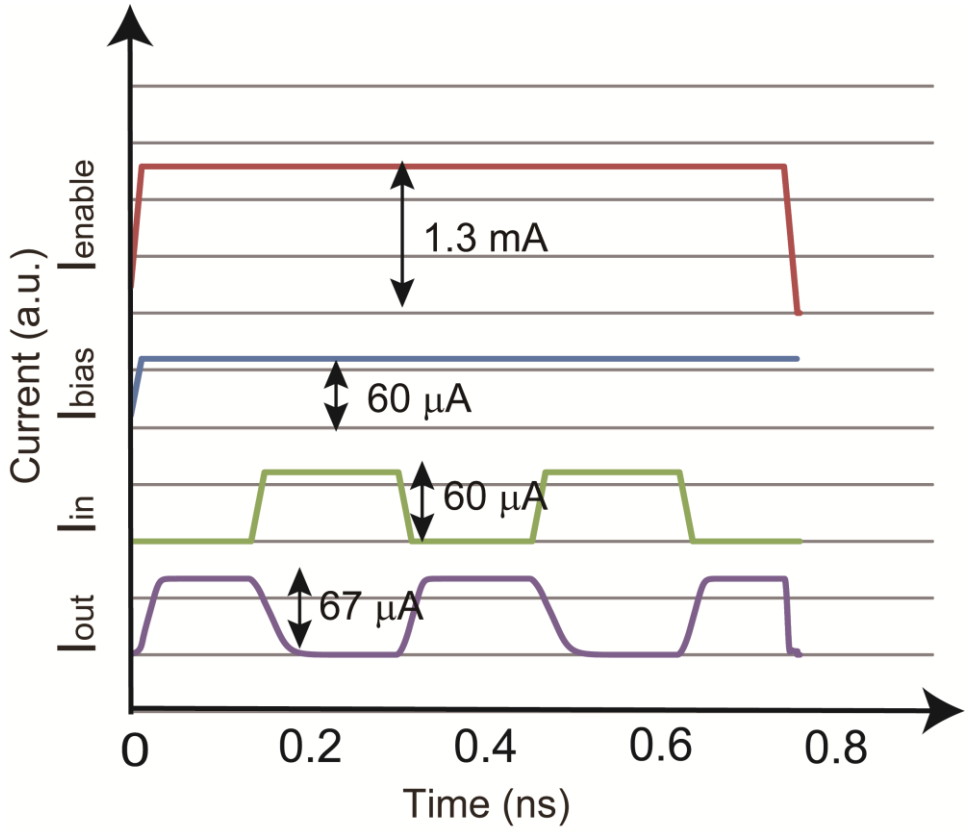

Current (a.u.)
Ienable
1.3 mA
Iin1
60 μA
Iin2
60 μA
Iout
91 μA
80 μA
0
0.4
0.8
1.2
1.6
Time (ns)

(b)

Fig. 7


Iin
Ibias
Ienable
L3
L4
K1
K2
Kin
Kbias
Lin
L5
Lbias
L1
L2
J1
J2
Lout
Iout

(a)


Current (a.u.)
Ienable
Ibias
Iin
Iout
1.3 mA
60 μA
60 μA
67 μA
0
0.2
0.4
0.6
0.8
Time (ns)

(b)

Fig. 8