Design Approach of Dynamically Reconfigurable Single Flux Quantum Logic Gates

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***Abstract*— Novel reconfigurable superconductive single flux quantum (SFQ) logic devices, the functions of which can be dynamically reconfigured by inputting control signals, have been investigated. The characteristics of single flux quantum circuits can be easily modulated by applying currents or magnetic fields because of the high sensitivity of superconductive circuits. We investigated several design approaches for the realization of dynamically reconfigurable SFQ logic devices. We employed direct current injection to the logic gate using a non-destructive read-out flip-flop. By changing the internal state of the non-destructive read-out flip-flop, the logic function can be dynamically reconfigured. We have designed and tested a dynamically reconfigurable Josephson transmission line (JTL)/delay flip-flop (DFF) circuit. The measured dc bias margin was 72.5–107.2%. Furthermore, we have demonstrated the operation of a variable bit-length shift register, composed of the dynamically reconfigurable JTL/DFF circuits. The investigated design approach can be applied to more sophisticated dynamically reconfigurable single flux quantum logic gates.**

***Index Terms*—Single flux quantum circuit, Reconfigurable logic device, Josephson junction**

I. INTRODUCTION

RECONFIGURABLE logic devices, the logic functions of which can be changed after circuit implementation, are extremely useful for practical applications. Reconfigurable logic devices implemented using semiconductor circuit technologies such as field-programmable gate arrays (FPGAs) are widely used.

Reconfigurable logic devices have also been proposed and implemented in the field of superconductive digital electronics, particularly, in single flux quantum (SFQ) [1]. SFQ technology is suitable for implementing reconfigurable logic devices because an SFQ circuit consists of connected superconductive loops containing Josephson junctions (SQUIDs) that are very sensitive to magnetic fields and currents. In [2,3], superconductive FPGAs were implemented by applying dc control currents to the circuit from external equipments. Superconductive reconfigurable logic devices can also be implemented by using flux quanta trapped by a superconductive phase shifter [4].

However, both these techniques use dc magnetic field programming superconductive circuits, and thus, are not suitable for high-speed circuit operation. Further, the proposed on-chip dc current generator produces large power dissipation [3].

In this study, we investigated dynamically reconfigurable SFQ logic devices, the logic functions of which can be reconfigured by applying control signals. The implementation method for the dynamically reconfigurable SFQ logic devices and the test results are described.

II. DYNAMICALLY RECONFIGURABLE SUPERCONDUCTIVE LOGIC DEVICES

First, we investigated the implementation of the method to build dynamically reconfigurable superconductive logic devices by designing a dynamically reconfigurable Josephson transmission line (JTL)/delay flip-flop (DFF) circuit. In the dynamically reconfigurable JTL/DFF circuit, the circuit operation of the signal propagation (JTL) and the latching function (DFF) can be reconfigured by inputting control signals. The dynamically reconfigurable JTL/DFF circuit is useful in a control circuit for pipelined SFQ processors designed on the basis of one-hot encoding [5]. The states of the processor can be efficiently skipped to process the exceptions by using the dynamically reconfigurable JTL/DFF circuits.

We have investigated two methods to implement the dynamically reconfigurable JTL/DFF circuit. Fig. 1 shows the circuit schematics of the two implementations. In the circuit illustrated in Fig. 1(a), the inductance of a storage loop in the DFF, L_1, is magnetically coupled to the inductance L_3. In the initial state, where no control signals are input, the circuit behaves as a conventional DFF. The datum, which is input from the "din" port, is stored in the storage loop composed of J_1, L_1, and J_2. The stored datum is released by inputting the clock (clk) signal. When no datum is stored in the storage loop, the clock input is cancelled by the switching event of the escape junction J_4.

However, once a control signal "set_to_jtl" is input and stored in a superconductive loop containing J_5, L_3, and J_6, the magnetic field is applied to the storage loop of the DFF via the mutual inductance between L_1 and L_3. The current flowing in the Josephson junction J_2 is increased by the applied magnetic

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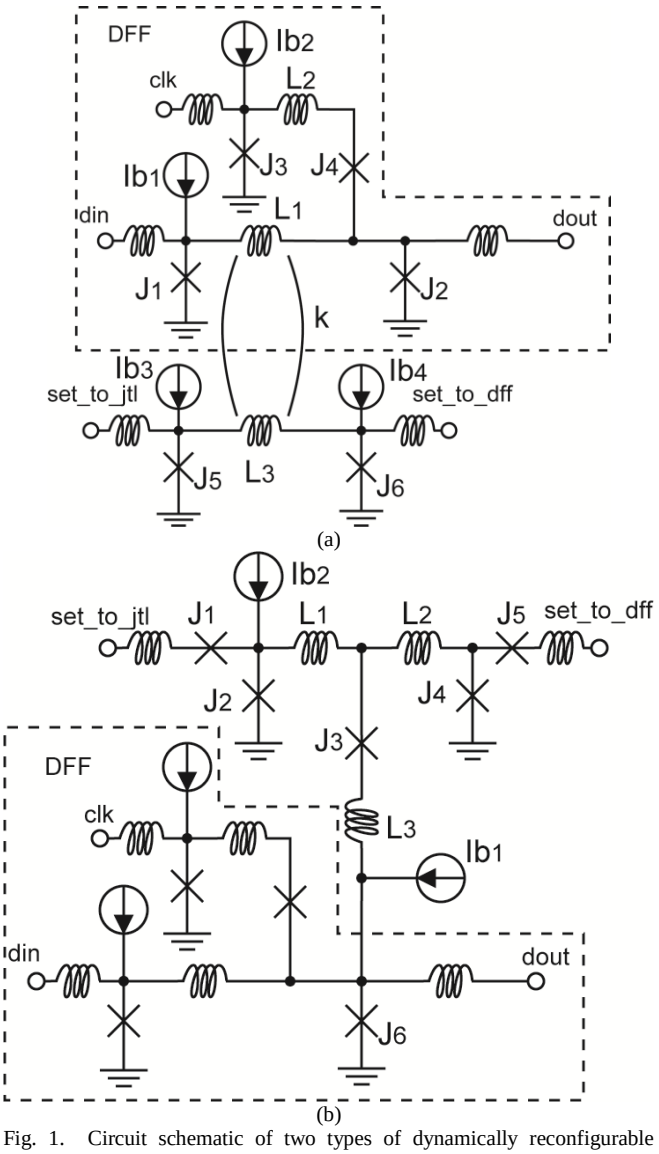


Fig. 1. Circuit schematic of two types of dynamically reconfigurable JTL/DFF circuits. The parts indicated by dashed lines are conventional delay flip-flop (DFF) circuits. In circuit (a), J_1 = 234 μA, J_2 = 169 μA, J_3 = 216 μA, J_4 = 163 μA, J_5 = J_6 = 234 μA, L_1 = 7.9 pH, L_2 = 3.3 pH, L_3 = 10.0 pH, k = 0.4, Ib_1 = 117 μA, Ib_2 = 157 μA, and Ib_3 = Ib_4 = 100 μA. In circuit (b), J_1 = 203 μA, J_2 = 132 μA, J_3 = 100 μA, J_4 =272 μA, J_5 = 225 μA, J_6 = 169 μA L_1 = 0.87 pH, L_2 = 3.0 pH, L_3 =0.45 pH, Ib_1 = 109 μA, and Ib_2 = 104 μA. The other parameters are the same as in circuit (a).

field. In this state, the data input from the "din" port is not stored in the storage loop and directly output to the "dout" port because the current flowing in the Josephson junction J_2 is increased by the magnetic fields and exceeds the critical current by the "din" input. Therefore, the circuit acts as a JTL. In this operating mood, the input datum from the "clk" port causes the switching of J_4, and the clock inputs are cancelled.

The circuit returns to the DFF-mode by applying the "set_to_dff" input that cancels the stored flux quantum in the loop containing L_3.Therefore, we can dynamically reconfigure the circuit operation of the DFF-mode and the JTL-mode by inputting the control signals "set_to_dff" and "set_to_jtl," respectively.

The second investigated circuit is shown in Fig. 1 (b). In this ci The second investigated circuit is shown in Fig. 1(b). In this circuit, a nondestructive read-out flip-flop that stores the control signal in the loop composed of J_2, L_1, J_3, and L_3 is attached to the conventional DFF circuit. The operation principle is similar to that of the circuit shown in Fig. 1(a). A flux quantum input from the "set_to_jtl" port is stored in the superconductive loop composed of J_2, L_1, J_3, and L_3. The circulating current induced by the stored flux quantum increases the current flowing in the Josephson junction J_6 and changes the circuit operation mode to JTL mode. In the JTL mode operation, the datum input from the "din" port is directly output to the "dout" port because the bias current flowing in J_6 is increased by the circulating current and J_6 switches by the "din" input. After the switching event of J_6, the flux quantum stored in the superconductive loop composed of J_2, L_1, J_3, and L_3 remains because the J_3 switch and the nondestructive read-out is performed. The stored flux quantum in the loop composed of J_2, L_1, J_3, and L_3 is released by the "set_to_dff" input, and the operation mode returns to the DFF mode.

We have compared the circuit performances of two dynamically reconfigurable JTL/DFF circuits on the basis of circuit simulation. Although the circuit illustrated in Fig. 1(a) is simple and can be implemented by a small number of

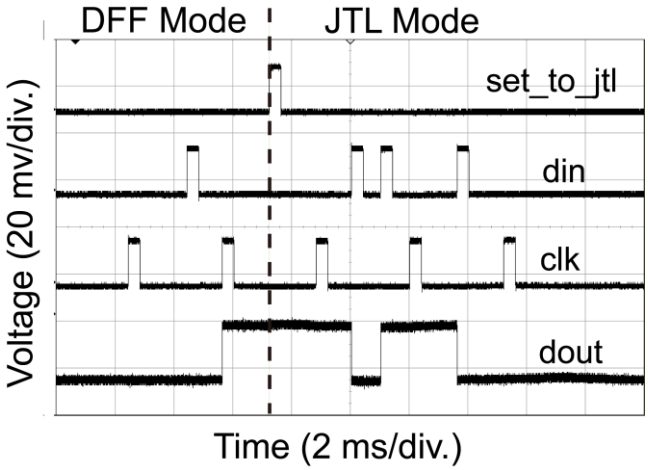


Fig. 2. Measured waveform of the dynamically reconfigurable JTL/DFF circuit. Upper three waveforms are the input sequences, and SFQ signals are input at each rising edge. The lowest waveform is output from the circuits, and each transition expresses the output of SFQ signals. Though "set_to_dff" input is not shown in this figure, it is input at the beginning of the input sequence.

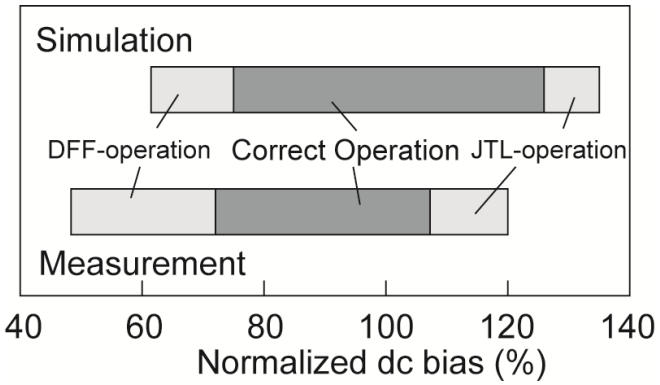


Fig. 3. Comparison of simulated and measured dc bias margins of the dynamically reconfigurable JTL/DFF circuit. In the regions labeled "DFF-operation" and "JTL-operation," the circuit behaves as DFF and JTL in both states. The dc bias is normalized by the designed value, 2.5 mV.

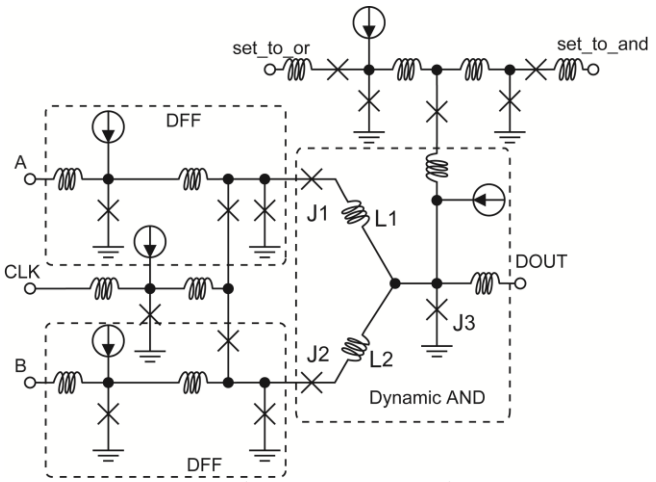


Fig. 4. Equivalent circuit of the dynamically reconfigurable AND/OR gate. $J_1 = J_2 = 154$ μA, $J_3 = 167$ μA, $L_1 = L_2 = 2.6$ pH. Only circuit parameters of the main part are shown. The circuit parameters of non-destructive read-out flip-flop are the same as in the caption of Fig. 1.

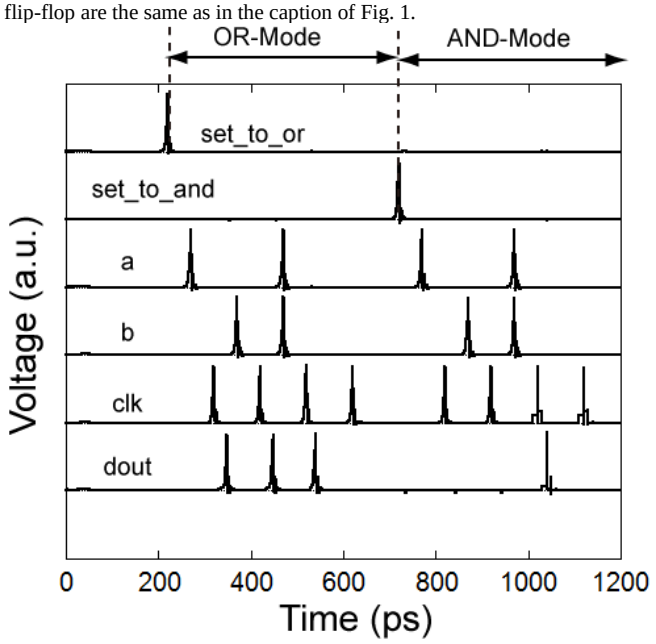
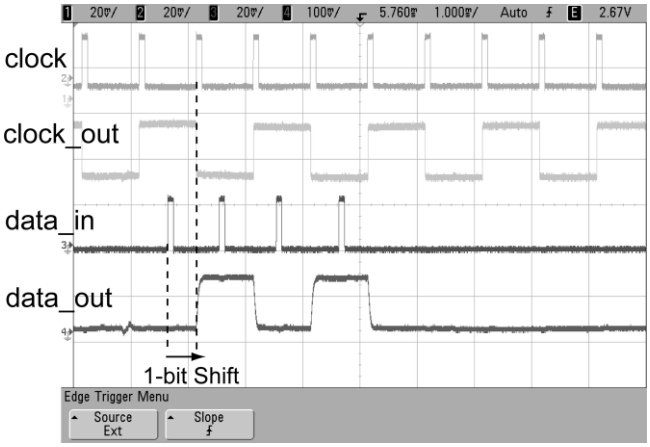


Fig. 5. Simulation result of the dynamically reconfigurable AND/OR gate.

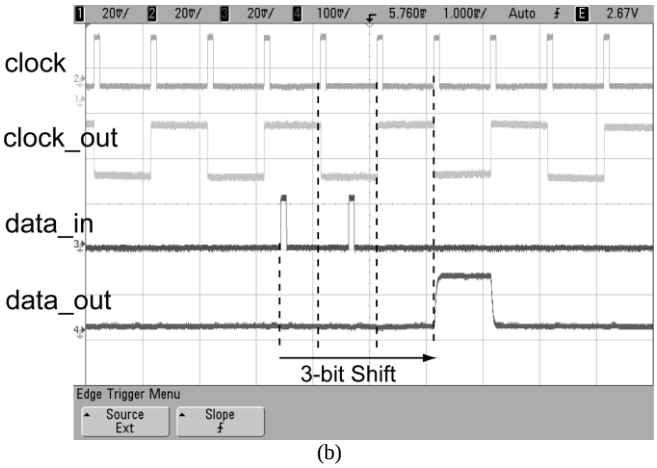
Josephson junctions, the operating margin is small compared to that of the circuit illustrated in Fig. 1(b). In order to obtain an operating margin of larger than ±20%, a large magnetic coupling factor (of more than 0.8) is required according to the circuit simulation if we employ the circuit illustrated in Fig. 1(a). It is very difficult to design such a strong magnetic coupling, and therefore, we selected the circuit illustrated in Fig. 1(b) for implementing the dynamically reconfigurable JTL/DFF circuit.

We designed and tested the dynamically reconfigurable JTL/DFF circuit using the ISTEC 2.5 kA/cm^2 Nb standard 2 process [6]. Further, we determined the correct operation of the dynamically reconfigurable JTL/DFF circuit, as illustrated in Fig. 2. The measured dc bias margin was 72–107%. Fig. 3 shows a comparison of the simulated and measured dc bias margins. If the bias voltage is high and the current flowing in the Josephson junction located at the output part of the DFF is increased, the input signal is not stored and is directly output, even if the "set_to_dff" signal has been input. When the bias voltage is low enough, the circuit operates as JTL. The measurement result shows very reasonable characteristics.

The implementation method discussed above can be applied to implement sophisticated logic gates such as the dynamically reconfigurable AND/OR and NAND/NOR gates. Fig. 4 shows an equivalent circuit of the dynamically reconfigurable AND/OR logic gate. A nondestructive read-out flip-flop is attached to the Josephson junction of the dynamic AND circuit. The dynamic AND circuit outputs when 2 input signals are simultaneously input [7]. The input signals "A" and "B" are stored in the DFFs. Stored "A" and "B" signals are simultaneously input to the dynamic AND. When both the signals are "1," the dynamic AND outputs the datum. Therefore, the whole circuit acts as a clocked AND gate. When the "set_to_or" signal is input, the current flowing in J_3 increases and J_3 switches when only one datum is input. In this state, the whole circuit acts as an OR gate. Therefore, we can reconfigure the circuit functions of the AND gate and the OR gate by inputting the "set_to_and" and the "set_to_or" signals, respectively. Fig. 5 shows a simulated waveform of the dynamically reconfigurable AND/OR gate. The simulated dc bias margin is 89–127%.



(a)



(b)

Fig. 6. Measured waveforms of variable bit-length shift register: (a) the operation of 1-bit shift and (b) 3-bit shift. Input data are output after (a) inputting 1 clock and (b) 3 clocks, respectively.

III. Variable Bit-length Shift Register

We implemented and tested a variable-bit-length shift register, the bit-length of which can be reconfigured from 0-bit to 4-bit, using the dynamically reconfigurable JTL/DFF circuits. The variable-bit-length shift register is composed of four dynamically reconfigurable JTL/DFF circuits. The datum input to the shift register is latched when the dynamically reconfigurable JTL/DFF circuit is set to the DFF-mode. Therefore, we can arbitrarily change the bit-length of the shift register by changing the number of JTL/DFF circuits set to the DFF-mode. The variable bit-length shift register can have various applications such as a bit shifter for a floating-point adder and multiplier [8,9].

Fig. 6 shows the measurement results of the variable bit-length shift register. Measured waveforms of the 1-bit mode and the 3-bit mode operations are shown in Fig. 6. We confirmed that the circuit operates as a variable digital delay (variable-length shift register) by changing the input control signals. The measured dc-bias margin was 71–91% for the 1- to 4-bit-length shift register operation and 71–123% for the JTL mode operation. Although the measured dc bias margin was small, these characteristics can be explained by the characteristics of the dynamically reconfigurable JTL/DFF circuit, as shown in Fig. 3. The experimental data on the shift register is in good agreement with the individual cell analysis shown in Fig. 3.

IV. Conclusion

We have investigated an implementation method for dynamically reconfigurable superconductive logic devices. The logic function could be dynamically reconfigured by modulating the circuit characteristic using the stored flux quantum in a nondestructive read-out flip-flop. Further, we have designed and tested the dynamically reconfigurable JTL/DFF circuit using the ISTEC 2.5 kA/cm^2 Nb standard 2 process and confirmed the correct operation. We have also demonstrated the correct operation of the variable bit-length shift register consisting of dynamically reconfigurable JTL/DFF circuits. This method can be applied to logic gates with more complex functionality, such as AND/OR and NAND/NOR gates.

Acknowledgments

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