Statistical Analysis of Error Rate of Large-Scale Single Flux Quantum Logic Circuit by Considering Fluctuation of Timing Parameters

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Abstract

The relationship between the timing margin and the error rate of the large-scale single flux quantum logic circuits is quantitatively investigated to establish a timing design guideline. We observed that the fluctuation in the set-up/hold time of single flux quantum logic gates caused by thermal noises is the most probable origin of the logical error of the large-scale single flux quantum circuit. The appropriate timing margin for stable operation of the large-scale logic circuit is discussed by taking the fluctuation of setup/hold time and the timing jitter in the single flux quantum circuits. As a case study, the dependence of the error rate of the 1-million-bit single flux quantum shift register on the timing margin is statistically analyzed. The result indicates that adjustment of timing margin and the bias voltage is important for stable operation of a large-scale SFQ logic circuit.

Keywords: Single flux quantum, SFQ circuit, Error rate, Timing design

1. Introduction

A single flux quantum (SFQ) circuit [1, 2] has superior high-throughput characteristics owing to use of magnetic flux quanta in a superconductor as an information carrier. High-frequency SFQ logic circuits that can operate at the clock frequency of several tens of GHz have been implemented for various applications [3-5]. Because of the high-frequency operation of SFQ circuits, unique clocking methods were investigated by utilizing clock skew positively [6].

Not only clock distribution but also precise timing adjustment is indispensable for the design of large-scale SFQ logic circuits because the SFQ logic circuit uses pulse logic, and the logical data are represented by the order of arrival and the arrival time of clock and input signals to each logic gate. Ensuring the appropriate timing margin, which is designed time difference between the arrival of the data and the clock inputs to the logic gates, is needed for the stable operation of the SFQ logic circuit [6]. Because the trade-off between the operation frequency and the operation stability exists, the timing margin should be carefully considered to design complex large-scale SFQ circuits such as the microprocessor [7, 8]. However, a clear guideline for timing design has not been established in terms of operation stability of the SFQ circuit. In this study, we statistically analyze the relationship between the error rate and timing margin of large-scale SFQ circuits by taking timing jitter and fluctuation of the setup/hold time of logic gates into account to build the clear timing design guideline.

2. Analysis of fluctuation of timing parameters of SFQ logic gate

All SFQ logic gates have a timing restriction, which is determined by timing parameters called the setup and hold time. Fig. 1 shows a timing chart of an SFQ delay

flip-flop. In the common synchronized logic circuit, the clock signal is periodically supplied to all logic gates. If the data input collides with clock input, logical error occurs at the logic gate. In the time region near the clock input, the data input is not allowed, and this area is the summation of the setup and hold time of the SFQ logic gate [6]. Assuming the timing margin as the time difference between clock and data inputs, the timing margin should be larger than setup of hold time of the SFQ logic gate. If the data input timing fulfills this timing constraint at all logic gates, the SFQ logic can operate correctly.

In actual circuits, thermal noises that fluctuate the signal propagation time affect the circuit operation. The influence of the timing jitter on the SFQ circuit operation was experimentally evaluated [9]. However, the setup and hold time of the SFQ circuit is also fluctuated by influences of thermal noises. Therefore, not only timing jitter but also fluctuation of the setup and hold time of the logic gate should be considered for robust SFQ circuit design.

We numerically evaluated the setup and hold time of each SFQ logic gate taking thermal noises at 4.2 K into account by using WRspice [10]. The assumed circuit fabrication process is the AIST 2.5 kA/cm^2 Nb standard process 2 [11]. Fig. 2 (a) shows the input data pattern used in this analysis of the delay flip-flop with an escape junction (DFFE). In the ideal case, where no thermal fluctuation exists, the SFQ signal does not form the output when the time difference between clock and data input (t_{din} - t_{clk}) is larger than the hold time. However, the output probability of the DFFE gradually transits from 1 to 0 with an increase in (t_{din} - t_{clk}) due to thermal noises. We calculated the dependence of output probability of the DFFE on (t_{din} - t_{clk}). We compared the characteristics of DFFEs driven by different bias voltages (V_b). Fig. 2 (b) shows

dependences of the output probability of the DFFE on (t_{din} - t_{clk}). Because fluctuation of timing parameters is caused by thermal fluctuations that obey the Gaussian distribution [12, 13], the transition curves in Fig. 1 (b) are fitted to the following equation including the error function (erf),

$$P(t_{din} - t_{clk}) = 0.5 - 0.5 \cdot erf\left\{\frac{(t_{din} - t_{clk}) - \mu_{hold}}{\sqrt{2}\sigma_{hold}}\right\}, \quad (1)$$

where μ_{hold} is the time difference value when the output probability of the DFFE is 0.5, and σ_{hold} is standard deviation of fluctuation of hold time of the DFFE. By fitting the characteristics to eq. (1) the μ_{hold} and σ_{hold} are obtained. Using the similar method, we calculated average and standard deviation values of the DFFE setup time.

Fig. 3 shows the input data pattern for the analysis and calculated output probability of the DFFE on time difference between the clock and data inputs. Average and standard deviation of setup time (μ_{setup} and σ_{setup}) of the DFFE is obtained by comparing calculated characteristics and the following equation,

$$P(t_{clk} - t_{din}) = 0.5 - 0.5 \cdot erf\left\{\frac{(t_{clk} - t_{din}) - \mu_{setup}}{\sqrt{2}\sigma_{setup}}\right\}. \quad (2)$$

Table 1 summarizes average (μ) and standard deviation (σ) values of the setup and hold time of the DFFE. One can see that the fluctuation of the setup and hold time is larger than the timing jitter, the typical value of which is 0.7 ps/junction [14]. Therefore, the main origin of the error of the SFQ logic circuits is not the timing jitter but fluctuation of the setup and hold time of the logic gate.

3. Statistical analysis of error rate of large-scale SFQ logic circuit

We statistically analyzed the relationship between the designed timing margin and the

error rate of the large-scale SFQ circuit. As a case study, we analyzed the error rate of the 1 million-bit shift register composed of DFFE cells as a function of the timing margin between the clock and data input for each DFFE cell. Fig. 4 shows the block diagram of the 1 million-bit concurrent-flow shift register and the input time chart for each DFFE cell. In this case, we define timing margin (Δt) as time difference between data and clock input for DFFE cells as shown in Fig. 4 (b). The operating frequency of the shift register is the inverse of the clock input frequency T.

Assuming fluctuation of the setup and hold time of SFQ logic gate and the timing jitter is independent, and the data and clock lines that connect the adjacent DFFEs are composed of 10 junction Josephson transmission lines, the fluctuation of setup/hold time and signal propagation time can be combined using the following relationship,

$$\sigma_{total} = \sqrt{\sigma_{hold}^2 + \sigma_{dffe}^2 + \sigma_{spl}^2 + 20\sigma_{jtl}^2} \quad (\Delta t < \mathrm{T}/2) \tag{3}$$

and

$$\sigma_{total} = \sqrt{\sigma_{setup}^2 + \sigma_{dffe}^2 + \sigma_{sple+}^2 20\sigma_{jtl}^2}, \quad (\Delta t > \mathrm{T}/2) \tag{4}$$

where σ_{total} is the combined timing fluctuation, $\sigma_{setup/hold}$ is standard deviation value of setup or hold time of the DFFE, σ_{DFFE} is the timing jitter of the DFFE output, σ_{spl} and σ_{jtl} are the timing jitter of splitter and Josephson transmission line, respectively. According to circuit simulation results, σ_{DFFE}, σ_{spl}, and σ_{jtl} at the standard bias voltage of 2.5 mV are 0.212 ps, 0.189 ps, and 0.077 ps/junction, respectively. The error rate (ER) of the 1-million-bit shift register can be approximately expressed as

$$ER(\Delta t) \approx 10^6 \cdot \left\{ 0.5 + 0.5 \cdot erf\left(\frac{\mu_{hold} - \Delta t}{\sqrt{2}\sigma_{total}} \right) \right\} \quad (\Delta \mathrm{t} < \mathrm{T}/2) \tag{5}$$

and

$$ER(\Delta t) = 10^6 \cdot \left\{ 0.5 + 0.5 \cdot erf\left(\frac{\Delta t - \mu_{setup}}{\sqrt{2}\sigma_{total}} \right) \right\}. \quad (\Delta t > T/2) \qquad (6)$$

We calculated the dependence of the error rate of the 1-million-bit shift register on the designed timing margin between the clock and data input for each DFFE assuming the 50 GHz operation. Fig. 5 shows a comparison of dependences of the error rate of 1 million-bit shift registers composed of various DFFE cells on designed timing margin. The calculated error rate characteristics, adjustment of not only timing margin but also the bias voltage is important for stable operation of the large-scale SFQ logic circuit.

4. Conclusion

We statistically analyzed the relationship between the timing margin for the SFQ logic gates and the error rate of the large-scale SFQ logic circuits by taking the timing jitter and the fluctuation of the setup and hold time of SFQ logic gate into account. It was observed that the fluctuation of the setup and hold time is more critical than the timing jitter for SFQ circuit operation. By using the extracted fluctuations of timing parameters of SFQ logic gates, we can calculate the error rate of large-scale SFQ logic circuits as a function of timing margin. By using the investigated quantitative error rate calculation, the guideline of timing design for large-scale SFQ circuits can be obtained.

Acknowledgement

This work was supported by JSPS KAKENHI Grant Number 26220904.

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Figure Captions

Fig. 1.

Fig. 2. (a) Input data pattern used in the analysis of DFFE; (b) Calculated dependences of output probability of the DFF on time different between clock (t_{clk}) and datum inputs (t_{din}). Dots and lines are calculated output probabilities and fitting curves, respectively. Each dot is calculated by 500 trials.

Fig. 3. (a) Input data pattern used in the analysis; (b) Calculated dependences of output probability of the DFF on time different between datum (t_{din}) and clock inputs (t_{clk}). Dots and lines are calculated output probabilities and fitting curves, respectively.

Fig. 4. (a) Block diagram of 1-million-bit shift register; (b) Definition of timing margin (Δt)

Fig. 5. Dependences of error rate of 1-million-bit shift register on timing margin Δt.

Table 1. Average (μ) and standard deviation (σ) values of setup/hold time of the DFFE

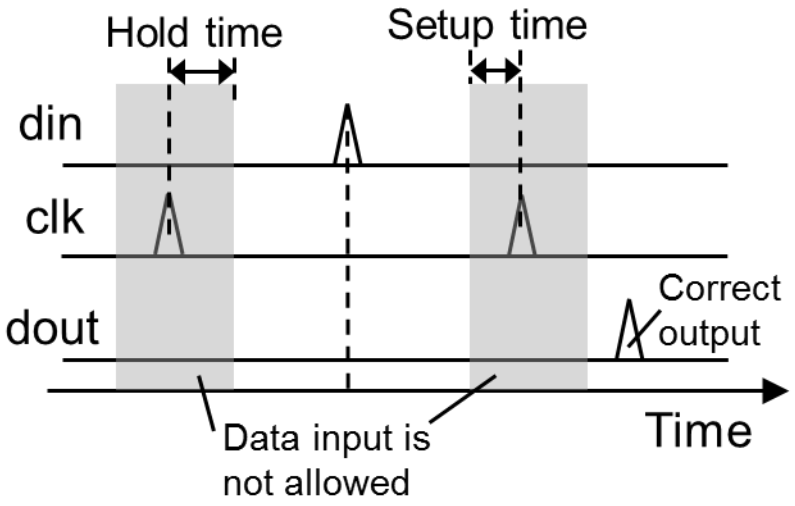
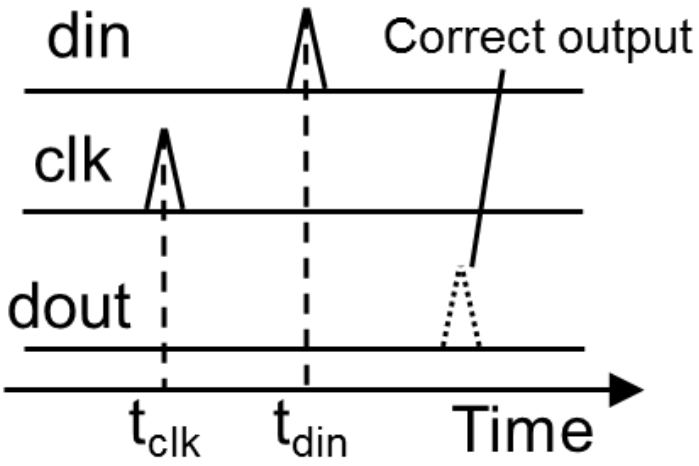
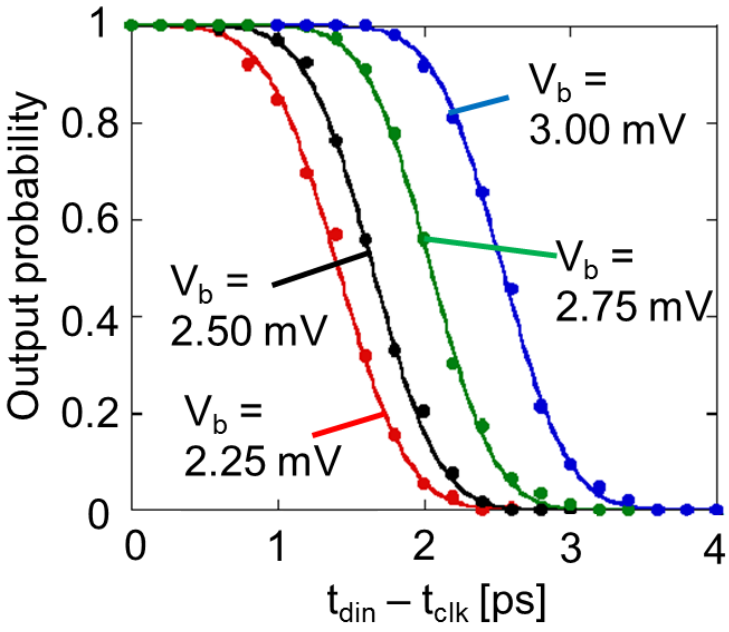

Hold time
Setup time
din
clk
dout
Correct
output
Data input is
not allowed
Time

Fig. 1

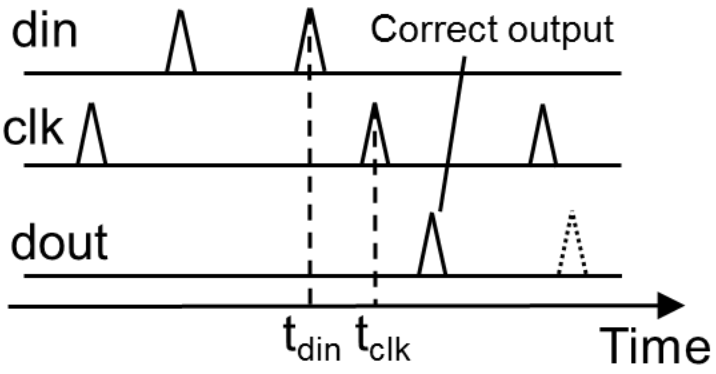

din
Correct output
clk
dout
t_{clk}
t_{din}
Time

(a)

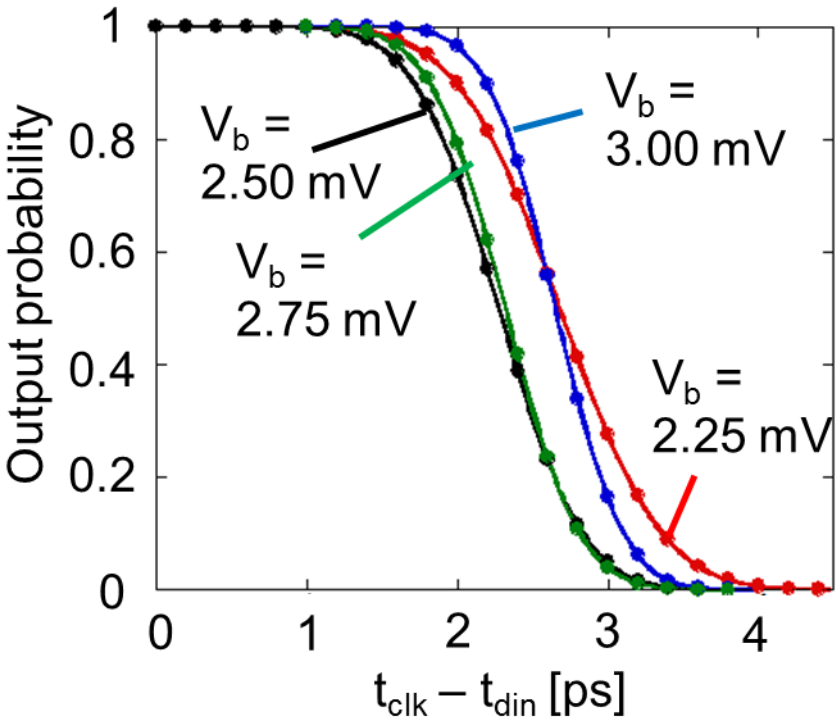

Output probability
1
0.8
0.6
0.4
0.2
0
0
1
2
3
4
$t_{din} - t_{clk}$ [ps]
V_b = 3.00 mV
V_b = 2.75 mV
V_b = 2.50 mV
V_b = 2.25 mV

(b)

Fig. 2

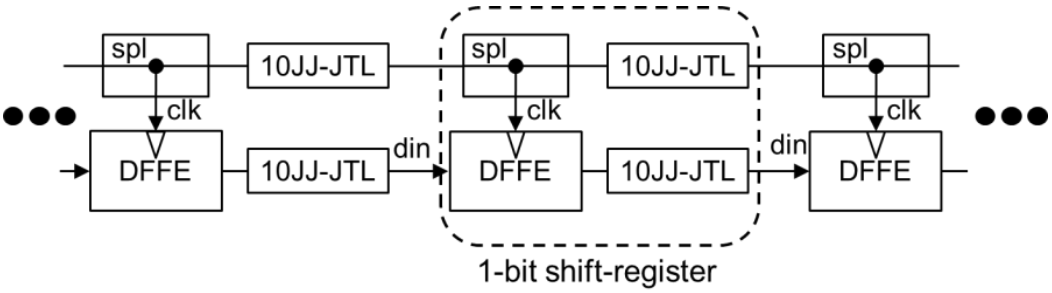

din
Correct output
clk
dout
t_{din} t_{clk}
Time

(a)

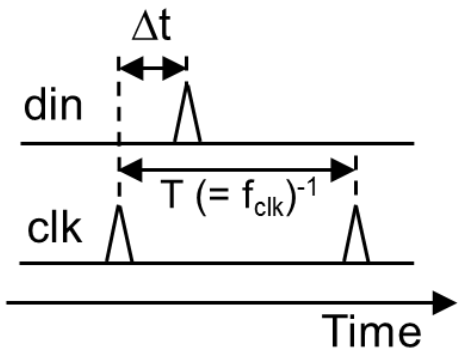

Output probability
1
0.8
0.6
0.4
0.2
0
0
1
2
3
4
$t_{clk} - t_{din}$ [ps]
V_b = 2.50 mV
V_b = 2.75 mV
V_b = 3.00 mV
V_b = 2.25 mV

(b)

Fig. 3


spl
10JJ-JTL
spl
10JJ-JTL
spl
clk
clk
clk
DFFE
10JJ-JTL
din
DFFE
10JJ-JTL
din
DFFE
1-bit shift-register

(a)


Δt
din
T (= f_clk)^-1
clk
Time

(b)

Fig. 4

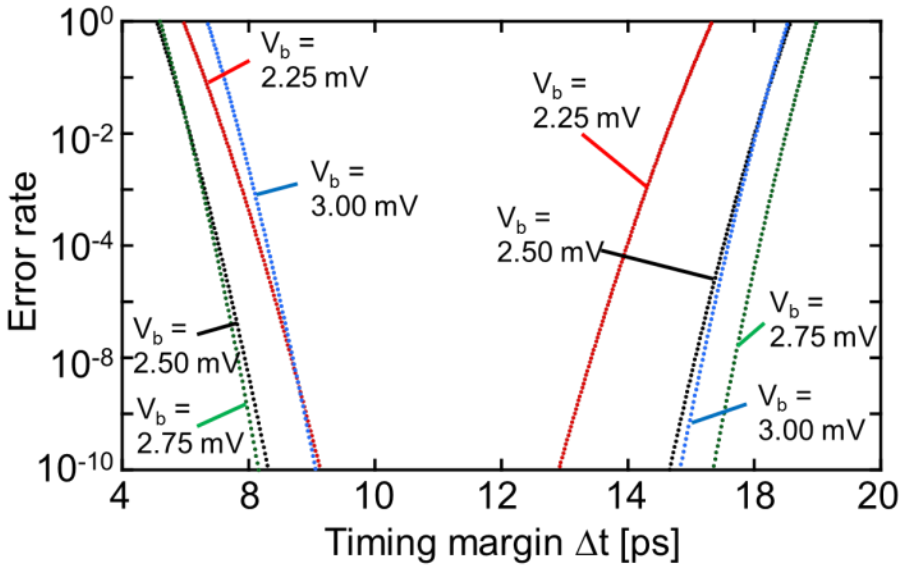

Error rate
Timing margin Δt [ps]
10^{0}
10^{-2}
10^{-4}
10^{-8}
10^{-10}
4
8
10
12
14
18
20
V_b = 2.25 mV
V_b = 3.00 mV
V_b = 2.50 mV
V_b = 2.75 mV
V_b = 2.25 mV
V_b = 2.50 mV
V_b = 2.75 mV
V_b = 3.00 mV

Fig. 5

Table 1

	V_b = 2.25 mV	V_b = 2.50 mV	V_b = 2.75 mV	V_b = 3.0 mV
μ_{hold} [ps]	1.410	1.649	2.044	2.533
σ_{hold} [ps]	0.379	0.354	0.348	0.358
μ_{setup} [ps]	2.683	2.277	2.320	2.653
σ_{setup} [ps]	0.535	0.438	0.390	0.357