Design Method of Single Flux Quantum Logic Circuits Using Dynamically Reconfigurable Logic Gates

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***Abstract*— In this study, we designed and tested dynamically reconfigurable AND/OR and NAND/NOR single flux quantum (SFQ) logic gates. The measured dc bias margins at low frequency were 99-126% and 121-144% for AND/OR and NAND/NOR gates, respectively. The experimentally confirmed maximum operating frequencies of the AND/OR and NAND/NOR gats were 36 GHz and 24 GHz, respectively. We investigated a circuit design method that enables the efficient design of SFQ logic circuits by using dynamically reconfigurable SFQ logic gates. The logic circuits were designed with a small number of gates using the input data pattern dependence of the Boolean function and reconfiguring the dynamically reconfigurable SFQ logic gates. As a case study, we designed and tested a bit-serial SFQ full adder using the investigated circuit design method. Compared with the conventional bit-serial SFQ full adder, the delay of the proposed full adder was reduced by 27%, assuming a clock frequency of 20 GHz. We confirmed correct operation of the adder with a low-speed test.**

***Index Terms*—Single flux quantum circuit, reconfigurable logic device, full adder.**

I. Introduction

RECONFIGURABLE logic devices such as a field-programmable gate array (FPGA) are used in a wide-range of applications because their circuit functions are reconfigured after circuit implementation to fit their purposes and requirements. In the field of superconducting single flux quantum (SFQ) circuits [1], reconfigurable logic devices have been studied [2]–[4]. Dynamically reconfigurable SFQ logic gates [5], whose logic functions are reconfigured by applying SFQ control signals, are believed to be suitable for high-throughput circuits that employ a deep pipeline because reconfiguration of the gates can be accomplished during circuit operation. The dynamically reconfigurable Josephson transmission line (JTL)/delay flip-flop (DFF) circuit has been demonstrated experimentally [5].

In this study, we designed and tested dynamically reconfigurable AND/OR and NAND/NOR SFQ gates, which are composed of a set of universal logic gates, to achieve a more flexible circuit design. Further, we also investigated a new design method of SFQ logic circuits using dynamically reconfigurable SFQ logic gates. In this design method, a simplified Boolean function is used to design the logic circuit by utilizing its data pattern dependence. By detecting the input data pattern and reconfiguring the logic functions of logic gates, we can efficiently design an SFQ logic circuit. We designed a bit-serial SFQ full adder as a case study. We evaluated the effectiveness of the new design method by comparing bit-serial SFQ full adders designed by the investigated and conventional design methods. We confirmed correct operation of the designed SFQ full adder with a low-speed test.

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II. Dynamically Reconfigurable SFQ Logic Gates

We designed the dynamically reconfigurable AND/OR gate on the basis of the circuit configuration proposed in [5]. The test circuit was implemented using the AIST 2.5 kA/cm^2 Nb standard process 2 (STP2) [6], [7]. Both low-speed and high-speed tests were performed by an on-chip test system [8]. Fig. 1 shows the low-speed test result of the dynamically reconfigurable AND/OR gate. The normalized dc bias margin obtained by the low-speed test was 99-126%. Fig. 2 shows a comparison of the dependences of the measured and simulated

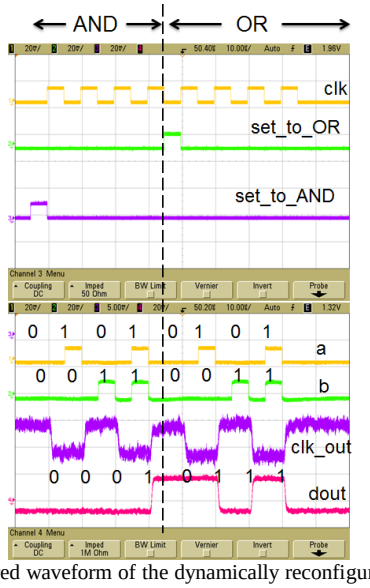

Fig. 1. Measured waveform of the dynamically reconfigurable AND/OR gate. The scale of the horizontal axis is 20 μs/div.

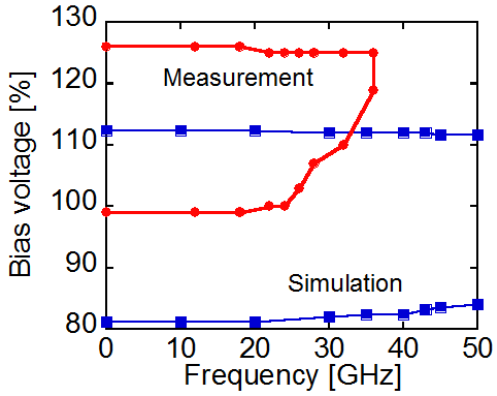

Fig. 2. Dependence of measured and simulated dc bias margins of the dynamically reconfigurable AND/OR gate on the operation frequency. The dc bias voltage is normalized by the designed value, 2.5 mV. The region surrounded by upper and lower lines corresponds to dc bias margin.

dc bias margins on the operation frequency. The bias voltage in Fig. 2 is normalized by 2.5 mV, which is the standard bias voltage in the cell library used in the study [9]. The measured bias margin shifted to a high bias region compared to the simulated result because of the higher critical current density of the Josephson junctions in the implemented circuit. The measured maximum operating frequency of the dynamically reconfigurable AND/OR gate was 36 GHz.

Further, we designed a dynamically reconfigurable NAND/NOR gate. This gate is thought to be useful because all logic circuits can be designed using a combination of NAND and NOR gates. Fig. 3 shows the equivalent circuit and parameters of the dynamically reconfigurable NAND/NOR gate. In the initial state, the circuit operates as a NAND gate by inputting the "clock" signal. The input "clock" is stored in a superconductive loop, which contains Josephson junctions J_8, J_7, and J_{11}. In this state, where no data are inputted from terminals "a" and "b," terminals, the J_{11} switches follow the "clock" input, and the SFQ signal is the output. When either inputs "a" or "b" is applied, the input signal is escaped by switching J_2 or J_4. When input "a" and "b" are applied, the input data induces switching of the Josephson junction J_7. As a result of switching J_7, the magnetic flux stored in the loop composed of J_8, J_7, and J_{11}, is escaped. In this state, no output is obtained when the "clock" is inputted.

After inputting the "set_to_NOR" signal, the circuit function is reconfigured to the NOR function. The flux quantum input from the "set_to_NOR" signal is stored in the loop consisting of J_{13}, J_{16}, and J_5. The initial bias current flowing in J_5 equivalently increases by the amount of circulating current induced by the stored flux quantum. In this state, one or both of the "a" and "b" inputs induce switching of J_5, and the inverse function is performed in the following part of the circuit. Therefore, the SFQ pulse is outputted only when

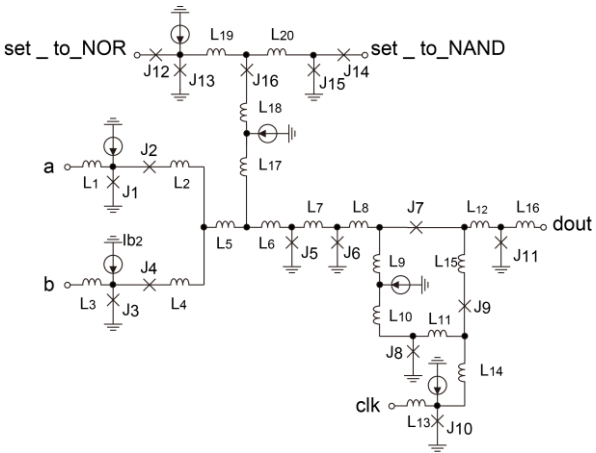

Fig. 3. Equivalent circuit of the dynamically reconfigurable NAND/NOR gate. Only the main part of the gate is shown. J_1 = 198 μA, J_2 = 110 μA, J_3 = 165 μA, J_4 = 115 μA, J_5 = 180 μA, J_6 = 120 μA, J_7 = 141 μA, J_8 = 100 μA, J_9 = 110 μA, J_{10} = 172 μA, J_{11} = 100 μA, J_{12} = 285 μA, J_{13} = 110 μA, J_{14} = 315 μA, J_{15} = 272 μA, L_1 = 2.97 pH, L_2 = 1.58 pH, L_3 = 2.02 pH, L_4 = 1.44 pH, L_5 = 0.38 pH, L_6 = 0.15 pH, L_7 = 3.69 pH, L_8 = 2.67 pH, L_9 = 6.05 pH, L_{10} = 0.13 pH, L_{11} = 2.32 pH, L_{12} = 0.14 pH, L_{13} = 3.02 pH, L_{14} = 0.38 pH, L_{15} = 1.84 pH, L_{16} = 6.84 pH, L_{17} = 0.71 pH, L_{18} = 0.22 pH, L_{19} = 3.90 pH, and L_{20} = 3.12 pH.

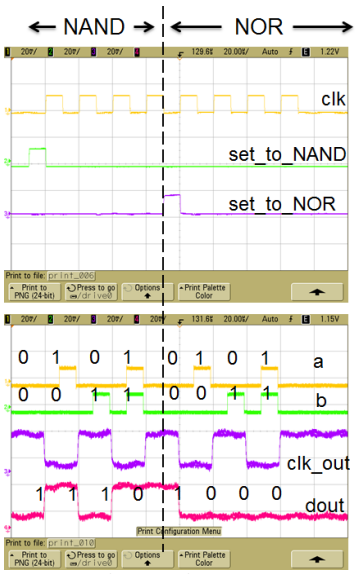

Fig. 4. Measured waveforms of the dynamically reconfigurable NAND/NOR gate. The scale of the horizontal axis is 20 μs/div.

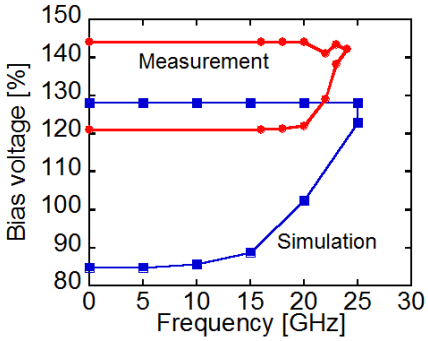

Fig. 5. Dependences of measured and simulated dc bias margins of the dynamically reconfigurable NAND/NOR gate on the operation frequency. The dc bias voltage is normalized by the designed value of 2.5 mV. The region surrounded by upper and lower lines corresponds to the dc bias margin.

zero is inputted to both inputs “a” and “b”.

We have designed and tested the dynamically reconfigurable NAND/NOR gate using the AIST STP2. Fig. 4 shows the measured waveform obtained from the low-speed test. The normalized measured dc bias margin at a low-frequency was 121-144%. Fig. 5 shows a comparison of the simulated and measured frequency dependences of the dc bias margin of the dynamically reconfigurable NAND/NOR gate. The measured maximum frequency of the dynamically reconfigurable AND/OR gate was 24 GHz.

Though the measured maximum operating frequency shows good agreement with the simulated result, the measured bias margin was narrower than the simulated result. This might be caused by the narrow parameter margin of the dynamically reconfigurable NAND/NOR gate. Because of the narrow margin, the measured dc bias margin was assumed to deteriorate because of the discrepancy between the designed and fabricated circuit parameters.

III. Design Method of Logic Circuits Using Dynamically Reconfigurable Logic Gates

We have investigated a circuit design method that enables us to design SFQ logic circuits efficiently by using the dynamically reconfigurable SFQ logic gates. In standard logic circuit design, the circuit is designed by placing and connecting logic gates on the basis of the Boolean function that represents the logic function of the circuit. The Boolean function of the logic circuit is generally overly complicated to process any input data patterns. This results in an increase in the number of logic gates and the circuit area and can be critical for implementation of large-scale SFQ logic circuits because the current integration level of SFQ circuit technology is much significantly lower than that of CMOS circuit technology.

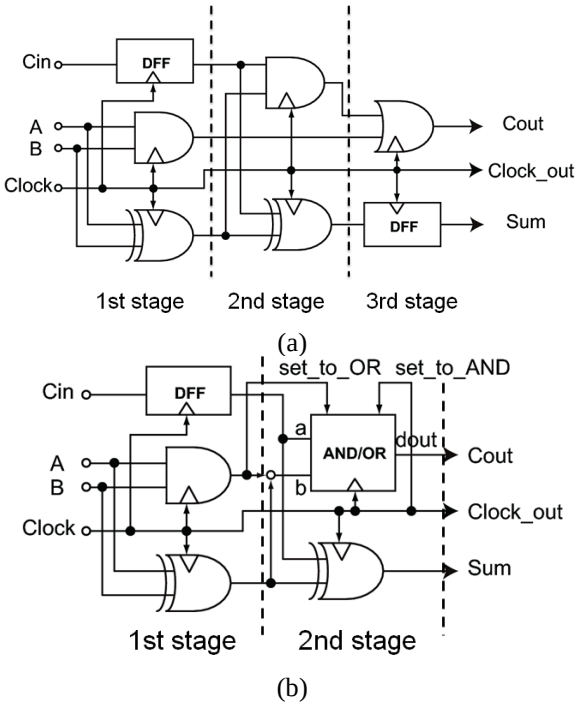

Fig. 6. Block diagrams of the (a) conventional SFQ full adder and (b) proposed SFQ full adder. In (a), a delay flip-flop (DFF) is inserted into the third stage to synchronize the two outputs, C_{out} and Sum.

However, the minimally required Boolean function depends on the input data patterns. If a specified input data pattern is provided, the Boolean function can be represented by a simplified function compared to a general form that can process all data patterns. By reconfiguring logic circuits using the dynamically reconfigurable SFQ logic gates according to input data, the logic circuit can be implemented with a small number of logic gates.

As a case study, we have designed a bit-serial full adder using the proposed SFQ logic circuit design method. The full adder, which calculates the addition of two input numbers taking the carry signal from the lower digit into account, is fundamental component of the arithmetic logic unit, and the SFQ full adder has been widely studied [10]–[14].

The general forms of the Boolean functions of summation (Sum) and the carry output (C_{out}) of the full adder are represented by

$$Sum = A \oplus B \oplus C_{in} \tag{1}$$

and

$$C_{out} = (A \cdot B) + (A \oplus B) \cdot C_{in}, \tag{2}$$

where A and B are input data and C_{in} is the carry signal input from a lower bit. The Boolean functions (1) and (2) can process all input patterns of A, B, and C_{in}.

The Boolean function of the carry output can be simplified by using its input pattern dependence. The Boolean function of the carry output can be simplified as

$$C_{out} = A \cdot B \cdot C_{in}, \quad \text{when} \quad (A,B)=(0,0), \tag{3}$$

$$C_{out} = (A \oplus B) \cdot C_{in}, \quad \text{when} \quad (A,B)=(0,1),(1,0), \tag{4}$$

and

$$C_{out} = A \cdot B + C_{in}, \quad \text{when} \quad (A,B)=(1,1). \tag{5}$$

When the input data pattern is (3) or (4), the carry out can be calculated by using XOR and AND gates as shown in (3) and (4). On the contrary, when both of the inputs data A and B are equal to one, the carry out is calculated not by the AND gate but by the OR gate, as shown in (5). Therefore, by using the dynamically reconfigurable AND/OR gate, the full adder can be designed.

Fig. 6 shows block diagrams of the conventional SFQ full adder and the SFQ full adder designed by the investigated design method. Both of the full adders employ concurrent-flow clocking for the high-speed operation [15]. The logic function of the dynamically reconfigurable AND/OR gate is reconfigured to OR when both of the A and B inputs are equal to one. In the conventional design, calculation of the carry out is performed by three clock stages that correspond to the

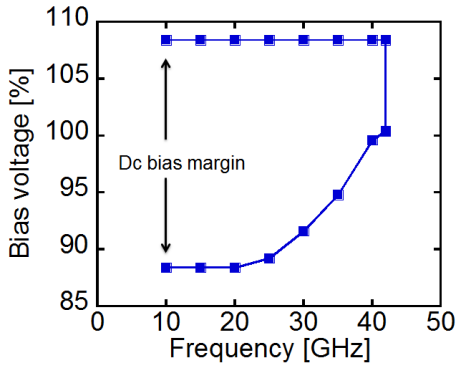

Fig. 7. Simulated clock frequency dependence of the dc bias margin of the proposed full adder

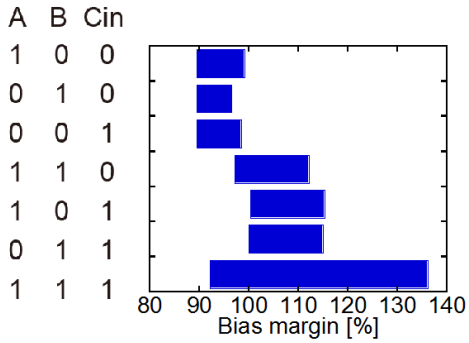

Fig. 8. Input data pattern dependence of the measured dc bias margin of the bit-serial SFQ full adder

maximum number of logic functions in (2). On the other hand, the carry out is calculated by two clock stages using the simplified Boolean function of (3), (4), and (5). Therefore, the full adder can be designed with two clock stages, as shown in Fig. 6 (b), by using a dynamically reconfigurable AND/OR gate. Because the number of clock stages of the newly designed full adder is reduced from 3 to 2 by introducing the new design method, the delay of the full adder is reduced from 193 to 140 ps compared to the conventional full adder when the clock frequency is 20 GHz. The total number of Josephson junctions of the full adder is also reduced from 236 to 224.

We have designed and tested the bit-serial SFQ full adder by introducing the investigated design method using the AIST STP2. Fig. 7 shows the simulated frequency dependence of the dc bias margin of the full adder. The simulated dc bias margin was 88-108%, and the maximum clock frequency was 40 GHz. We experimentally confirmed the correct operation of the full adder at a low clock frequency. Fig. 8 summarizes the input data dependence of the dc bias margin of the implemented full adder obtained by the low-speed test. Correct operation was confirmed for all patterns of input data. The measured dc bias margin was relatively wide for the input pattern of (A, B, C_{in}) = (1, 1, 1). In this input data pattern, both the "Sum" and "C_{out}" outputs were obtained. The circuit simulation results indicate that both of the dynamically reconfigurable AND/OR and XOR gates operate as simple transmission gates that propagate the clock input to the output ports independently of the input data pattern in the high-bias region. The measured wide dc bias margin is thought to be composed of the correct operation region and the operating region where this malfunction occurred.

IV. Conclusion

We designed and tested the dynamically reconfigurable AND/OR and NAND/NOR gates using the AIST 2.5-kA/cm^2 Nb STP2. We experimentally confirmed the correct operation of both gates at a clock frequency greater than 20 GHz. We investigated a circuit design method that enables us to design SFQ logic circuits efficiently by using the dynamically reconfigurable SFQ logic gates. As a case study, we designed a bit-serial full adder on the basis of the proposed SFQ logic circuit design method. The number of clock stages of the full adder was reduced compared to the conventional full adder. We confirmed low-speed operation of the implemented full adder.

Acknowledgment

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