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Design and Evaluation of Magnetic Field Tolerant Single Flux Quantum Circuits for Superconductive Sensing Systems

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SUMMARY A promising application of a single-flux quantum (SFQ) circuit is read-out circuitry for a multi-channel superconductive sensor array. In such applications, the SFQ read-out circuit is expected to operate outside a magnetic shield. We investigated an SFQ circuit structure, which is tolerant to an external magnetic field, using the AIST 2.5 kA/cm^2 Nb standard 2 process, which has four Nb wiring layers including the ground plane. By covering the entire circuit using an upper Nb wiring layer called the control (CTL) layer, the influences of the external magnetic field on the SFQ circuit operation can be avoided. We experimentally evaluated the sheet inductance of the wiring layer underneath the CTL shielding layer to design a magnetic-field-tolerant SFQ circuit. We implemented and measured test circuits comprising toggle flip-flops (TFFs) to evaluate their magnetic field tolerances. The operating margin and maximum operating frequency of the designed TFF did not deteriorate with increases in the magnetic field applied to the test circuit, whereas the operating margin of the conventional TFF was reduced by applying the magnetic field. We have also demonstrated the high-speed operation of the designed TFF operated in an unshielded environment at a frequency of up to 120 GHz with a wide operating margin.

key words: *SFQ circuit, cell library, sensor array, magnetic field tolerance*

1. Introduction

Superconducting sensing systems composed of a superconducting sensor array and single-flux quantum (SFQ) read-out circuits [1] have been proposed and implemented to build large-scale multi-channel superconductive sensor arrays [2]–[5]. By using the SFQ read-out circuit, the number of wires that connect the superconducting sensor array and room-temperature instruments can be reduced. This results in a reduction in noise and thermal inflow to the low-temperature environment, allowing the high performance of the sensor array to be fully utilized. The number of wires can be efficiently reduced further by employing a signal-multiplexing technique [6].

In superconducting sensing systems, the SFQ circuits are exposed to external magnetic fields such as the magnetic field of the earth and the bias magnetic field required for the operation of superconductive sensors. Therefore, the SFQ read-out circuits are expected to operate outside a magnetic shield to connect the superconducting sensor and the SFQ read-out circuit directly in the same temperature stage. Connecting the sensor chip and the SFQ chip in a magnetic shield using cables is one method of implementation of a superconductive sensing system. However, a large number of cables deteriorate the system performance because of the narrow bandwidth of the cable. By using the SFQ read-out circuits, the potential of the sensor array can be fully realized. Moreover, removing the expensive magnetic shields is helpful for reducing the implementation cost.

We investigated an SFQ circuit structure, which is tolerant to an external dc magnetic field for superconducting sensing systems using the AIST 2.5 kA/cm^2 Nb standard 2 process [7], which has four superconductive wiring layers, including the ground plane. The influences of the external magnetic fields on SFQ circuit operation and tolerance to the magnetic fields were experimentally evaluated.

2. Design of Magnetic-Field-Tolerant SFQ Circuits

Figure 1 shows a cross section of an SFQ circuit fabricated using the AIST 2.5 kA/cm^2 Nb standard 2 process. The circuit has four superconducting wiring layers called the ground plane (GP), BAS, COU, and control (CTL) layers. The thicknesses of each wiring layer are 400, 300, 400, and 500 nm, respectively. Josephson junctions (JJs) are implemented between the BAS and COU layers. We investigated a circuit structure shown in Fig. 1, where the active circuit contains JJs, which are completely shielded by the GP and CTL layers. This circuit structure has already been proposed to reduce the parasitic inductances of the SFQ circuits for stable operation [8].

To design the SFQ circuit, the extraction of inductance from the circuit layout is indispensable. In our cell library, the L-meter [9] is used for inductance extraction. However, the precision of the extracted inductance might be worse in the case that the wiring layer is sandwiched by two shielding layers. Therefore, we evaluated the sheet inductance of the COU layer that is mainly used as wiring in the SFQ circuit

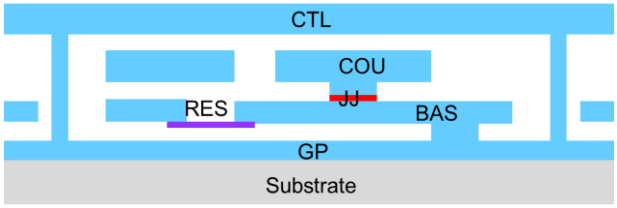

Fig. 1 Cross-sectional view of an SFQ integrated circuit fabricated using the AIST 2.5 kA/cm^2 Nb standard 2 process. The GP and the RES refer to ground plane and resistor layers, respectively. Each layer is not planarized in the actual circuit.

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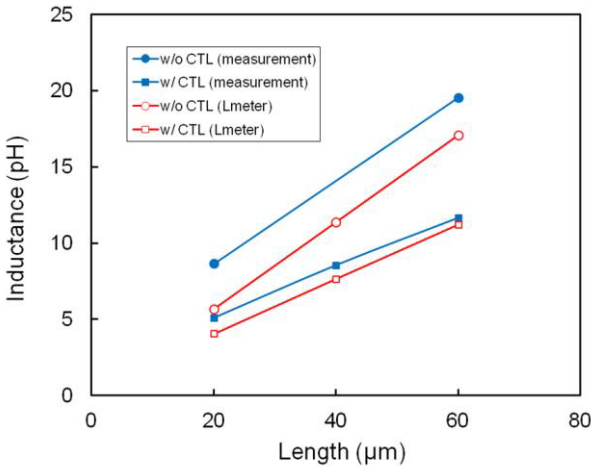

Fig. 2 Comparison of dependences of measured and extracted loop inductance layers on a COU wiring layer length with a width of 4 μm. The sheet inductance corresponds to the slope of the line.

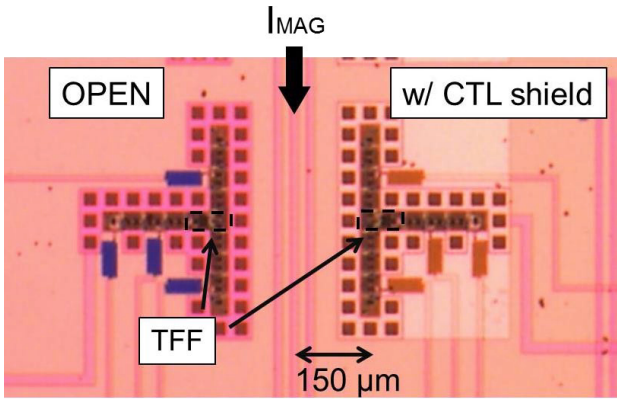

Fig. 3 Photograph of chip in the test circuit. Dc current (IMAG) is supplied to generate the magnetic field. The current supply line is a simple microstrip line with a width of 30 μm. The distance between the current supply line and TFFs is 150 μm.

underneath the CTL shielding layer by measuring the loop inductances of dc-SQUIDs. We measured three dc-SQUIDs, in which two JJs are connected by the COU layer that has the microstripline structure on the ground plane with lengths of 20, 40, and 60 μm, and a width of 4 μm, which is a typical line width of the COU wiring layer in our cell library.

Figure 2 shows the dependences of the loop inductance of dc-SQUIDs underneath the CTL shielding layer on the length of the COU layer. Figure 2 also shows the measured loop inductances of the dc-SQUIDs, without the CTL layer and the calculated inductance extracted from the circuit layout using the L-meter. The sheet inductance of the COU layer, which does not include the parasitic inductance of the dc-SQUID, can be calculated from the slopes of the lines in Fig. 2. The difference between the measured sheet inductance and the extracted sheet inductance by the L-meter is less than 10%, which is acceptable for the circuit design. Therefore, the inductances extracted by the L-meter were used to design the magnetic-field-tolerant SFQ circuits.

We have designed fundamental SFQ circuits, including a Josephson transmission line (JTL), a pulse splitter, a delay flip-flop (DFF), and a toggle flip-flop (TFF), with the CTL shielding layer. The circuit parameters were optimized to obtain wider dc bias and critical margins using the circuit parameter optimizer [10].

To build a large-scale SFQ circuit, the alignment and density of the ground holes called moats should be investigated carefully to avoid the influences of trapped flux quanta on the circuit operations [11]. However, the moat structure and density have not been investigated in this study because the circuit scale of the SFQ read-out circuit for sensing systems is relatively small compared to those of digital circuits.

3. Experimental

We have designed a test circuit to evaluate the external magnetic field tolerance of the designed SFQ circuits that have a CTL shielding layer. Figure 3 shows a microphotograph of the test circuit. In this test circuit, the magnetic-field-tolerant TFF is placed near a current supply line, and we can measure the magnetic field tolerance of the TFF by supplying a large dc current I_{MAG} to the current supply line. Two TFFs in the OPEN [12] and SUSHI [13] cell libraries that have no magnetic shield layer are also placed on the same chip and were measured for their magnetic field tolerances to compare the results.

First, we tested the TFFs, which have two output ports V_{out1} and V_{out2} inside double-layer μ-metal magnetic shields attached to the probe to evaluate the magnetic field tolerance quantitatively. We measured the dc bias margin and the maximum operating frequency of the TFFs as a function of the supplied dc current I_{MAG}. The bias margin was defined as the bias voltage when operation at frequencies higher than 100 GHz was obtained. The maximum operating frequency was measured using the average voltage method [14]. Because the TFF is a 1/2-frequency divider, the TFF operates correctly when the output average voltage is half of the input average voltage [15].

Figure 4 and Fig. 5 show the dependences of the bias margin and the maximum operating frequency of each TFF on the supplied dc current I_{MAG}. The maximum operating frequency of the TFF was measured by the maximum input average voltage [14]. The operating margin and maximum operating frequency of the TFF with the CTL shielding layer did not deteriorate with an increase in I_{MAG}, whereas the magnetic field strongly affected the operations of the TFFs in the OPEN and SUSHI cell libraries. We found that the SUSHI cell is more sensitive to a magnetic field compared with the OPEN cell. This is thought to be the case because all bias lines in a SUSHI cell are covered by superconducting layers, and the applied magnetic field is concentrated in the storage loops in the cell.

We also tested the TFFs outside the μ-metal magnetic shields. Figure 6 shows the experimentally obtained waveforms. The correct operation of the designed TFF with the CTL shielding layer was obtained, whereas the TFFs in

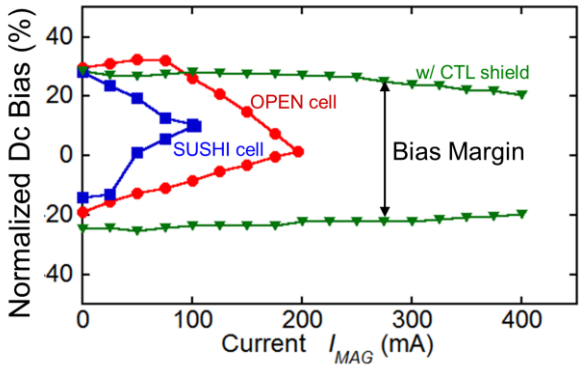

Fig. 4 Measured dependences of dc bias margins of each TFF on the supplied dc current I_{MAG}. Dc bias voltage is normalized by the designed value, 2.5 mV. The region between the upper and lower curves corresponds to the bias margin.

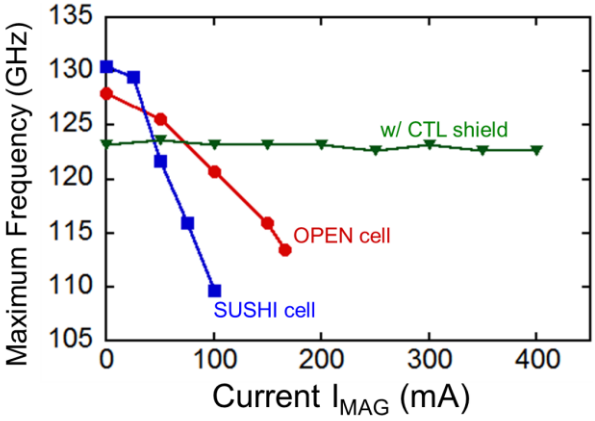

Fig. 5 Measured dependences of the maximum operating frequencies of each TFF on the supplied dc current I_{MAG}. According to the simple estimation, a magnetic field of 0.4 μT was applied to the storage loop of the TFF when a value of I_{MAG} of 100 mA was supplied.

the OPEN cell libraries did not work correctly. The measured maximum operating frequency of the designed TFF was 120 GHz.

Figure 7 shows the measured dc bias margins of newly designed and conventional TFFs. The measured dc bias margin of the TFF operating outside the magnetic shields was almost identical to one obtained inside the magnetic shields. The experimental results indicate that the investigated circuit structure has a magnetic field tolerance sufficient for high-speed operation in an unshielded environment.

4. Conclusion

We have investigated an SFQ circuit structure that is tolerant to external dc magnetic fields for superconductive multi-channel sensor array systems. By covering the circuit using an upper superconducting layer, we implemented magnetic-field-tolerant SFQ circuits. We evaluated the magnetic field tolerance of a TFF. The dc bias margin and the maximum operating frequency of the TFF did not deteri-

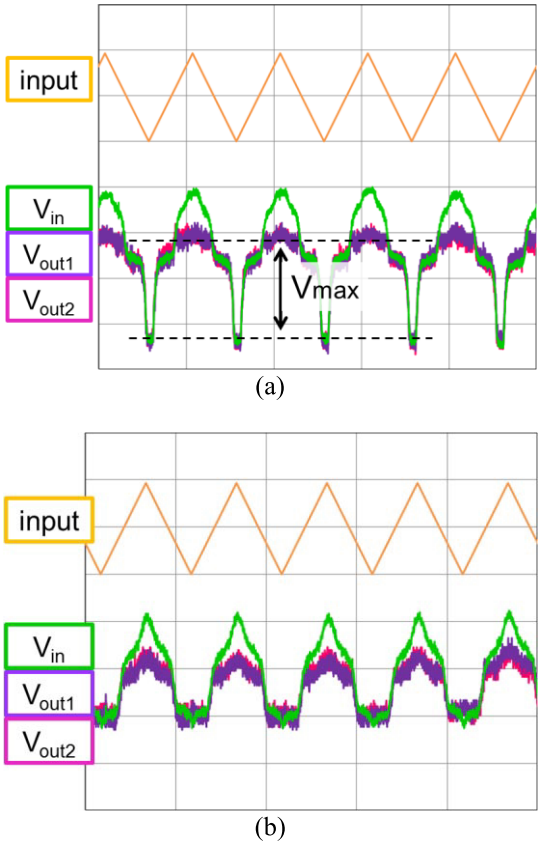

Fig. 6 Measured waveforms of (a) the newly designed magnetic-field-tolerant TFF and (b) the conventional TFF in the OPEN cell library. The circuits were measured outside the μ-metal magnetic shields. The conventional TFF output finite voltages to the input and output ports when no input current was injected. This means that the test circuit operated in the self-oscillating mode because of the reduction in the threshold current of the SQUID loops caused by the magnetic field. We concluded that correct operation of the conventional TFF was not observed. The scales are 500 μs/div. for the horizontal axis, 1 V/div. for the input, 10 mV/div. for V_{in}, and 5 mV/div. for V_{out1} and V_{out2}. V_{max} is the maximum input average voltage.

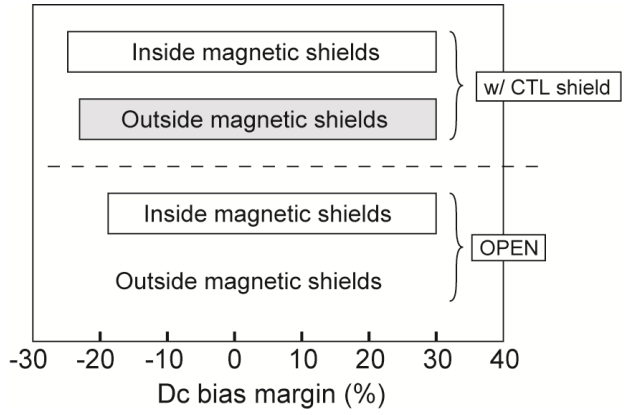

Fig. 7 Comparison of dc bias margins of the magnetic field tolerant TFF (w/ CTL shield) and the conventional TFF (OPEN). The dc bias margin is normalized by the designed bias voltage, 2.5 mV. The TFF in the OPEN cell library did not work correctly outside the μ-metal magnetic shields.

orate with an increase in the applied magnetic field to the circuit. The maximum operating frequency of the magnetic-field-tolerant TFF operated outside of the μ-metal magnetic shields was 120 GHz. The magnetic-field-tolerant read-out SFQ circuit, which can operate at a high clock frequency clock outside magnetic shields, can be built for superconducting sensor array systems using the investigated circuit structure.

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