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30 GHz Operation of Single-Flux-Quantum Arithmetic Logic Unit Implemented by Using Dynamically Reconfigurable Gates

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SUMMARY A single-flux-quantum (SFQ) arithmetic logic unit (ALU) was designed and tested to evaluate the effectiveness of introducing dynamically reconfigurable logic gates in the design of a superconducting logic circuit. We designed and tested a bit-serial SFQ ALU that can perform six arithmetic/logic functions by using a dynamically reconfigurable AND/OR gate. To ensure stable operation of the ALU, we improved the operating margin of the SFQ AND/OR gate by employing a partially shielded structure where the circuit is partially surrounded by under- and over-ground layers to reduce parasitic inductances. Owing to the introduction of the partially shielded structure, the operating margin of the dynamically reconfigurable AND/OR gate can be improved without increasing the circuit area. This ALU can be designed with a smaller circuit area compared with the conventional ALU by using the dynamically reconfigurable AND/OR gate. We implemented the SFQ ALU using the AIST 2.5 kA/cm^2 Nb standard process 2. We confirmed high-speed operation and correct reconfiguration of the SFQ ALU by a high-speed test. The measured maximum operation frequency was 30 GHz.

key words: *SFQ circuit, shielding, arithmetic logic unit, reconfigurable logic device*

1. Introduction

Superconducting single-flux-quantum (SFQ) circuits [1], [2] have been widely studied because of their unique and excellent characteristics: their low-power and high-speed operation. However, large-scale computing systems based on SFQ circuits have not been built so far. One of disadvantages of the SFQ circuit is its low integration level. Because the current fabrication process technology for the SFQ circuit is not mature compared to that of CMOS technology, the typical linewidth of the wiring of the SFQ circuit is 1–2 μm [3], [4]. Therefore, the circuit function density of the SFQ circuit per unit circuit area is still low. One method to improve the circuit function density of the SFQ circuit is building reconfigurable logic devices that enable us to perform multiple circuit functions by using a single circuit block.

We have been developing dynamically reconfigurable SFQ logic gates where the circuit function is reconfigured by control signal inputs [5]. The dynamically reconfigurable logic gates are suitable for high-speed reconfiguration of SFQ logic circuits compared to the other superconducting reconfigurable logic devices using phase shift elements [6], [7], and can be applied to deep pipelined digital circuits [8], [9]. We have investigated circuit design methodology using dynamically reconfigurable SFQ logic gates [10]. Because the characteristics of the superconducting circuits are easily modulated by applying the magnetic field of a bias current, the design methodology can be applied not only to SFQ logic circuits but also to other superconducting circuits such as the quantum flux parametron [11], [12].

The high-speed operation of the bit-serial adder designed by using dynamically reconfigurable SFQ logic gates has been demonstrated [10]. However, the measured operating margin of the bit serial adder was narrow because of the unstable operation of the dynamically reconfigurable SFQ AND/OR gate, the function of which is reconfigured to AND- and OR-modes by inputting control signals.

In this study, we improved the operating margin of the dynamically reconfigurable SFQ AND/OR gate by employing a new circuit structure where the circuit is partially surrounded by under- and over-ground layers [13], [14] to reduce the parasitic inductance of the signal lines. We designed and tested an arithmetic logic unit (ALU), which is one of the most important circuit components of computation systems, using the dynamically reconfigurable AND/OR gate to evaluate the effectiveness of introducing dynamically reconfigurable logic gates in superconducting logic circuit design.

2. Design of Arithmetic Logic Unit

Figure 1 shows the equivalent circuit of the dynamically re-

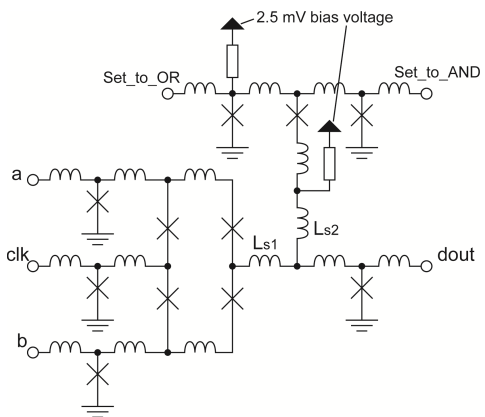

Fig. 1 Equivalent circuit of the dynamically reconfigurable AND/OR gate. The detailed circuit parameters are shown in [5].

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configurable AND/OR gate [5]. The simulated normalized dc bias margin of the conventional dynamically reconfigurable AND/OR gate was 81–112% [10]. The bias margin was limited by the parasitic inductance of the signal merging parts. In order to improve the margin and operating stability of the dynamically reconfigurable AND/OR gate, we investigated a new circuit structure that we called a partially shielded structure, where signal lines in the SFQ circuit are covered by under- and over-ground planes. We used the control (CTL) layer [3], which is the top wiring layer in the AIST 2.5 kA/cm^2 Nb standard process 2 (AIST-STP2), as the over-ground plane. A three-dimensional inductance extraction tool, InductEx [15], [16], was used to extract the inductances from the circuit layout. Figure 2(a) shows the mask layout of the dynamically reconfigurable SFQ AND/OR gate that is compatible with the CONNECT cell library [17]. Figure 2(b) shows an expanded view of the mask layout represented by the dashed square in Fig. 2(a). The over-ground plane, which is composed of the CTL layer, is electrically shorted to the ground plane using the stacked ground contacts. By introducing the partially shielded structure, the inductances of the merging part of the dynamically reconfigurable AND/OR gate represented by L_{s1} and L_{s2} in Fig. 1, which are a critical parameter for circuit operation, can be reduced from 0.733 pH to 0.426 pH and 0.735 pH to 0.426 pH, respectively. As a result, the simulated bias margin of the AND/OR gate is improved from 81–112% to 87–127% without increasing the circuit area. The cell size of the designed dynamically reconfigurable AND/OR gate is 80 × 120 μm, which is the same size as the conventional AND/OR gate.

Figure 3 shows a block diagram of the ALU we designed using the dynamically reconfigurable AND/OR gate. The ALU has six arithmetic/logic functions: addition (ADD), two subtraction (SUB1 and SUB2), AND, OR, and exclusive-OR (XOR) in three pipeline stages. The ALU is composed of a bit-serial adder designed by using the dynamically reconfigurable AND/OR gate [10], two exclusive-OR (EXOR) gates, and five nondestructive read-out (NDRO) gates for reconfiguration of the circuit functions. We can

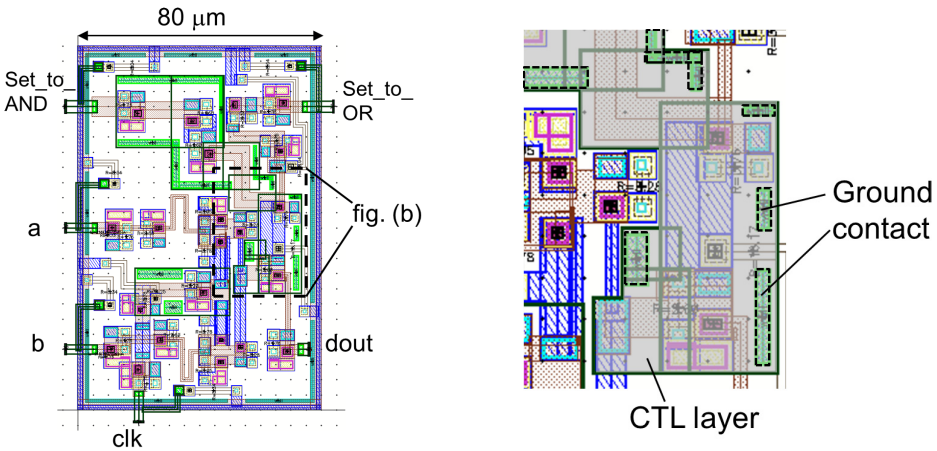


Fig. 2 (a) Mask layout of the dynamically reconfigurable AND/OR cell and (b) its expansion view of the layout represented by the dashed square in (a).

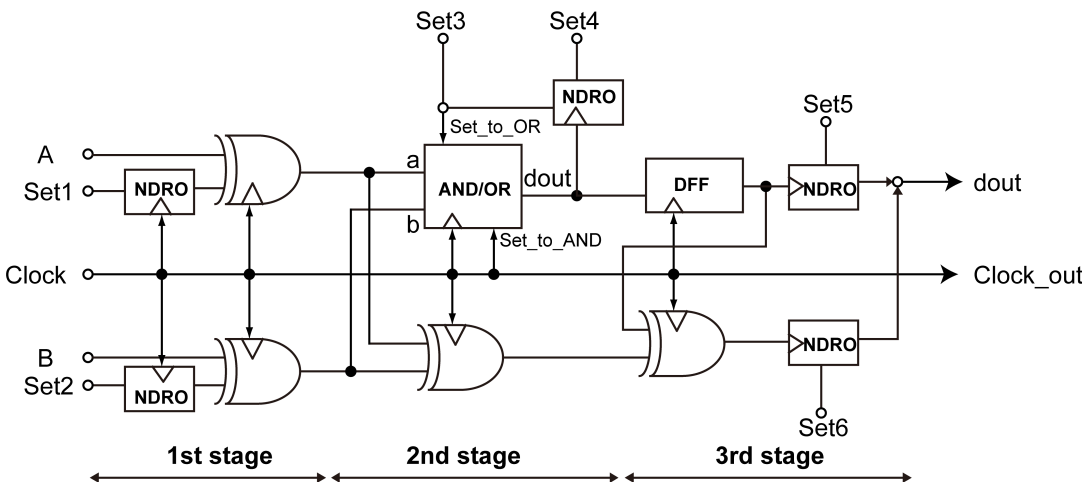


Fig. 3 Block diagram of the arithmetic logic unit designed by the using dynamically reconfigurable AND/OR gate. NDRO means the non-destructive read-out gate.

select the functionality of the ALU by inputting six control signals (Set1–Set6) that set internal states of the NDROs. Table 1 lists control signal inputs for each functions of the ALU. The ADD and SUB operations are performed by the bit serial adder in the ALU. AND and OR operations are performed by directly outputting the data outputs from the AND/OR gate. The EXOR operation is done by the EXOR gate in the third pipeline stage. When the function of the ALU is reconfigured, all NDRO gates are reset before inputting following reconfiguration signals. The number of pipeline stages is 3, which is the same as that of the conventional SFQ ALU [18].

We designed the ALU using the AIST-STP2. The total Josephson junction number and the circuit area of the designed ALU are 354 and 0.28×0.84 mm, respectively. By comparing this ALU's characteristics with those of a conventional ALU [18], the total Josephson junction number and the circuit area are reduced by 34% and 41%, respectively. The results indicate that the logic circuit design that uses the dynamically reconfigurable logic gates is suitable for a high-speed superconducting logic circuit.

Table 1 Control signal inputs for each function.

Function	Operation	Set1	Set1	Set3	Set4	Set5	Set6
ADD	A+B				1		1
SUB1	A-B		1		1		1
SUB2	B-A	1			1		1
AND	A&B				1	1	
OR	A|B			1	1	1	
XOR	A⊕B						1

3. Experimental

We tested the implemented ALU by taking low-speed and high-speed measurements. We confirmed five functionalities of the ALU and their reconfigurations by inputting appropriate control signals to the ALU. Although the OR operation was not confirmed by the incorrect wiring of the output signal, we confirmed correct high-speed operation of the AND/OR gate because ADD and SUB operations require reconfiguration of the function of the AND/OR gate. Figure 4 shows the function dependence of the measured dc bias mar-

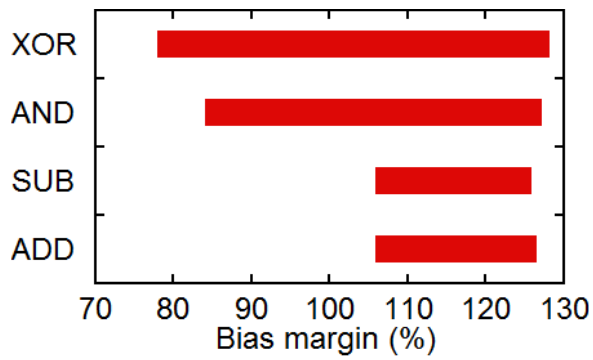
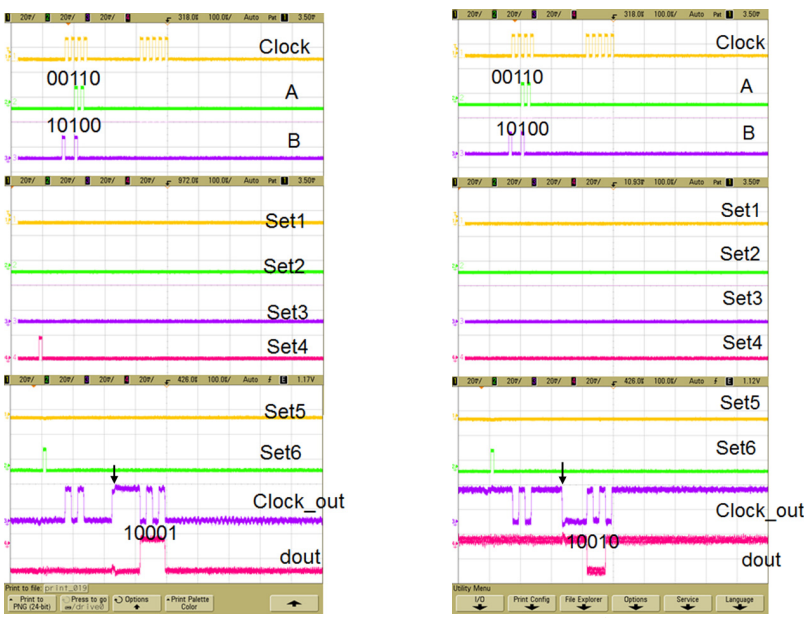


Fig. 4 Function dependence of the dc bias margin of the ALU measured at a low-frequency region. The margin of SUB1 and SUB2 are summarized as the one of SUB operation because the measured margins were the same. The bias margins are normalized by the designed bias voltage, 2.5 mV.



(a) (b)

Fig. 5 Measured waveforms of (a) ADD and (b) XOR operations of the ALU by the high-speed test. At the points represented by arrows, the clock generator is triggered and high-speed SFQ clock pulses are input to the ALU. Data are input and output from the least significant bit (LSB). In (a), correct data output $(10001)2 = (01100)2 + (00101)2$ is obtained. In (b), correct data output $(01001)2 = (01100)2 \oplus (00101)2$ is obtained.

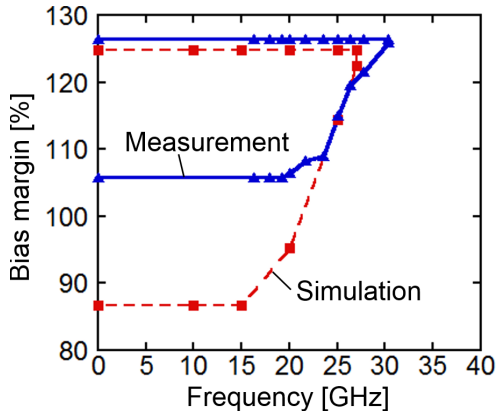


Fig. 6 Dependence of the bias margin of ADD operation of the ALU at the clock frequency. The bias margin is normalized by the designed bias voltage, 2.5 mV.

gin obtained by the low-speed test. The dc bias margins of ADD and SUB operations were narrower than those of AND and XOR operations because the timing error occurs in a feedback loop for the carry signal in the bit-serial adder.

We confirmed the correct operation of four functions of the ALU by using a high-speed test. Figure 5 shows examples of measured waveforms, where ADD and AND operations were correctly reconfigured by inputting appropriate control signals obtained by the high-speed tests. We measured the frequency dependence of the bias margin of ADD operation by using an on-chip high-speed test method [19]. Figure 6 shows a comparison of measured and simulated dependences of the dc bias margin of the ADD operation on the operation frequency. The measured maximum operating speed of the ALU was 30 GHz, which is higher than the simulated value. This discrepancy was thought to be caused by the critical current density of the Josephson junctions of the measured circuit being higher than the designed value.

4. Conclusion

We designed and measured an ALU with six arithmetic/logic functions by using dynamically reconfigurable AND/OR SFQ logic gates with improved operating margins. By introducing the dynamically reconfigurable AND/OR gate to the bit-serial adder in the ALU, the number of Josephson junctions and circuits in the ALU were reduced by 34% and 41%, respectively, compared with those of a conventionally designed ALU. This result shows the effectiveness of introducing dynamically reconfigurable logic gates in SFQ circuit design. We experimentally confirmed four functionalities of the ALU. The maximum operating frequency of the ALU was 30 GHz.

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