Doctoral Thesis

Proposal of Nonlinear Deadbeat Control for Boost Converter and the Experimental Verification

昇圧コンバータの非線形デッドビート制御の提案とその実験検証

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by

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Abstract

This thesis discusses the proposal of nonlinear deadbeat control for continuous conduction mode (CCM) boost converter and the experimental verification. First, the nonlinear state equation is derived, and second a nonlinear current reference deadbeat control is proposed. Third, a new nonlinear controller to implement the load disturbance compensation is proposed. Then the simulations using PSIM software and verifications by experiments, it is confirmed that under the conditions of an input voltage 12 V, an output voltage of 20 V, a load resistance of 4 Ω and a sampling frequency of 100 kHz, the voltage command tracking capability of a settling time of 280 μs is achieved, and an output voltage recovery time of 1.46 ms is achieved for a sudden unknown load change. Mathematical analysis is performed to confirm asymptotic stability and robustness of the control method during voltage and current perturbation, disturbance occurrence and parameter variations. It is found that the voltage and current errors eigen values converge towards inside of the unit circle thus maintaining asymptotic stability for each perturbation case investigated. Methods to design the controller parameters are stipulated to be within the physical realization and can be applied to boost converter of any application in CCM. The proposed control method is compared with other literature that applied different digital control methods to boost converters of various applications. It is found that nonlinear deadbeat control proposed in this thesis is about twice as fast for reference tracking response, and can reject disturbances quickly for a load current three times bigger than other literature. Therefore, it is concluded that these data are the best even though the proposed control is based on nonlinear equations. Few differences are observed between experiments and simulations. Further investigations reveal the cause to be time delay in the switching device and other unmodeled nonlinear switching device phenomena. Future work will focus on improving the control method to compensate for nonlinearities.

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I express deep gratitude to my family, for standing there for me, whenever I had to pull those long nights and long weekends, days, or months never at home, while undertaking this study.

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I dedicate this thesis to my family;

to my wife Getrude, my daughter Bethania Furaha, my son Bethani Faraji, my father Thadei, my mother Mary, ...

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Chapter 1

Introduction

1.1 Background

Popular applications of boost converters are in servo drive (e.g. rocket nozzle systems [28]), thermoelectric generators [27], switch mode power supplies, hybrid and pure electric vehicles [29], high power fuel cell electric vehicles [58] and others. These converters provide the interface between the unregulated DC grid and load which require higher regulated DC voltage, oftentimes designed to reduce losses at high power applications. [44]

However due to their discrete nonlinear nature stemming from the switching action, these converters are known to have unstable zero in the plant which makes difficult to achieve higher controller performance. [1,9] Because of this nature of the boost converter, in this thesis author will explore new control approaches based on nonlinear modeling. Systematic analysis and derivations will be carried out. The developed theories will be validated via simulations and experiments. This process will involve developing the nonlinear discrete time model for the converter and use of that modeling to develop nonlinear deadbeat controller (NDB). The NDB has been adopted because of its inherent features, some of which are fast transient response because of the deadbeat control and the capturing of converter nonlinear characteristics through discrete time model.

Two deadbeat control algorithms are developed - voltage mode deadbeat control (vNDB) and current mode deadbeat control (cNDB). However preliminary findings shows limitations of the vNDB thus its discussion is very short in this thesis. However, greater emphasis is placed on cNDB because of its attractive features and it has been investigated in detail because it is the major contribution of this thesis to the body of knowledge.

1.2 Motivations

Boost converters which are applied to servo systems are required to have fast reference tracking response and robustness against disturbances and parameter variations. However the unstable right-half-plane (RHP) zero limits higher performance control [31], causing slow response. The controller bandwidth can be improved by appropriately selecting the off time of the switch with a discrete time implementation. [42] However, this technology is applied to small signal modeling of the boost converter. Chen et al. [18] and Mushi et al. [1] presented control algorithms which showed voltage command tracking responses of few milliseconds. The responses were deemed slow and attributed to the presence of the RHP zero. The RHP zero causes negative output voltage response at first after command change and then the voltage follows and tracks the voltage command thus causing the slow response. Bao et al. [3] presented adaptive feedforward compensation for voltage source disturbance rejection. Sun et al. [2] implemented active disturbance rejection control algorithm to compensate highly nonlinear disturbances of a converter. However, Bao et al. [3], Sun et al. [2] and Hohmuth et al. [41] control methods do not account for voltage command change. Karamanakos et al. [22] proposed direct model predictive current control (MPC) strategy for boost converters, and reported fast current regulation with the results that voltage transient was 3.5 ms. However that MPC approach suffer high computational complexity as evinced in [36].

Above discussed literature and what is found in Literature review in Chapter 2 enabled the author of this thesis to identify that control methods applied to boost converters produce responses which are categorized below.

- Fast response: the algorithm performs well in tracking command change, but performs poorly when disturbance occurs in the system.
- Robust to disturbances: the algorithm performs well in rejecting disturbances, but performs poorly when voltage command changes.
- Slightly fast response to voltage command change and robust to disturbance inputs: the algorithm gives moderate response to voltage command tracking as well as rejecting disturbances.

Lack of control method that is superior in both reference command tracking and disturbance

rejection formed basis motivation for this study. Further on, it was noted that reported literature considered converters with small loading current ranging about few milliamps. E.g. 0.67 A [6], 0.2 A [7], 0.05 A [8] to mention few references. These mentioned reasons motivated author to undertake this study for the boost converter and develop a nonlinear deadbeat controller that is superior in both command tracking and disturbance rejection transient response and higher load current capability.

1.3 Research Objectives

Motivations and technology gaps were identified previously in Section 1.2, which pointed out the need to undertake this study. Therefore this paper will address the following objectives in order contribute to the technology of DC-DC converter control:

- Propose a nonlinear discrete state equation of the boost converter. This model is useful for digital control design and implementation.
- Develop a nonlinear reference current deadbeat control based on the modeling above. This control is expected to have fast and short transient response times.
- Propose a reference current which comprises of two terms. The first one is for output voltage error regulation, and the second is steady state inductance current control.
- Implement load current and disturbance observer and use these estimated load current and disturbance signals to cancel any unknown disturbance inputs into the system.
- Implement simulations and experiments to verify the developed control system.
- Discuss stability of the system under the developed control law and prove that the system is robust against parameter variations.
- Discuss how the performance of the proposed system compares with other literature with regards to performance indices:– settling time and recovery time.

1.4 Thesis Outline

The organization of this thesis can be described as follows. Chapter 1 covers the Introduction which describes the study background, motivations and research objectives. Extensive Litera-

ture Review has been presented in Chapter 2 and a clear explanation of performance indices is explained therein. Chapter 3 presents Research Methodologies by explaining the modeling, simulation and experiment procedures. Chapter 4 presents Voltage Mode Control Simulation and Experiment Results and related brief discussions. Chapter 5 presents Current Mode Control Simulation and Experiment Results and related discussions. Chapter 6 discusses the Nonlinear Phenomena and Stability Analysis of the current mode nonlinear deadbeat control. Chapter 7 discusses the thesis Conclusions – contributions and future research work. List of Published Papers is included in Appendix A. Some Mathematical Derivations and theories are presented in the Appendix B.

Chapter 2

Literature Review

This chapter presents the previous state of the art digital control methods applied for boost converters and the expected performance characteristics or indices. Digital control advantages such as system reliability, reduced controller design time, programmability, and possibility to include various performance enhancements have been discussed widely [21,45–47,49,53] including sensorless control [55], this Section highlights the superiority of deadbeat current mode control over voltage mode control.

2.1 Desired Performance Indices

We start this discussion by defining the desired performance indices for the boost converter responses for voltage command tracking and disturbance rejection. They are: settling time t_s and recovery time t_{rec} defined below and presented as desired transient characteristics of Fig. 2.1.

Settling time (t_s) is the time taken for the output voltage to rise from 0% and settle within 90% of command voltage exemplified in Fig. 2.1(a). Aim of control engineers is to realize the quick and short settling time with small (or no) overshoot shown by the pink curve, instead of the unimproved response of blue curve.

Recovery time (t_{rec}) is the period for the voltage dip (decrease due to disturbance input) to recover back to 90% of command voltage exemplified in Fig. 2.1(b). It is desired to have a quick recovery time [55] with small voltage dip shown by the pink curve, which is an improvement over the blue curve response.

In Fig. 2.1 $v_O(t)$ is the output voltage and $i_d(t)$ is the disturbance current, while t_s and t_{rec} take the definitions above. Control methods applied to boost converter are of two types,

namely:– voltage mode control and current mode control which are discussed next.

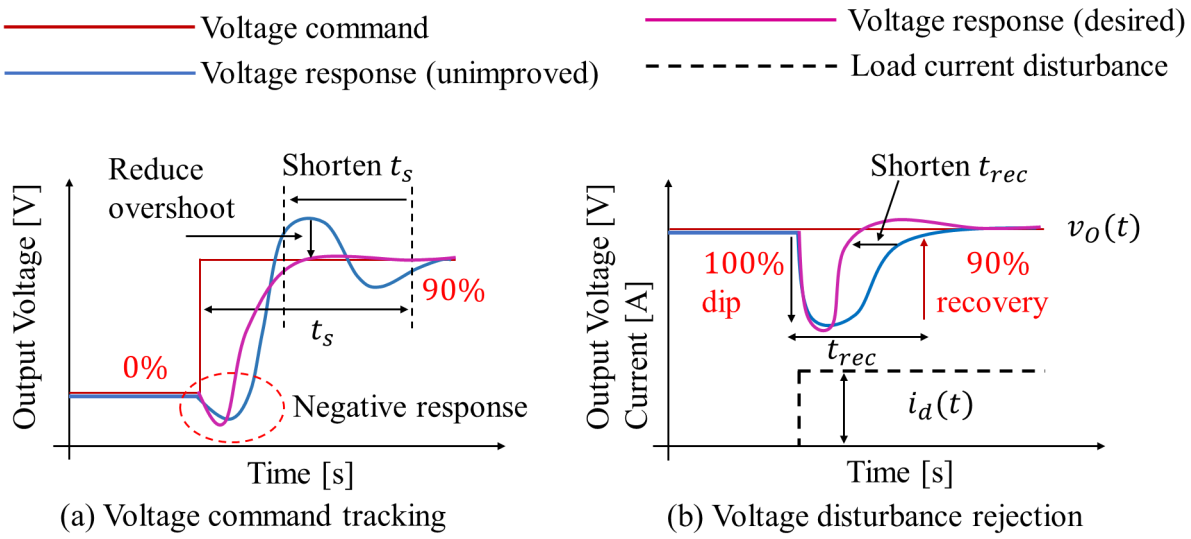


Figure 2.1: Desired transient characteristics of boost converter output voltage response.

2.2 Voltage Mode Control

Kazimierczuk [4] explains that voltage mode control involves direct control of output voltage by manipulating the duty cycle via a negative feedback. Disadvantages of this control mode is due to the presence of the RHP zero on the small signal transfer function from duty cycle to the output voltage for the case of boost converter. [14, 54, 59] This RHP makes the controller less robust and slow because of limited bandwidth.

We discuss the applications of voltage mode control and their performance characteristics in the following. Karamanakos et al. [15] proposed a direct voltage control of DC–DC boost converter using enumeration–based model predictive control. The voltage regulation is achieved by the model predictive controller (MPC) and load disturbance is estimated by state estimator. Under voltage input variation 10 V to 15 V, output voltage variation 15 V to 30 V, 1.9 ms settling time was achieved together with 0.5 ms recovery time for load disturbance 73 Ω to 36.5 Ω. Mushi et al. [9] proposed a nonlinear deadbeat control for boost converter and directly controlled the voltage output. Under simulation of input voltage 12 V, output voltage ramp variation 20 V to 21 V, settling time 0.1 ms was achieved but with a large steady state error. That research did not mention about load disturbance. Shirazi et al. [17] implemented an

autotuning digital controller for DC–DC power converters based on online frequency–response measurements. Under input voltage 15 V, output voltage variation 30 V to 35 V, 0.8 ms settling time was achieved and 0.6 ms recovery time under load variation 0.3 A to 0.6 A was achieved. We note that mentioned research works supplied very small load currents which works very well with voltage mode control. However, for larger load currents, the voltage mode control is susceptible to control saturation [61], therefore a superior control is required. Luckily, current mode control has been investigated and proved to be reliable with higher capability. In next section we will discuss the characteristics of current mode control.

2.3 Current Mode Control

Erickson et al. [5] explains that current mode control (also known as current programmed control) uses inductance current to indirectly control the output voltage. Its several advantages are – simpler dynamics because the small signal transfer function from control current to output voltage contain one less pole than the small signal transfer function from duty cycle to output voltage. Also with this control it is possible to achieve robust wide–bandwidth control of the output voltage because it moves the RHP zero to higher frequency close to the converter switching frequency.

Based on its advantages there has been extensive efforts to develop current mode control methods for boost converters to mention but few previous works. [1,11–13,16,18,20,23,25,26,30] This control type has proven to be the most fast and robust because the control engineer does not worry about the complications brought about with voltage mode control.

Chen et al. [23] derived predictive digital current programmed control for DC–DC converters but never presented the output voltage regulation results. Chen et al. [18] proposed closed–loop analysis and cascade control of a nonminimum phase boost converter with two loops: – fast inner current loop using sliding mode control and slow outer voltage loop using a proportional integral (PI) control. Under input voltage 20 V, output voltage variation 35 V to 40 V a 10 ms settling time was presented. This control handled load variation 40 Ω to 30 Ω with 10 ms recovery time. Flores et al. [12] proposed a robust nonlinear control of a boost converter via algebraic online parameter identification. With this highly complex algorithm, under unknown input voltage and unknown load, the 3 ms settling time was confirmed and the recovery time was difficult to be ascertained from the presented figures. Mushi et al. [1] made a proposal

for faster disturbance rejection of boost DC–DC converter based on simplified current minor loop. Under input voltage 12 V, output voltage variation 20 V to 21 V, 5 ms settling time was presented and a load variation 2 A to 2.5 A resulted to recovery time of 17 ms. Mentioned researches presented too long recovery times.

Oettmeier et al. [16] reported MPC of switching in a boost converter using a hybrid state model with a sliding mode observer (SMO). The optimal switching and SMO applied to boost converter under input voltage 115 V, output voltage variation 165 V to 175 V resulted settling time 1.7 ms. However no load variation recovery time was reported. Oucheriah et al. [13] reported a PWM–based adaptive sliding–mode control for boost DC–DC converters. The voltage error integration was not added to the voltage error regulation because the steady–error was very small. Under input voltage variation 6 V to 10 V output voltage was controlled at 12 V. When output voltage changed 7 V to 12 V a settling time 25 ms was reported. When load varied 160 Ω to 40 Ω resulted into a recovery time 20 ms. Takei et al. [19] reported a load current feed forward control of boost converter for downsizing output filter capacitor. Under input voltage 50 V, output voltage 100 V, load variation 3 A to 8 A, a 5 ms recovery time was reported, however no mention of output voltage variation is made. Tong et al. [20] reported a sensorless predictive peak current control for boost converter using comprehensive compensation strategy which used a first order current observer. Under output voltage 15 V, load variation 15 Ω to 10 Ω, a 0.18 ms recovery time was reported. However no mention of voltage command tracking is made.

Wai et al. [11] proposed a design of voltage tracking control for DC–DC boost converter via total sliding–mode technique in the sense of Lyapunov stability theorem. The controlled system was observed to have total sliding motion without a reaching phase. Output voltage changed from 0 V to 200 V achieving a settling time of 1000 ms. However load variation 80 Ω to 50 Ω, the recovery time could not be ascertained from the article's presented figures.

Those mentioned previous literature pointed out the deficiencies which need to be addressed, namely – control systems result into either fast response and susceptible to disturbances; robust to disturbances and not fast response; or both slightly fast and robust which is the knowledge and technological gap existing in those previous literature. The author will address these challenges as objectives in this thesis and thus contributing to the knowledge and technology of DC-DC boost converter control.

2.4 Deadbeat Control Advantages

Let's review deadbeat control algorithms applied to either boost converter or buck converter or others by pointing out its merits. Bibian et al. [25] proposed a high performance predictive deadbeat digital controller for DC power supplies and verified the control on buck converter. The inductor current could track the reference in single control period. Lai et al. [26] reported a predictive digital–controlled converter with peak current–mode control and leading–edge modulation for a buck converter. Authors of that paper confirmed that the digital control produced same transient ripple as the analog controller, but with a slightly longer settling time. Mizushima et al. [10] reported a development of DC–DC converter for high/low voltage output using deadbeat control for a buck converter used for plasma applications with very fast output voltage tracking response. Wen et al. [30] reported a DC–DC converter with digital adaptive slope control in auxiliary phase for optimal transient response. The control method improved efficiency of the buck converter by achieving 2% heavy–load and 10% light–load efficiency improvement. Qiu et al. [39] proposed sensorless digital average current mode control of PWM three types of DC-DC converters – buck, boost and buck-boost. This technology was validated on the boost converter by achieving reference inductor current tracking in two switching periods.

Deadbeat control has been extensively applied to inverters [32,33,48,56], rectifiers and active filters [57] and buck converters [10] since the deadbeat controller places all the poles of the closed loop system at the origin thus ensuring fast transient response.

2.5 Summary of Chapter Two

We have discussed the desired performance indices and two types of control methods - voltage mode and current mode control. We have established the utility of digital (deadbeat) control for converters which results in stability like in [49, 51, 52], to fast response [53] and robust to disturbances like in [37,50] In next Chapter, we will develop nonlinear deadbeat control by using discrete time modeling of boost converter.

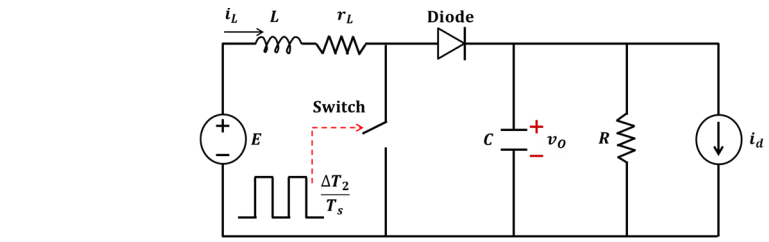
Chapter 3

Research Methodologies

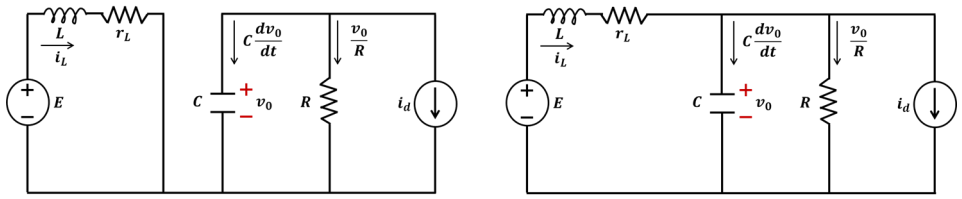
This chapter presents research methodologies employed to study and investigate the outlined objectives in Section 1.3 of Chapter 1. The research methodologies include – the modeling strategies, simulation procedures and experiment processes. For purposes of this thesis Fig. 3.1(a) - (c) represent equivalent circuits of boost converter in different operating modes. We assume at all times that the converter will operate in continuous conduction mode (CCM). In the figure E stands for input unregulated DC voltage, i_L represents current through inductor. L and r_L represent the inductance and inductor ESR respectively. Output filter is made up of capacitor C and load resistor R which is connected in parallel to the load disturbance current i_d. Advantages of separating the disturbance current i_d from the known load R is to facilitate implementation of load and disturbance observer to be discussed later. Output voltage is represented by v_O which is the parameter to be controlled. Therefore Fig. 3.1(a) represents simplified equivalent boost converter circuit. Switch ON and OFF states (in which ΔT_2 is the PWM off time duration) are presented in Fig. 3.1(b) and (c) during CCM. The i_L, v_O, and i_d are continuous/discrete time varying variables as will be shown later. We will use circuits of Fig. 3.1 and waveforms of Fig. 3.2 to develop the discrete time model and the continuous time model of the boost converter necessary for our proposed controller design.

3.1 Sampled Data Model of Boost Converter

Figure 3.2 shows waveforms of the boost converter under digital control. The first figure represents PWM wave pulses, the second figure represents the output voltage waveforms and third figure represents inductance current waveforms. Black curves presents the actual continuous time waveforms, while the red curves presents the sampled waveforms at time instant k. The



(a) Boost converter equivalent circuit



(b) During switch ON

(c) During switch OFF

Figure 3.1: Boost converter (a) equivalent circuit, (b) switch ON state, (c) switch OFF state.

variables displayed are $\Delta T_1[k]$ and $\Delta T_2[k]$ as the ON and OFF duration of the converter's switch. The sampling period is similar to switching period and given by $T_s = \Delta T_1[k] + \Delta T_2[k]$. The k within the brackets means the discrete time index. The $v_O[k]$, $i_L[k]$, and $\Delta T_2[k]$ represent the sampled voltage, sampled inductance current, and PWM duty ratio at discrete time instant k. The PWM duty $\Delta T_2[k]$ is placed at the center of the sampling period while all signals are sampled at the start of each sampling period. Since different sampling instant produces different controller's frequency response. [42] The converter's states when ON and OFF are assumed to be those in Figs. 3.1(b) and (c). We start by denoting the state vector as $x(t)$, state transition matrices as A_i, $i = 1, 2, 3$, control distribution matrices as B_i, $i = 1, 2, 3$, disturbance distribution matrices as W_i, $i = 1, 2, 3$, and disturbance as $d(t)$. For the three instants within the

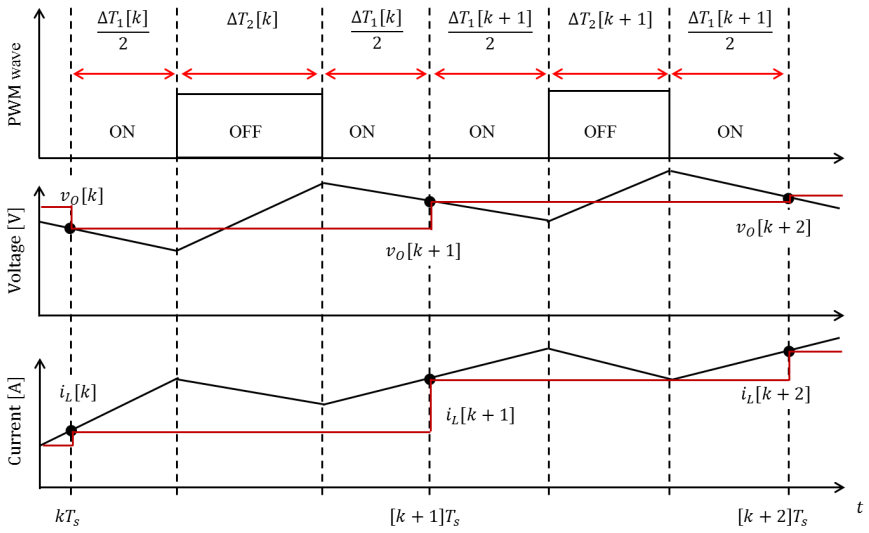


Figure 3.2: Boost converter waveforms for digital control: actual (black) and sampled (red).

sampling periods of Fig. 3.2, one gets the following dynamic equations:

$$\text{ON: } \dot{x}(t) = A_1 x(t) + B_1 x(t)\Delta T_2(t) + W_1 d(t), \quad kT_s \le t < \frac{\Delta T_1[k]}{2} \tag{3.1}$$

$$\text{OFF: } \dot{x}(t) = A_2 x(t) + B_2 x(t)\Delta T_2(t) + W_2 d(t), \quad \frac{\Delta T_1[k]}{2} \le t < \frac{\Delta T_1[k]}{2} + \Delta T_2[k] \tag{3.2}$$

$$\text{ON: } \dot{x}(t) = A_1 x(t) + B_1 x(t)\Delta T_2(t) + W_1 d(t), \quad \frac{\Delta T_1[k]}{2} + \Delta T_2[k] \le t < (k+1)T_s \tag{3.3}$$

$$x(t) = [i_L(t) \;\; v_O(t)]^T, \quad A_1 = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}, \; A_2 = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \tag{3.4}$$

$$B_1 = B_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix}, W_1 = W_2 = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}, \quad d(t) = [E \;\; i_d(t)]^T \tag{3.5}$$

Thus after short calculations using Euler's formula, following sampled data model of the boost converter is obtained. [9]

$$v_O[k+1] = \left(1 - \frac{T_s}{RC}\right) v_O[k] + \frac{1}{C} i_L[k]\Delta T_2[k] - \frac{T_s}{C} i_d[k] \tag{3.6}$$

$$i_L[k+1] = \left(1 - \frac{r_L}{L} T_s\right) i_L[k] - \frac{1}{L} v_O[k]\Delta T_2[k] + \frac{T_s}{L} E \tag{3.7}$$

These equations show strong bilinear nonlinearity of $i_L[k]\Delta T_2[k]$ in (3.6) and $v_O[k]\Delta T_2[k]$ in (3.7). From the nonlinear discrete model of the boost converter (3.6)-(3.7), author proposes two types of nonlinear deadbeat control (NDB). The first is voltage mode and the second is the current mode deadbeat controller. We will investigate briefly both control modes.

3.2 Voltage Mode Nonlinear Deadbeat Control

The voltage mode nonlinear deadbeat (vNDB) [9] controller is designed from voltage equation (3.6) by replacing the next sampling instant voltage $v_O[k+1]$ with the reference voltage $v_{ref}[k+1]$, thus the vNDB is calculated below.

$$\Delta T_2[k] = \frac{v_{ref}[k+1] - \left(1 - \frac{T_s}{RC}\right) v_O[k]}{\frac{1}{C} i_L[k]} \tag{3.8}$$

3.2.1 Modification of vNDB to Avoid Saturation

However for practical purposes (3.8) controller easily saturates when current is very small where the converter will be forced to go into discontinuous conduction mode. Thus the control is modified by multiplying a small gain g_0 to produce new control law $\Delta T_2^{new}[k]$ as follows.

$$\Delta T_2^{new}[k] \equiv g_0 \Delta T_2[k] = g_0 \left(\frac{v_{ref}[k+1] - \left(1 - \frac{T_s}{RC}\right) v_O[k]}{\frac{1}{C} i_L[k]} \right), \quad 0 < g_0 < 1 \tag{3.9}$$

At steady state and when $k \to \infty$ the voltage between one sampling period and next are similar $v_O[k] \approx v_O[k+1]$. Substitute (3.9) into (3.6) and divide output voltage $v_O[k]$ by reference voltage $v_{ref}[k]$ to obtain voltage gain factor $G(g_0)$ below.

$$G(g_0) \equiv \frac{v_O[k]}{v_{ref}[k]} = \frac{g_0}{1 - \left(1 - \frac{T_s}{RC}\right)(1 - g_0)} \tag{3.10}$$

The expression (3.10) points to the weakness of the vNDB method discussed in next section.

3.2.2 Limitations of vNDB

The control law vNDB developed in 3.10 will result into a persistent output voltage steady state error. Another weak point is that the controller will be susceptible to voltage and current ripples and prone to noise within the circuit. [9, 61] We will show results of simulations and experiments later to demonstrate those mentioned weaknesses. Therefore a better and superior control approach is developed in following section.

3.3 Current Mode Nonlinear Deadbeat Control

The current equation (3.7) does not have the inverse response as does the voltage equation (3.6) which was used to derive the vNDB in the previous section. Therefore in this section a current

mode nonlinear deadbeat control (cNDB) is proposed by replacing the next sampling instant current $i_L[k+1]$ with the reference current $I_{ref}[k+1]$. Thus the cNDB control is calculated below. [10, 34, 35]

$$\Delta T_2[k] = \frac{\left(1 - \frac{r_L}{L}T_s\right) i_L[k] - I_{ref}[k+1] + \frac{E}{L}T_s}{\frac{1}{L}v_O[k]} \tag{3.11}$$

The feature of this control law is the design of nonlinear reference current $I_{ref}[k+1]$ which allows the fast response within the maximum current limit of the converter switch. This current reference is proposed to contain two terms as follows.

$$I_{ref}[k+1] = A\left(v_{ref}[k+1] - v_O[k]\right) + I_{Lave}[k] \tag{3.12}$$

The first term $A\left(v_{ref}[k+1] - v_O[k]\right)$ is the output voltage error regulation multiplied by the design parameter A, and the second term $I_{Lave}[k]$ is the average inductance current. Both terms will be designed independently in next sections.

3.3.1 Design of Parameter for Voltage Regulation

By rough approximations, capacitor of Fig. 3.3 needs to be charged from $v_O[k]$ at instant k to $v_{ref}[k+1]$ at instant $k+1$. To do this the inductor will supply energy for the duration of $\Delta T_2[k]/T_s$ of the entire switching period. [34, 35] Thus approximate energy balance equation is formulated below.

$$\frac{1}{2}L\left(I_{ref}[\,k+1]\right)^2\frac{\Delta T_2[k]}{T_s} \approx \frac{1}{2}C\left(v_{ref}[k+1] - v_O[k]\right)^2 \tag{3.13}$$

Which is solved for $I_{ref}[k+1]$ as

$$I_{ref}[k+1] \approx \sqrt{\left(\frac{C}{L}\right)\left(\frac{T_s}{\Delta T_2[k]}\right)}\left(v_{ref}[k+1] - v_O[k]\right), \tag{3.14}$$

thus comparing (3.14) to voltage regulation of (3.12) an inference can be made about approximate value of gain A below.

$$A \approx \sqrt{\left(\frac{C}{L}\right)\left(\frac{T_s}{\Delta T_2[k]}\right)} \tag{3.15}$$

This indicate possible range of the gain A value to use in the iteration to experimental tuning, because in actual experiment, the parameters L and C are not the nominal values and the actual PWM duration $\Delta T_2[k]$ varies within sampling period.

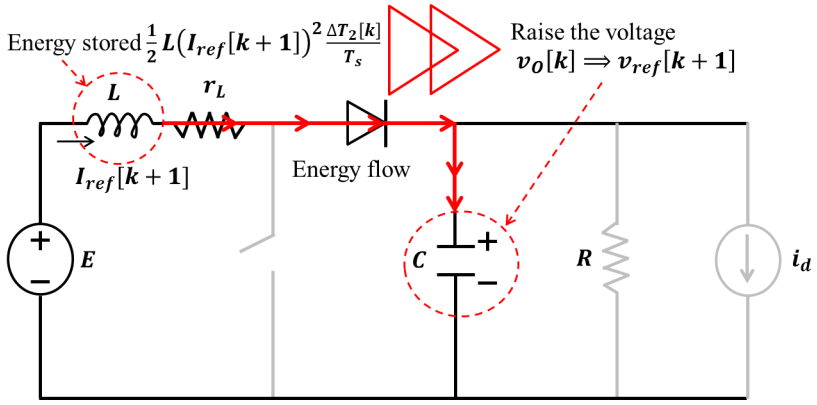


Figure 3.3: Approximate energy flow from inductance L to raise voltage at capacitance C.

3.3.2 Design of Average Inductance Current

To design the average inductance current in s domain $I_{Lave}(s)$ for (3.12) we need to use state space modeling approach. Consider Fig. 3.1(b) and (c) during ON and OFF switch states respectively. Average state space model in continuous time domain is obtained by integrating (3.1)-(3.3) under the respective intervals and dividing by sampling period T_s. Then we can write the s domain transfer functions for output voltage and inductance current below.

$$v_O(s) = \left(\frac{R}{sRC+1}\right)\left(\frac{\Delta T_2(s)}{T_s}\right) i_L(s) - \left(\frac{R}{sRC+1}\right) i_d(s) \tag{3.16}$$

$$i_L(s) = \left(\frac{1}{sL+r_L}\right) E - \left(\frac{1}{sL+r_L}\right)\left(\frac{\Delta T_2(s)}{T_s}\right) v_O(s) \tag{3.17}$$

This modeling has several presentations, one of which is depicted in the block diagram of Fig. 3.4 where the system has three inputs – DC input voltage E, disturbance current $i_d(s)$, and deadbeat control $\Delta T_2(s)/T_s$. Asssuming we know the nominal parameters of the converter, we can derive averaging output current $i_A(s)$ as inverse of the plant (3.16) considering zero disturbance $i_d(s)$ = 0 below.

$$i_A(s) = \left(\frac{sR_nC_n+1}{R_n}\right) v_O(s) \tag{3.18}$$

Where R_n and C_n represents nominal parameters of the converters which might be different from the actual ones due to environment or any other factors. However, the derivative component of (3.18) will amplify high frequency noise. Thus to render the signal useful for control purposes, a low pass filtered version $\hat{i}_A(s)$ is proposed instead, using a filter w_O as the cut off frequency.

$$\hat{i}_A(s) = \left(\frac{w_O}{s+w_O}\right)\left(\frac{sR_nC_n+1}{R_n}\right) v_O(s) \tag{3.19}$$

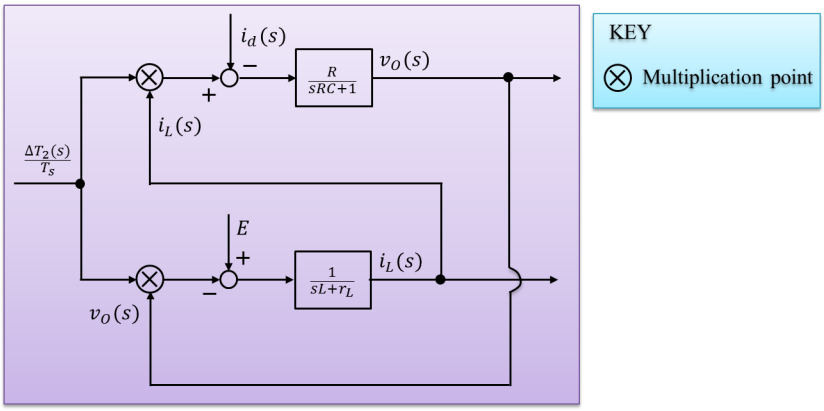


Figure 3.4: Average state space model of boost converter of (3.16)-(3.17).

The caret symbol on top of the variable means it is an estimated value (obtained by low pass filtering the original noisy variable value). However, this equation lacks the robustness to disturbances which occur at higher frequency than the one used to estimate $\hat{i}_A(s)$ in (3.19) because it was derived by assuming disturbance $i_d(s) = 0$. This can be rectified by considering plant (3.16)-(3.17) and use of Fig. 3.4. This disturbance $i_d(s)$ can be estimated by utilizing a low pass filter with cut off frequency w_{obs} in the following equation.

$$\hat{i}_d(s) \equiv \left(\frac{w_{obs}}{s + w_{obs}}\right)\left(\left(\frac{\Delta T_2(s)}{T_s}\right) i_L(s) - \left(\frac{sR_nC_n + 1}{R_n}\right) v_O(s)\right) \tag{3.20}$$

Two control variables have been obtained - the low frequency estimated averaging output current $\hat{i}_A(s)$ in (3.19) and high frequency estimated disturbance current $\hat{i}_d(s)$ in (3.20). The total output current (that passes through the diode to the output of Fig. 3.1(a)) can be taken as sum of these two currents below.

$$\hat{i}_{A-total} \equiv \hat{i}_A(s) + \hat{i}_d(s) \tag{3.21}$$

Where $\hat{i}_{A-total}$ is the total output current and is proportional to average inductor current $I_{Lave}(s)$ and the duty ratio $\Delta T_2(s)/T_s$. Therefore estimation of $\hat{i}_{A-total}$ simplifies the control design and implementation because no current sensors are needed to measure the actual load current $i_A(s)$ and the difficult to measure actual disturbance current $i_d(s)$. Instead, we proceed to use the proportionality relationship between $\hat{i}_{A-total}$, $I_{Lave}(s)$, and $\Delta T_2(s)/T_s$ to propose the new estimated inductance current $\hat{I}_{Lave}(s)$ below.

$$\hat{I}_{Lave}(s) \equiv \left(\frac{w_C}{s + w_C}\right)\left(\frac{T_s}{\Delta T_2(s)}\right)\left(\hat{i}_A(s) + \hat{i}_d(s)\right) \tag{3.22}$$

Where w_C is the filter used to smooth out the duty ratio $\Delta T_2(s)/T_s$ changing at the switching frequency $f_s = 1/T_s$ which would otherwise distort the average signal obtained. Digitally equations (3.19), (3.20) and (3.22) of s domain (continuous time) are implemented in z domain (discrete time) using the Trapezoidal rule according to Appendix B.2.

3.3.3 Overall Proposed Control Block Diagram

This section proposes the complete control block diagram. The voltage error regulation (3.14) and its gain (3.15) in Section 3.3.1, the estimated average inductance current (3.22) in Section 3.3.2 are combined to formulate the nonlinear reference current deadbeat control thus modifying (3.11) and (3.12) respectively shown below.

$$\Delta T_2[k] = \frac{\left(1 - \frac{r_L}{L}T_s\right) i_L[k] - I_{ref}[k+1] + \frac{E}{L}T_s}{\frac{1}{L}v_O[k]} \tag{3.23}$$

$$I_{ref}[k+1] = A\left(v_{ref}[k+1] - v_O[k]\right) + \hat{I}_{Lave}[k] \tag{3.24}$$

Combining all control computations – the continuous time averaged state space model (3.16)-(3.17), estimations of load current, disturbances and inductance current (3.18)-(3.22) and discrete time control (3.23)-(3.24) the complete proposed nonlinear deadbeat reference current control is presented by Fig. 3.5 explained as follows. The upper left blocks correspond to the discrete time nonlinear deadbeat control calculation, the lower left blocks corresponds to the estimation of average inductance current $\hat{I}_{Lave}(s)$, the zero order hold (termed ZOH in the diagram) and the limiter represents the digital pulse width modulator (DPWM), and right side blocks correspond to the state space averaged model which was shown earlier in Fig. 3.4. One should note the constant magnitude block with gain 1 used to explain the division operation of the duty ratio $\Delta T_2(s)$ signal of the lower left hand blocks.

Arrangement of Fig. 3.5 suggests the following design guideline for the filter cut off frequencies which depend on the desired bandwidth. [34] However, precise design will be explained later on.

$$w_O < w_C,\ w_O < w_{obs},\ w_C \leq w_{obs} \tag{3.25}$$

This suggestion will be confirmed experimentally and by simulation later in Chapter 5. Later, we will be develop theories to explain that actually the selection of those filter cut off frequencies can be accomplished arbitrarily with the limitation of the noise and overshoot of the measured signals. [60]

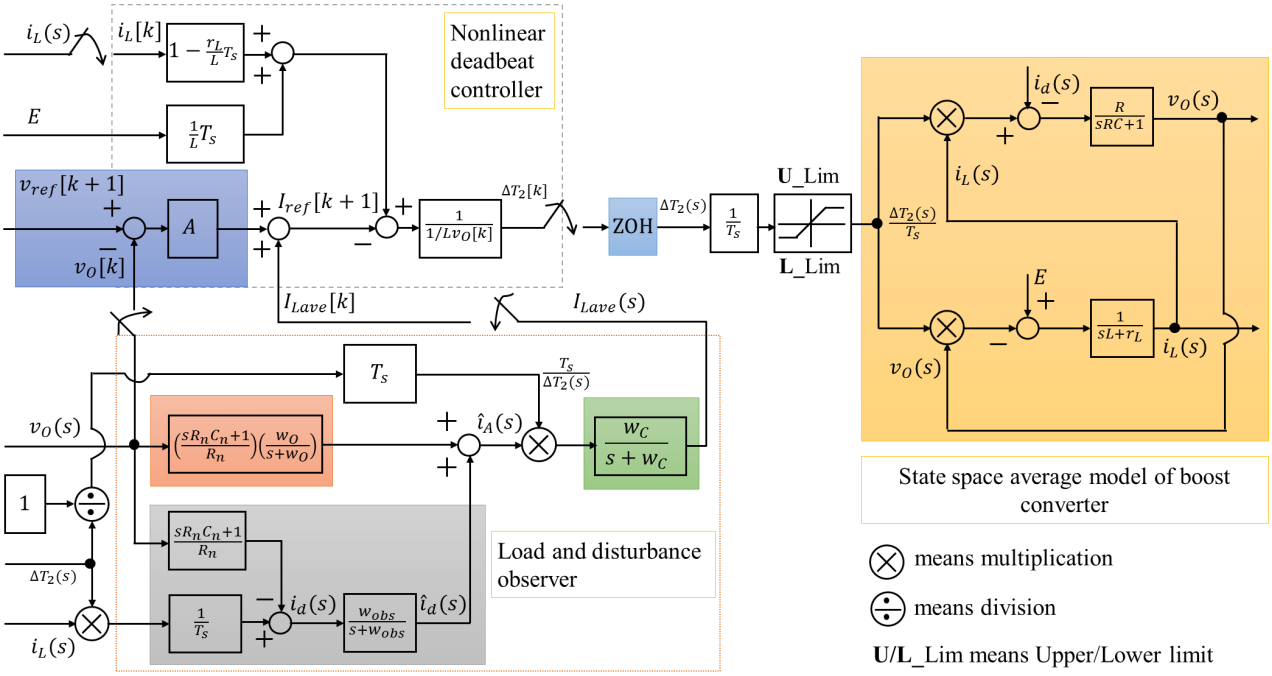


Figure 3.5: Proposed reference current nonlinear deadbeat control block diagram (cNDB).

3.4 Simulation and Experiment Setup

To verify the proposed control methods, several simulations were implemented on the power electronics simulation software (known as PSIM). Empirical gain tunings were achieved on the simulations before implementing them experimentally. After verification by simulation, confirmation by experiment was done on a boost converter with nominal parameters listed in Table 3.1. Note: these parameters are considered to be nominal.

The digital control system (PE–Expert4) made by MyWay Plus Corporation consists of floating point digital signal processor (DSP) TMS320F28335. The inductance current signal was obtained using LEM CAS 15-NP hall effect transducer, while the voltage signal was obtained using simple voltage divider bridge. Output voltage and inductance signals were sampled once at start of every sampling period by the analog to digital converter (A/D). The control code was written on text file on the personal computer (PC), then compiled and downloaded to the DSP. The DSP reads the signals at the start of the sampling period, then calculated the required control variable, and sent the signal to the DPWM. The DPWM sent the signal via digital to analog converter (D/A) to the switching circuit to open or close the switching devices. Further

Table 3.1: Boost Converter Parameters.

Parameter	Symbol	Value	Units
Inductance	L	22	μH
Inductor ESR	r_L	0.05	Ω
Capacitance	C	60	μF
Resistor load	R	4	Ω
Input DC voltage	E	12	V
Switching frequency	f_s	100	kHz
Sampling period	T_s	10	μs
Reference voltage	v_{ref}	$14.64 \rightarrow 20$	V

Table 3.2: Parameters of RC Filters for Experimental Setup.

Parameter	for voltage (v_O) probes	for current (i_L) probes
Resistor	5 kΩ	780 Ω
Capacitor	660 pF	1800 pF
Equivalent time constant	3.3 μs	1.4 μs

the DSP performed condition monitoring, by displaying the current variables via the graphical user interface (GUI). The GUI provided means to collect experiment data by direct saving of text or picture files. That way, the undertaking of the experiment was simplified.

Command voltage change $v_{ref}[k+1]$ was effected at the keyboard. Resistor bank simulated the unknown load disturbance. This disturbance was connected parallel to the known load resistor through a digital circuit which ensured fast connection to avoid the possible ringing brought by use of mechanical switches observed previously. [1]

Further, since the output voltage and inductance current were observed to be noisy, it was necessary to connect RC filters to signal probes, where the filter parameters are displayed in Table 3.2. All measuring signal cables were made very short twisted pair cables to reduce crosstalk. However, there was still significant noise observed in the signal collected and analyzed as will be shown later in presented results.

3.5 Summary of Chapter Three

We have presented research methodologies by developing the necessary discrete time model of the boost converter and its equivalent continuous time model. Then we used the modeling to develop nonlinear deadbeat control laws and explained the simulation through use of PSIM software. We have explained the simulation procedures and explained experimental setup for implementation of the proposed deadbeat control laws on the boost converter. We have explained how the signal conditioning is done on the experimental platform.

Chapter 4

Voltage Mode Control Simulation and Experiment Results

This chapter discusses the results of simulation and experiment by applying the voltage mode control (vNDB) of Section 3.2. This chapter will explore the vNDB performance for boost converter that supplies large load current (i.e. small resistance of 4 Ω) and we will focus on the sensitivity to parameter L the converter's inductance.

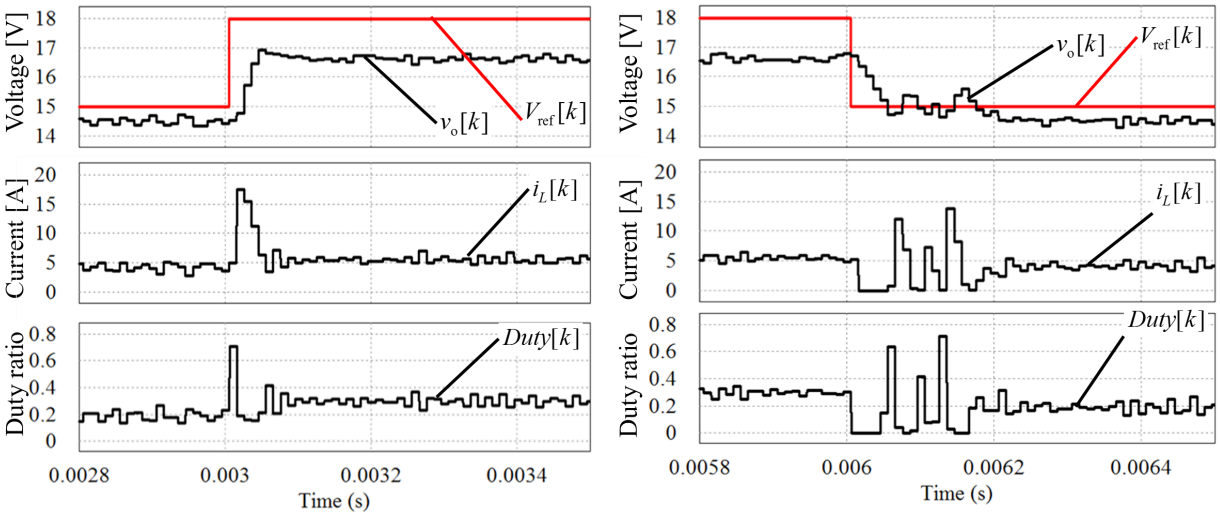
4.1 Sensitivity of Voltage Mode Control to Inductance

During voltage command increase, the vNDB developed by Equation 3.9 can realize short rising time when the converter is designed with smaller inductance. [61] However, the system quickly become unstable when too small inductance value was used signifying the sensitivity of this control to that parameter. On the other hand, the falling time does not depend on inductance, but on output capacitance. [19] These were observations based on simulations and experiments for different scenarios. The first scenario voltage reference was increased from 15 V to 18 V, and two inductance values – 5 μH and 20 μH were investigated. The second scenario voltage reference was decreased from 18 V to 15 V with similar inductance values as previous scenario. In following figures, $v_O[k]$ represents output voltage, $V_{ref}[k]$ represents reference voltage, $i_L[k]$ represents inductance current, and $Duty[k]$ represents duty ratio.

$$Duty[k] = 1 - \frac{\Delta T_2[k]}{T_s} \tag{4.1}$$

With input DC voltage E the output voltage is related to the duty ratio by the following.

$$v_O[k] = \frac{ET_s}{\Delta T_2[k]} \tag{4.2}$$



(a) Waveforms during voltage rising.

(b) Waveforms during voltage falling.

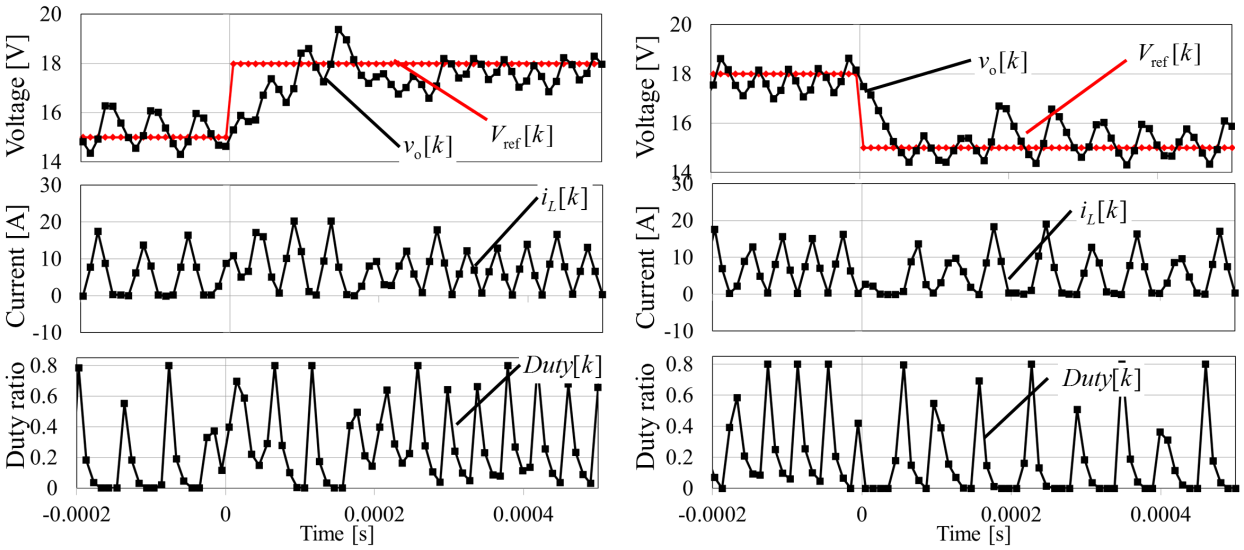
Figure 4.1: Simulation waveforms for $L = 5$ μH : (a) voltage rising, and (b) voltage falling.

Figures 4.1-4.4 the LHS are waveforms during voltage command increase, while the RHS are waveforms during voltage command decrease. The order of the waveforms displayed goes as follows – top is the output voltage, middle is the inductance current, and bottom is the duty ratio.

Therefore when inductance was $L = 5$ μH simulation waveforms are shown by Fig. 4.1 and experiment waveforms are shown by Fig. 4.2. This case represents the low inductance value. Lower than $L = 5$ μH the system was completely unstable so the results will not be presented here. When inductance was $L = 20$ μH simulation waveforms are shown by Fig. 4.3 and experiment waveforms are shown by Fig. 4.4. This case represents the high inductance value.

4.2 Results and Discussions

First, it is noted that, large inductance value is important to stabilize the experiment system. [61] Second, simulation output voltage differed from experiment with regards to steady state error. This was because the experiment system saturated easily, see duty ratio saturation on Figs. 4.2(a) and (b) both cases of voltage command increase (15 V to 18 V) and voltage command decrease (18 V to 15 V). The other difference was that in the experiment the duty ratio and current oscillated more than the simulation results. Several reasons could be the causes of such oscillations, for example noise in the experiment set, and experiment parameter's



(a) Waveforms during voltage rising.

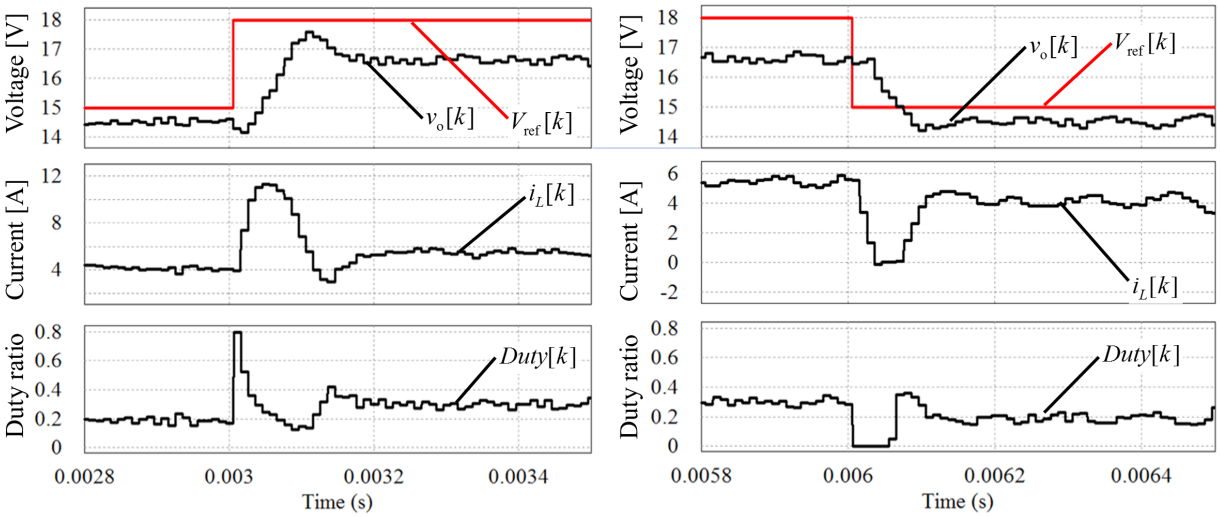
(b) Waveforms during voltage falling.

Figure 4.2: Experiment waveforms for $L = 5$ μH : (a) voltage rising, and (b) voltage falling.

tolerances. Lastly, it is noted that the vNDB control causes steady state error because the gain g_0 of (3.9) cannot be made very big otherwise the system become unstable. Figs. 4.1-4.2 show results for $L = 5$ μH which contain more oscillations than those of Figs. 4.3-4.4 results for $L = 20$ μH. Thus the converter's responses improved due to increase of inductance L, a strong dependence of the vNDB on the system parameters. Because of these observations, it became clear that it is better to develop the nonlinear deadbeat control by the current mode control which will show better response waveforms than voltage mode control has shown.

4.3 Summary of Chapter Four

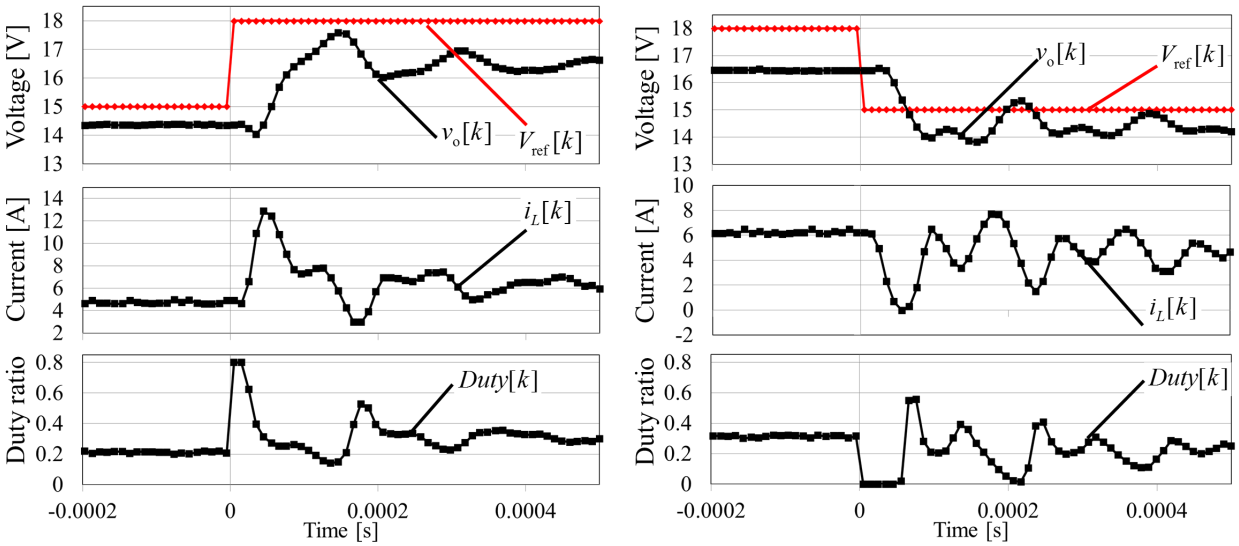
This chapter presented simulations and experiment results of voltage mode deadbeat control. It was shown that vNDB is heavily sensitive to inductance value, and easy for duty ratio and current to saturate. Steady state error persisted because gain tuning had to be within a very small range and the experiment system was prone to noise. Further, it was noted that the responses oscillations became less with increase of inductance value, which is not desired in this deadbeat control.



(a) Waveforms during voltage rising.

(b) Waveforms during voltage falling.

Figure 4.3: Simulation waveforms for $L = 20\ \mu$H : (a) voltage rising, and (b) voltage falling.



(a) Waveforms during voltage rising.

(b) Waveforms during voltage falling.

Figure 4.4: Experiment waveforms for $L = 20\ \mu$H : (a) voltage rising, and (b) voltage falling.

Chapter 5

Current Mode Control Simulation and Experiment Results

Simulation and experiment results of current mode control (cNDB) of Section 3.3 are presented here. First, nominal controller settings are tabulated in Table 5.1 which are based on nominal converter's plant model.

5.1 Voltage Reference Tracking

The voltage reference was abruptly changed from 14.64 V to 20.0 V. Simulated voltage command tracking capability results are presented in Fig. 5.1 while experiment verification of voltage command tracking capability results are presented in Fig. 5.2. Performance index measured is voltage settling time (t_s). Simulated results (Fig. 5.1) show settling time 277 μs and experiment results (Fig. 5.2) show settling time 280 μs. The negative voltage response (from 14.64 V dip to 14.0 V) due to the presence of right-half-plane zero [1, 18] is observed. Both experiment and

Table 5.1: Nominal Settings for the Nonlinear Current Deadbeat Controller.

Parameter	for experiment	for simulation	Units
Gain A	1.6	2.6	–
w_C	4	4	krad/s
w_O	4	4	krad/s
w_{obs}	4	4	krad/s
C_n	60	60	μF
R_n	4	4	Ω
L_n	20	20	μH

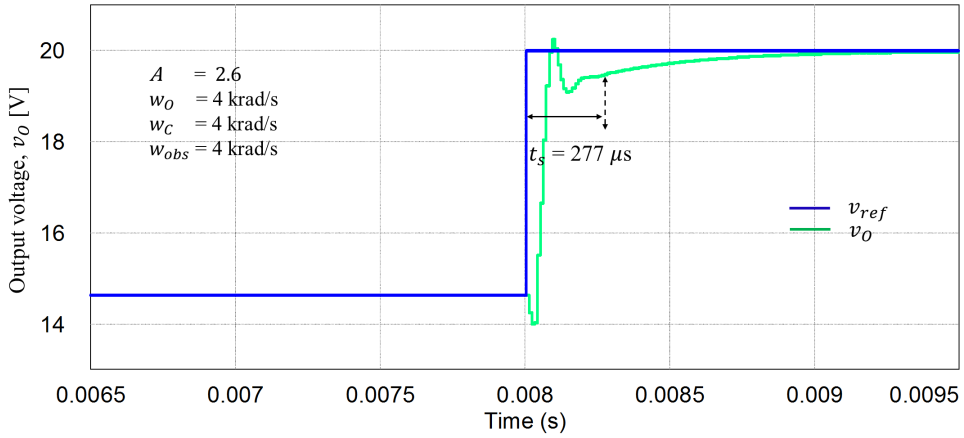


Figure 5.1: Reference tracking:-output voltage and reference results (voltage tracking settling time $t_s = 277$ μs, simulation waveforms).

simulation results agree very well. The current responses during the voltage reference tracking are shown in Fig. 5.3 for simulation and Fig. 5.4 for experiment. They show good agreements.

5.2 Disturbance Suppression

Load disturbance was input by a sudden connection of unknown resistor bank to the output of the converter. Disturbance suppression capability results are presented in Fig. 5.5 for simulation and in Fig. 5.6 for experiment. Performance index measured is the voltage recovery time (t_{rec}). Simulated results (in Fig. 5.5) and experiment results (in Fig. 5.6) show disturbance suppression capability with recovery time 1.34 ms and 1.46 ms respectively. This demonstrates good agreement of simulated theory and experiment implementation.

5.3 Decreasing and Increasing Load Current

Above results have demonstrated the utility of the cNDB control method for both voltage command reference tracking and disturbance rejection recovery. Another aspect to investigate is the case for 50% decrease and increase of load current which is considered as a severe situation for a boost converter in operation. It is a severe situation causing large voltage surge or dip of the output voltage which the controller has to adjust quickly to track the reference. [30] Figures 5.7-5.8 presents the simulation results of this investigation; i.e. (1) 50% load current decrease which is from 3.66 A to 1.8 A, and (2) 50% load current increase which is from 1.8 A to 3.66 A.

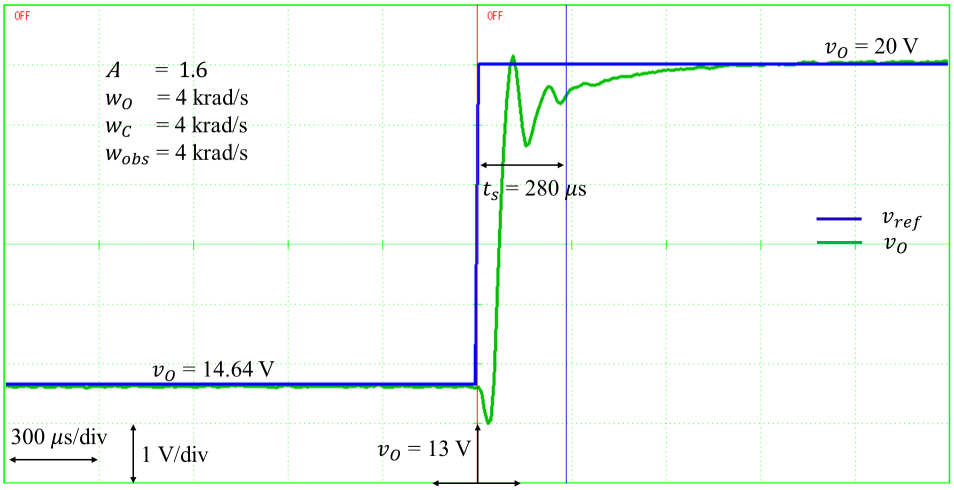


Figure 5.2: Reference tracking:-output voltage and reference results (voltage tracking settling time $t_s = 280$ μs, experiment waveforms).

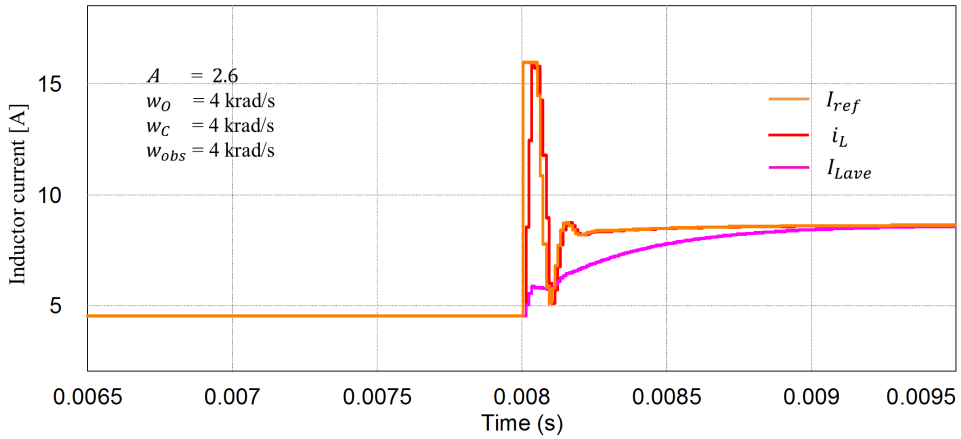


Figure 5.3: Inductor currents during voltage reference tracking (simulation waveforms).

As expected the large voltage surge appears in Fig. 5.7, and the deadbeat control manages to eliminate voltage error quickly and the voltage was controlled to the reference command after about 1 ms. Large voltage dip occurred in Fig. 5.8, the deadbeat controller quickly controlled the voltage to the reference by eliminating the voltage error after about 1.41 ms. It can be concluded that large load disturbance of Fig. 5.8 takes longer to recovery than of Fig. 5.7. The reason is that large load increase cause increase of the converter's time constant, whereas large load decrease reduces the converter's time constant given by $\tau = 1/RC$. Note that, load current is given as $i_O(s) = v_O(s)/R$. Because of time limitations experimental verification of this result is not presented in this thesis. Simulation and experiment results of disturbance rejection of

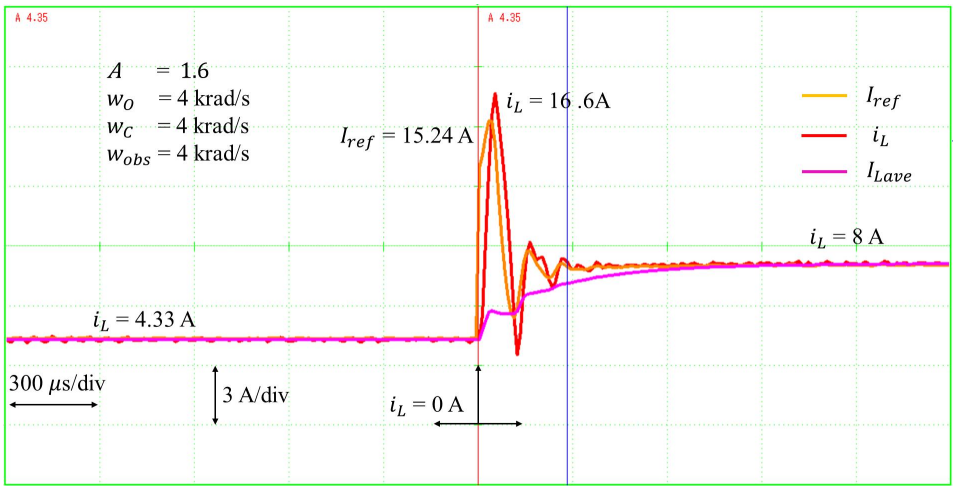


Figure 5.4: Inductor currents during voltage reference tracking (experiment waveforms).

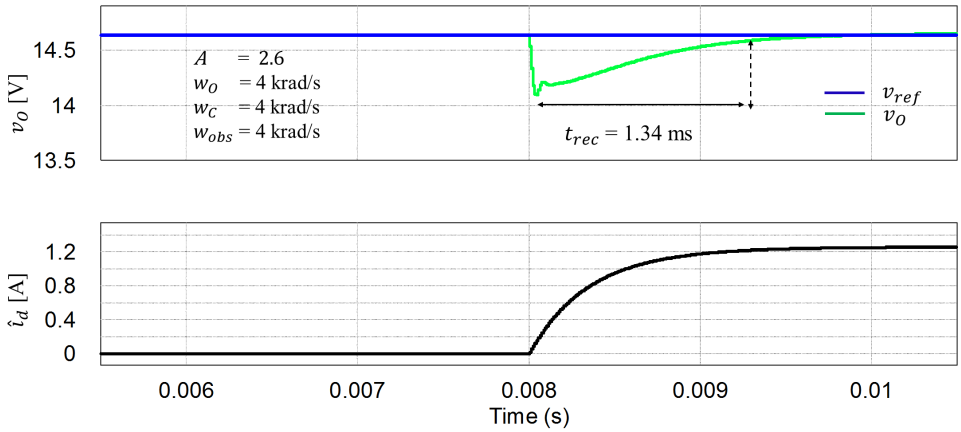


Figure 5.5: Simulation results of disturbance rejection. Top: the output voltage and the reference. Bottom: the estimated disturbance. Disturbance rejection time $t_{rec} = 1.34$ ms.

Figs. 5.5-5.6 are similar, therefore the 50% load current reduction or increase experimental results are expected to be similar to the simulated voltage responses presented by Figs. 5.7-5.8.

5.4 Discussions

This section presents further discussions about the present research and also makes comparison to previous literatures. First we outline the originality of this research approach. Then we proceed to explain how to empirically determine the controller parameters, and explain the observations of this control approach.

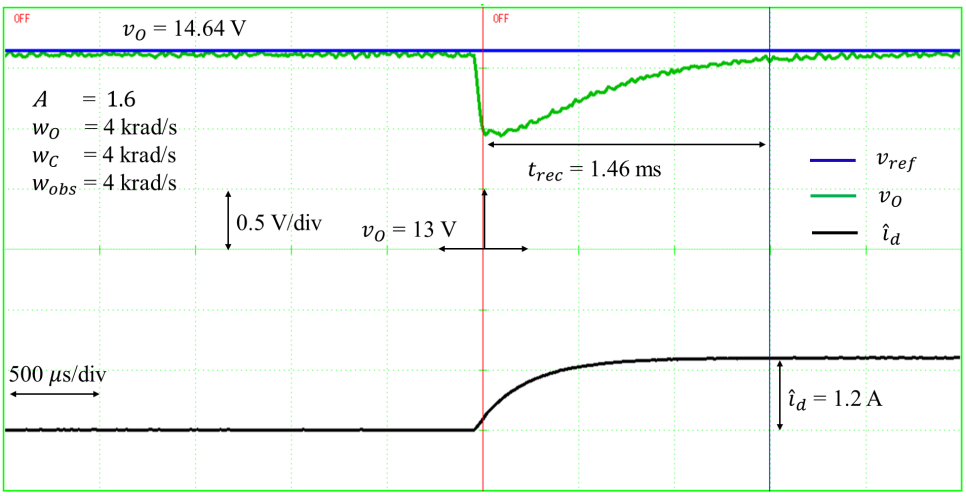


Figure 5.6: Experiment results of disturbance rejection. Top: the output voltage and the reference. Bottom: the estimated disturbance. Disturbance rejection time $t_{rec} = 1.46$ ms.

5.4.1 Originality of this Research

This research has achieved the following five major contributions. Firstly it has developed the discrete time nonlinear state equations for a boost converter in CCM. Secondly it has used this modeling to develop a new nonlinear current reference deadbeat control which is better than the voltage mode control. Thirdly the current reference was proposed to contain two terms: – one is the output voltage regulation and the other is the estimated steady state inductance current. Fourthly, the load disturbance observer is proposed and is added to current reference term for feedforward disturbance compensation. Due to the implementation of this cNDB, a very quick reference voltage tracking was experimentally achieved with the disturbance recovery time in the reasonably quick range. Finally, simulation results indicated the ability of this control method to eliminate voltage surges or dips due to sudden large decrease or increase of load current.

5.4.2 How to Empirically Determine the Controller Parameters

The selection of the three parameters in Fig. 3.5 is done empirically as follows. The w_O is the smoothing filter for the average load current, and it should be the lowest among w_C and w_{obs}. w_C is the cut off frequency of the low pass filter for the nonlinear term $T_s/\Delta T_2(s)$. It should be a little higher than w_O. w_{obs} is the cut off frequency of the load disturbance observer, thus it should be high enough to compensate the high frequency disturbance components. Thus

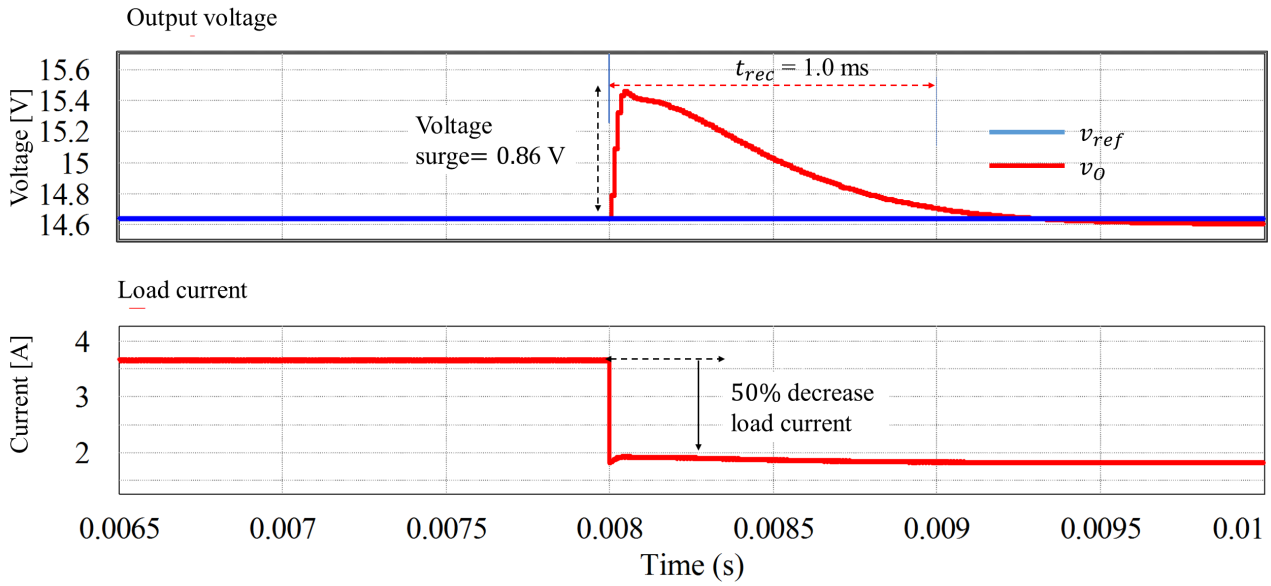


Figure 5.7: Simulation results when load current is reduced by 50%. Top: output voltage and reference. Bottom: load current.

condition explained in (3.25) is reasonable.

This suggestion is confirmed in Fig. 5.8 for settling time trends and Fig. 5.9 for recovery time trends depending on the values of those three cut off frequencies. Later we will give bode plots and explanations in Chapter 6 of overall performances of these three parameters. Use of (3.15) to calculate gain A is possible in simulations, but author found that due to square root and inverse operation involved, it became unstable during experiment in DSP code implementation. Thus they chose constant gain A ($A = 1.6$ for experiment and $A = 2.6$ for simulations). Gain A for simulation is higher, because there is no delay in control during simulation, while in experiment there is control delay and when gain A is large it causes large output voltage oscillations. Later in Chapter 6 we will explain how to determine this gain concretely.

5.4.3 Differences Between Simulation and Experiment Results

This subsection explains the differences between output voltage oscillations between simulation (Fig. 5.1) and experiment results (Fig. 5.2). For better explanations, the the two figures are joined in one display in Fig. 5.11 below. Both simulation and experiment voltage output response are shown and the oscillation region where they differ is highlighted. Empirically we can attribute those differences to time delay in experiment and unmodeled nonlinear switching

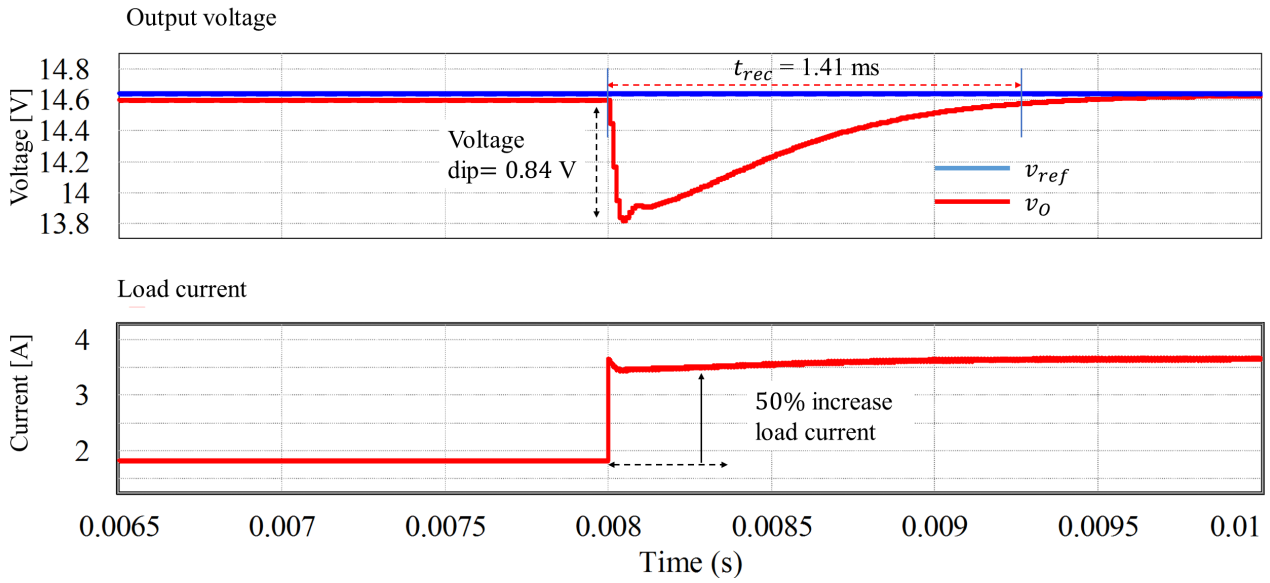


Figure 5.8: Simulation results when load current is increased by 50%. Top: output voltage and reference. Bottom: load current.

phenomena occuring in the switches. Later in Chapter 6 stability analysis we will see the causes of the oscillations and other nonlinearities.

5.4.4 Shortening Voltage Settling and Recovery Time

This Section presents summary of results which indicate that the settling and recovery time are shortened by the nonlinear reference current deadbeat control. Due to condition in (3.25) and arrangements of Fig. 3.5, w_C has higher influence on the settling time than does w_{obs}. It should be noted that if w_C is selected very low, the immediate effect is slower voltage responses, see Fig. 5.9 on left hand side.

Sudden disturbance requires both quick estimation (by w_{obs}) and fast feed forward (by w_C). That is why Fig. 5.10 shows the disturbance rejection capability increases with increase of both w_{obs} and w_C. In that figure it is noted that if these two filters are fast for example $w_{obs} = w_C = 5.0$ krad/s a 1.2 ms recovery time is realized which is reasonably fast, however it would cause a large overshoot and large oscillations. Therefore we can confirm that proper selection of w_{obs} and w_C could result into shortening the t_s and t_{rec}.

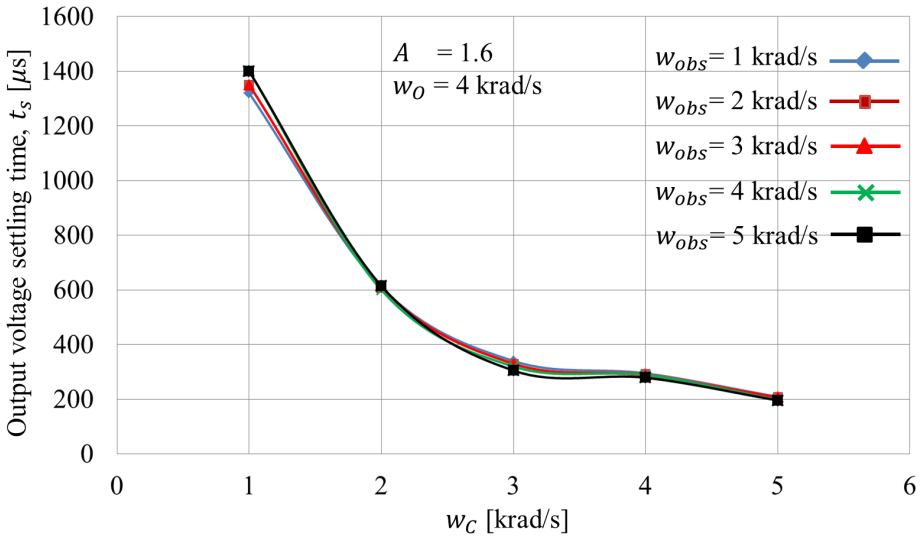


Figure 5.9: Experiment results of settling time (t_s) trends with filter cut off frequencies.

5.4.5 Performance Comparisons to Past Literatures

The proposed control method (cNDB) is compared to past literature which applied digital control to boost converter for various applications [1, 11–13, 15–20] summarised in Table 5.2.

Voltage command tracking capability is shown in Table 5.2 on sixth column (settling time, t_s). Shirazi et al. [17] showed the settling time 800 μs for switching mode power supplies. Oettmeier et al. [16] proposed a model predictive controller (MPC) with a sliding mode observer for portable electronic devices, and reported settling time 1700 μs for voltage change 165 V to 175 V. This research reports 280 μs settling time for a converter applied in servomotor applications.

Disturbance suppression capability is shown in Table 5.2 on last column (recovery time, t_{rec}). Tong et al. [20] reported the recovery time 0.18 ms for automotive applications. Karamanakos et al. [15] proposed a direct voltage control using enumeration based MPC for DC motor drives applications, and reported recovery time 0.7 ms for load change 0.2 A to 0.4 A. On the other hand, this research reports 1.46 ms recovery time for load change 3.66 A to 4.88 A. This load current is 3.6 times larger than that in Tong et al. [20], thus it is in reasonably quick range.

Comparison with respect to switching frequency is presented in Table 5.2 on second column. Oucheriah et al. [13] proposed a PWM-based adaptive sliding-mode control for a switching frequency 200 kHz, and reported slower responses than this research.

Comparison with respect to sampling period is presented in Table 5.2 on third column.

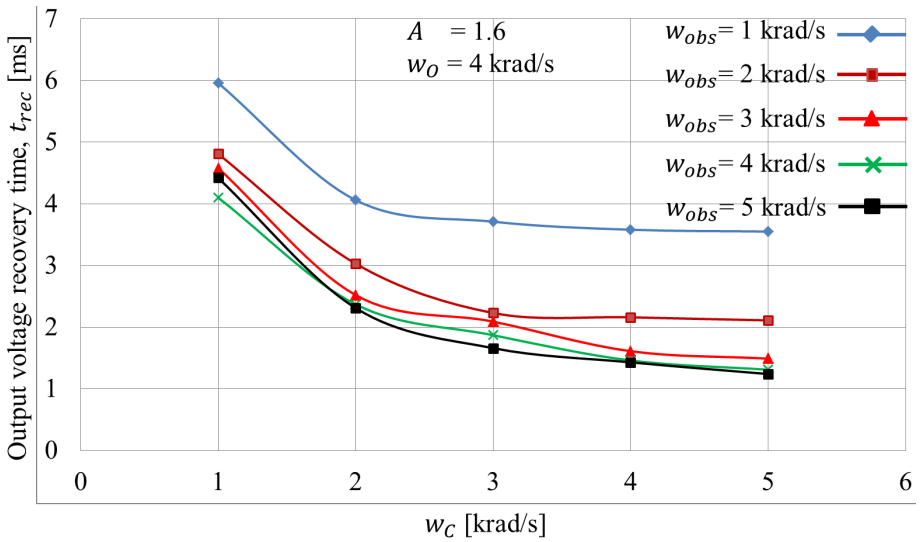


Figure 5.10: Experiment results of recovery time (t_{rec}) trends with filter cut off frequencies.

Chen et al. [18] proposed a closed-loop analysis and cascade control for sampling period 1 μs, and reported slower responses than this paper.

Comparison based on amount of load current can be seen on seventh column (disturbance or load change) of Table 5.2. The table shows that all loads (load current) supplied by other converters are several orders of magnitude smaller than the one in this thesis. Regardless of this larger load on the converter, the cNDB has better t_s and t_{rec} than others.

We can conclude that this thesis proposed control (cNDB) reports better responses than other literature, even though it is based on discrete time modeling and the controller tuning was done empirically.

5.5 Summary of Chapter Five

We have presented detailed simulation and experimental results which showed superiority of cNDB control over the previous vNDB control. The experimental results were better than other previous literature for boost converters of various applications. The controller was able to suppress the voltage surge/dip due to sudden reduction/increase of the load current. Differences between simulations and experiments results were explained to be caused by unmodelled switching device phenomena.

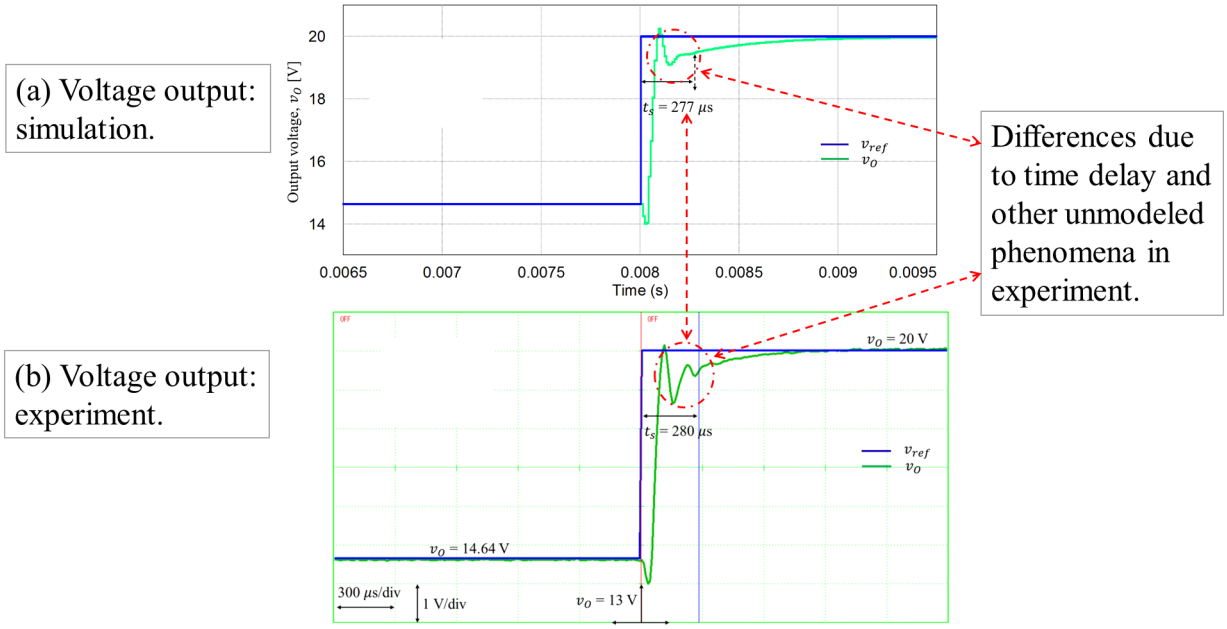


Figure 5.11: Difference of output voltage oscillations between simulation and experiment.

Publication date	Switching frequency [kHz]	Sampling period [μs]	Input voltage [V]	Output voltage change [V]	t_s [μs]	Disturbance (load change)	t_{rec} [ms]
Flores et al, 2014 [12]	45	100	NA**	15 → 24	3000	89 → 38 Ω	Not known*
Oucheriah et al., 2013 [13]	200	NA**	6 → 10	7 → 12	25000	160 → 40 Ω	20
Tong et al., 2014 [20]	100	10	5 → 6	15	NA**	15 → 10 Ω	0.18
Karamanakos et al., 2013 [22]	NA**	15	10 → 13.5	15 → 30	3500	73 → 36.5 Ω	2
Karamanakos et al., 2014 [15]	NA**	10	10 → 15	15 → 30	1900	73 → 36.5 Ω	0.7
Oettmeier et al., 2009 [16]	16	NA**	115	165 → 175	1700	NA**	NA**
Shirazi et al., 2009 [17]	195	0.72	15	30 → 35	800	0.3 → 0.6 A	0.6
Chen et al., 2011 [18]	20	1	20	35 → 40	10000	40 → 30 Ω	10
Takei et al., 2014 [19]	10	NA**	50	100	NA**	3 → 8 A	5
Kim et al., 2017 [40]	100	10	8 → 12	16 → 18	2000	40 → 20 Ω	2.5
Kirshenboim et al., 2017 [24]	200	NA**	3.3	12	NA**	0.5 → 2.4 A	0.15
Mushi et al., 2015 [1]	100	10	12	20 → 21	5000	2 → 2.5 A	17
This thesis (cNDB)	100	10	12	14.64 → 20.0	280	4 → 3 Ω	1.46

t_s	is the settling time defined as period for the voltage to change from 0% of command voltage to its settling value within 90% command voltage.
t_{rec}	is the recovery time defined as period for the voltage to recover from 100% voltage dip to when more than 90% of the voltage dip is recovered after sudden disturbance.
Not known*	Difficult to read data from figure presented in that paper.
NA**	Figure and/or data not available in that paper.
→	Means from to.

The sixth column of **disturbance (load change)** includes both change of load resistance and output load current as written in respective references.

Table 5.2: Performance Comparison of cNDB with Past Literatures.

Chapter 6

Nonlinear Phenomena and Stability Analysis

Nonlinear phenomena was observed in the previous chapter. This Chapter explains the detailed reason why such phenomena occur through mathematical analysis, simulation and experimental results. As a result, stability analysis is accomplished as well and method to concretely design the controller parameters are outlined. First we note that under nominal input DC voltage E the converter will operate at steady state point defined by the following.

$$v_O[k]_{k\to\infty} = V_\infty \tag{6.1}$$

$$i_L[k]_{k\to\infty} = I_{L\infty} \tag{6.2}$$

$$\Delta T_2[k]_{k\to\infty} = \Delta T_{2\infty} \tag{6.3}$$

$$\hat{I}_{Lave}[k]_{k\to\infty} = \hat{I}_{Lave\infty} \tag{6.4}$$

$$i_L[k]_{k\to\infty} = I_{ref}[k]_{k\to\infty} = \hat{I}_{Lave\infty} \tag{6.5}$$

Where X_∞ represents the respective steady state variable at that operating point.

6.1 Nonlinear Phenomena

There is nonlinear phenomena occurring in Fig. 5.1-5.2, thought to be caused by the differences between $\hat{I}_{Lave}[k]$ and $i_L[k]$ shown in Fig. 5.3-5.4 for both simulation and experiment results. Earlier investigations of these phenomena [35] pointed out possible reasons which are going to be expanded and explained in the next section. We will investigate the causes of the nonlinearities through stability analysis by deriving conditions for asymptotic stability of the system.

6.2 Stability Analysis

The detailed stability analysis is discussed in this section. It is conducted by considering variations of variables such as the voltage and inductance current, variations of converter parameters (L and C) [43] from their nominal values, variations of the gain A and its limitation to the performance of the system, unlike the one considering boundary and hybrid controllers. [38]

6.2.1 Stability when Inductance Current is Constant

We will use the discrete model developed in (3.6)-(3.7) and other equations from Chapter 3 to formulate our stability analysis. Suppose that the current does not change during any voltage transient. Then, putting (3.11) into (3.7) shows current tracking reference current within one sampling period to be following.

$$i_L[k+1] = I_{ref}[k+1] \tag{6.6}$$

We use the following assumptions of zero disturbance $i_d[k] = 0$ and no change of inductance current $i_L[k]$, and voltage change $\Delta v_O[k]$ below.

$$\begin{aligned} i_d[k] &= 0 && (6.7)\\ i_L[k] &= \hat{I}_{Lave\infty} = I_{ref}[k+1] && (6.8)\\ v_O[k] &= V_\infty + \Delta v_O[k] && (6.9)\\ v_O[k+1] &= V_\infty + \Delta v_O[k+1] && (6.10) \end{aligned}$$

Short calculation involving (3.6), (3.11) and (6.7) will give following next sampling instant voltage.

$$v_O[k+1] = \left(1 - \frac{T_s}{RC}\right) v_O[k] + \frac{T_s}{C} i_L[k] \left(\frac{E - r_L i_L[k]}{v_O[k]}\right). \tag{6.11}$$

Substituting (6.1)-(6.5) into (6.11) will yield steady state condition (6.12) below.

$$\frac{V_\infty}{R} = \hat{I}_{Lave\infty} \left(\frac{E - r_L \hat{I}_{Lave\infty}}{V_\infty}\right) \tag{6.12}$$

Condition (6.8), voltage Eqs. (6.9)-(6.11), the steady state condition (6.12) above and the approximation (6.13) are used together to calculate voltage error (6.14) with its solution given

by (6.15).

$$\frac{1}{v_O[k]} \equiv \frac{1}{V_\infty + \Delta v_O[k]} \approx \frac{1}{V_\infty}\left(1 - \frac{\Delta v_O[k]}{V_\infty}\right) \tag{6.13}$$

$$\Delta v_O[k+1] = \left(1 - \frac{2T_s}{RC}\right)\Delta v_O[k] \tag{6.14}$$

$$\Delta v_O[k] = \left(1 - \frac{2T_s}{RC}\right)^k \Delta v_O[0] \tag{6.15}$$

Value of $(1-2T_s/(RC))^k$ in (6.15) decreases as $k \to \infty$, thus $\Delta v_O[k]$ will converge asymptotically to zero and voltage does not overshoot or oscillate. This analysis was termed 'simplified stability analysis' in [35] because of assumption of constant current operation which is not realistic. Overshoot and oscillations occurred in the presented results and this discussion need to be expanded in next sections.

6.2.2 Stability when Inductance Current is Not Constant

Previous section assumed a smooth and constant current during voltage transient. However, Fig. 5.2 showed overshoot and oscillations of output voltage for experiment results. These results point that $i_L[k]$ deviates from $\hat{I}_{Lave\infty}$ which is actually observed in Fig. 5.4 where the inductor current experiment results are presented. Thus following inductor current relationship may be assumed.

$$i_L[k] = \hat{I}_{Lave\infty} + \Delta i_L[k] \tag{6.16}$$

Where $\Delta i_L[k]$ is current variation around the equilibrium point. Using (6.9)-(6.13) and (6.16) in short calculations yields (6.17) as the new nonlinear voltage error.

$$\begin{aligned}\Delta v_O[k+1] = &\left(1 - \frac{T_s}{RC}(2 + \alpha[k])\right)\Delta v_O[k] \\ &+ \frac{T_s}{RC}\left(V_\infty \alpha[k] - \frac{(1+\alpha[k])\,\alpha[k] r_L \hat{I}_{Lave\infty}}{E - r_L \hat{I}_{Lave\infty}}\right)(V_\infty - \Delta v_O[k])\end{aligned} \tag{6.17}$$

Where the ratio of current error to average current is denoted $\alpha[k]$ which varies rapidly with time shown below.

$$\alpha[k] \equiv \frac{\Delta i_L[k]}{\hat{I}_{Lave\infty}} = \frac{i_L[k] - \hat{I}_{Lave\infty}}{\hat{I}_{Lave\infty}} \tag{6.18}$$

The following observations are made as depicted in Fig. 6.1:

1. If $\alpha[k]$ represented by (6.18) is very large, voltage error (6.17) will overshoot and oscillations occur in the transient.

2. Simplification of (6.17) gives one of its terms as the nonlinear product (6.19),

$$\frac{\Delta v_O[k]}{V_\infty}\alpha^2[k] \tag{6.19}$$

which if large and oscillatory will cause (6.17) to overshoot and oscillate.

3. Equation (6.19) also indicate that if either $\Delta v_O[k]$ or $\alpha[k]$ is decreasing in next sampling instants, then the oscillations will decrease in amplitude.

When the converter is operating at duty ratio (0.1<duty<0.5, duty = 1 - $\Delta T_2[k]/T_s$) the following approximations

$$\frac{r_L \hat{I}_{Lave\infty}}{E} \approx 0, \text{and } \frac{\Delta v_O[k]}{V_\infty} \approx 0 \tag{6.20}$$

can be used in (6.17) to calculate voltage error as (6.21).

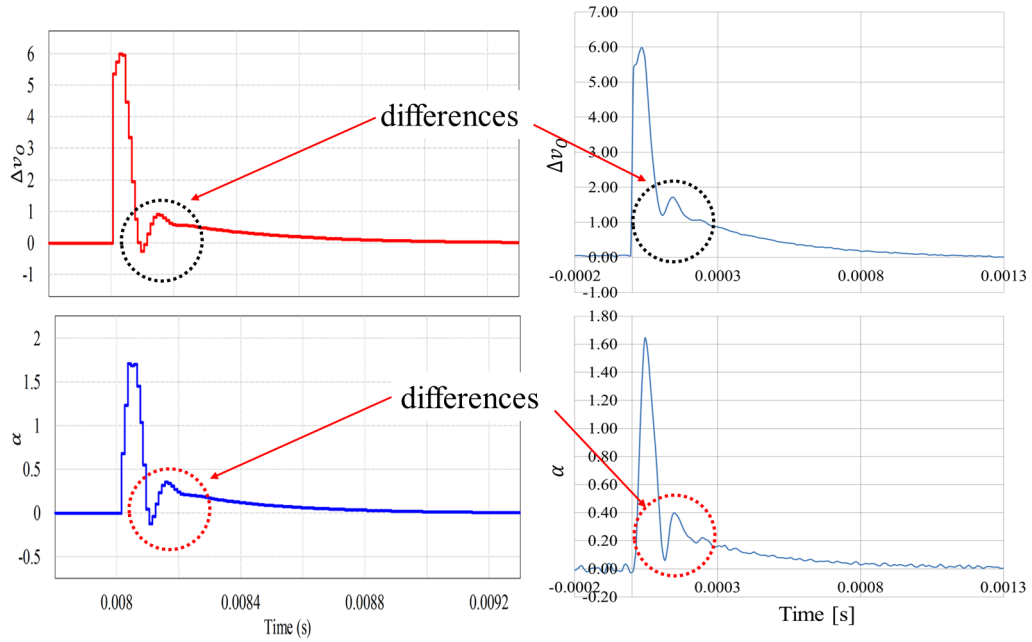
$$\Delta v_O[k+1] = \left(1 - \frac{T_s}{RC}\left(2 + \alpha[k]\right)\right)\Delta v_O[k] + \frac{T_s}{RC}V_\infty \alpha[k] \tag{6.21}$$

Therefore voltage error (6.21) will spike on account of large $\alpha[k]$ see Fig. 6.1 where Fig. 6.1(a) represents simulation results, and Fig. 6.1(b)represents experiment results. In the figure top is $\Delta v_O[k]$ and bottom is $\alpha[k]$. Deadbeat controller will ensure current is controlled to the reference thus in (6.18) $\alpha[k] \approx 0$ in few sampling instants. After initial overshoot the voltage oscillation is not sustained shown by Fig. 6.1, confirming system stability even when current changes.

6.2.3 Stability with Regards to Gain for Voltage Regulation

During experiments large gain A used to compute voltage error regulation (3.14) caused large overshoot and oscillations, this section investigates this phenomena. Substitute (3.11) and (3.12) into (3.6) to obtain (6.22).

$$\begin{aligned} v_O[k+1] = &\left(1 - \frac{T_s}{RC}\right)v_O[k] \\ &+ \frac{L}{C}\frac{i_L[k]}{v_O[k]}\left(\left(1 - \frac{r_L}{L}T_s\right)i_L[k] - A\left(v_{ref}[k+1] - v_O[k]\right) - \hat{I}_{Lave}[k] + \frac{E}{L}T_s\right) \end{aligned} \tag{6.22}$$



(a) Simulation results (b) Experiment results

Figure 6.1: Simulation and experiment results. Top: voltage error $\Delta v_O[k]$. Bottom: ratio of current error $\alpha[k]$.

In one sampling period it is reasonable to make an assumption that $i_L[k] \approx \hat{I}_{Lave}[k]$, which when applied into (6.22) the result will be (6.23).

$$\begin{aligned} v_O[k+1] = &\left(1 - \frac{T_s}{RC}\right) v_O[k] \\ &- \frac{L}{C}\frac{\hat{I}_{Lave}[k]}{v_O[k]}\left(A\left(v_{ref}[k+1] - v_O[k]\right) + \frac{T_s}{L}\left(E - r_L\hat{I}_{Lave}[k]\right)\right) \end{aligned} \tag{6.23}$$

Let's define β as the following ratio which is non-negative scalar and not greater than unity.

$$\beta \equiv \frac{E - r_L\hat{I}_{Lave}[k]}{v_O[k]}, \text{ where } 0 < \beta < 1 \tag{6.24}$$

This ratio (6.24) when used into (6.23) and followed by short computation yields the following.

$$v_O[k+1] = \left(1 - \frac{T_s}{RC}\right) v_O[k] + \beta\frac{T_s}{C}\hat{I}_{Lave}[k] \quad - A\frac{L}{C}\frac{\hat{I}_{Lave}[k]}{v_O[k]}\left(v_{ref}[k+1] - v_O[k]\right) \tag{6.25}$$

Since $V_\infty \approx v_{ref}[k+1]$, $\hat{I}_{Lave}[k] \approx \hat{I}_{Lave\infty}$ and apply (6.8)-(6.10), and (6.13) into (6.25) followed by performing short computations, the following relations are obtained.

$$\frac{V_\infty}{R} = \beta \hat{I}_{Lave\infty} \tag{6.26}$$

$$\Delta v_O[k+1] = \left(1 - \frac{T_s}{RC} + A\frac{L}{C}\frac{\hat{I}_{Lave\infty}}{V_\infty}\right)\Delta v_O[k] \tag{6.27}$$

Equation (6.26) is similar to (6.12) by taking steady state $\beta \equiv (E - r_L\hat{I}_{Lave\infty})/V_\infty$. Recursively computing Eq. (6.27) gives the following solution.

$$\Delta v_O[k] = \left(1 - \frac{T_s}{RC} + A\frac{L}{C}\frac{\hat{I}_{Lave\infty}}{V_\infty}\right)^k \Delta v_O[0] \tag{6.28}$$

System stability and convergence is assured when the multiplier of $\Delta v_O[0]$ in (6.28) is less than unity, because as $k \to \infty$ the error decays asymptotically to zero. Simulation results presented in Fig. 6.2 for voltage reference tracking and Fig. 6.3 for disturbance rejection show that A shorten settling time t_s and reduce voltage dip but not recovery time t_{rec}. Figure 6.2 show that shortening of settling time with higher A increases undesirable large output voltage overshoot. Voltage dip is decreased in Fig. 6.3 with large A with no appreciable shortening recovery time. These results are mathematically written in (6.25) and (6.27).

6.2.4 Stability with Parameter Variation

This section discusses the stability of the cNDB control system against converter parameter variations. It focuses on variations of inductance L and capacitance C during a steady state duty ratio $\Delta T_{2\infty}/T_s$.

Variation of Capacitance

Steady state output voltage according to (3.6) and (6.1)-(6.5) is

$$V_\infty = \left(1 - \frac{T_s}{RC}\right)V_\infty + \frac{1}{C}I_{L\infty}\Delta T_{2\infty}. \tag{6.29}$$

Variation of capacitance ΔC causes next sampling instant output voltage perturbation shown below.

$$V_\infty + \Delta v_O[k+1] = \left(1 - \frac{T_s}{R(C+\Delta C}\right)V_\infty + \left(\frac{1}{C+\Delta C}\right)I_{L\infty}\Delta T_{2\infty} \tag{6.30}$$

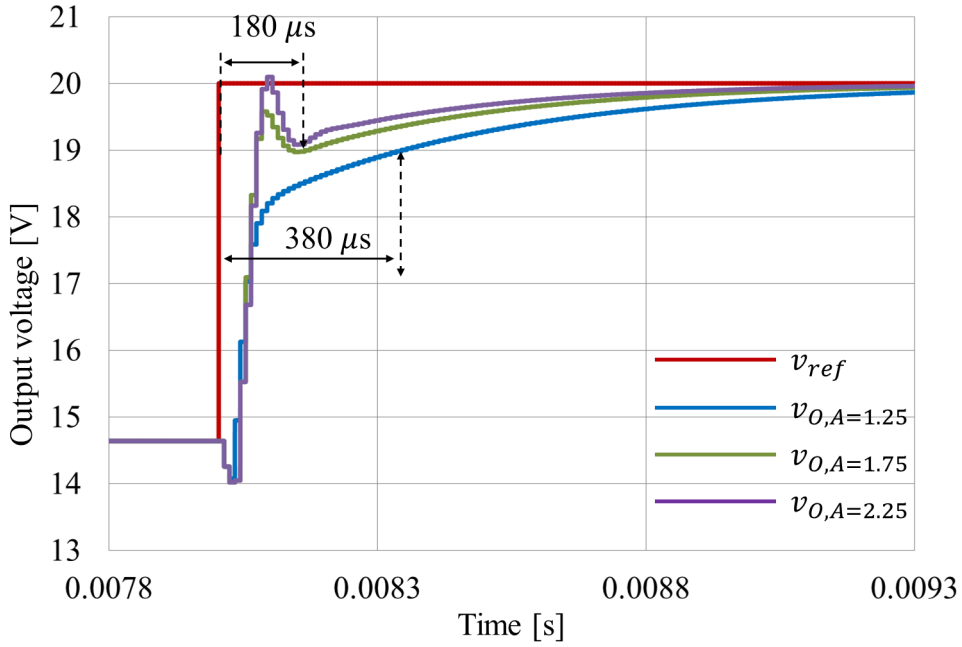


Figure 6.2: Output voltage response (simulation reference increase) with various gain A values.

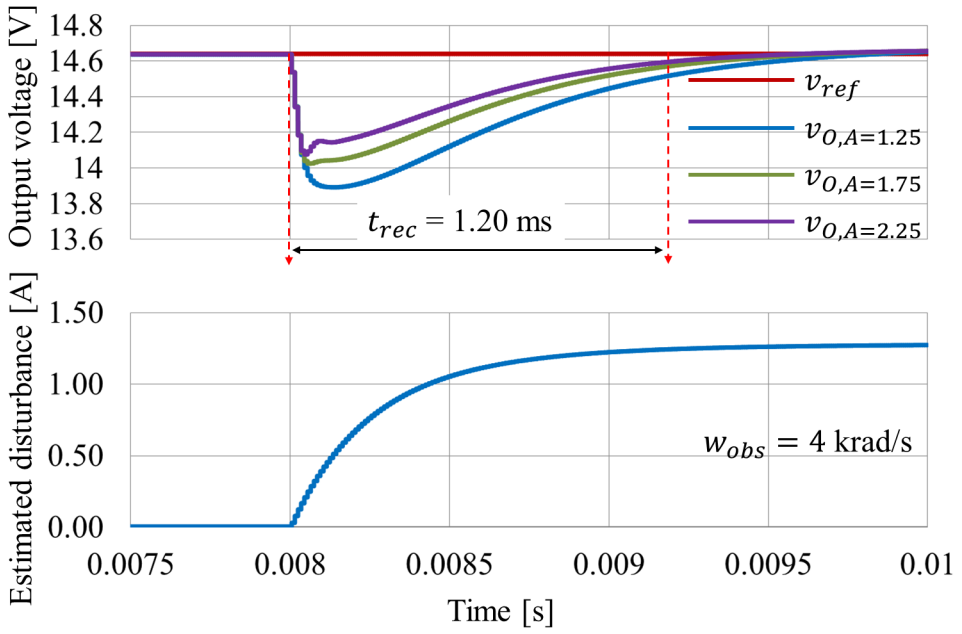


Figure 6.3: Output voltage response (simulation disturbance input) with various gain A values.

The voltage error is deduced by subtracting (6.29) from (6.30) to yield the following relation.

$$\Delta v_O[k+1] = \left(\frac{\Delta C}{C(C+\Delta C)}\right)\left(I_{L\infty}\Delta T_{2\infty} - \frac{V_\infty}{R}\right) \tag{6.31}$$

The theory of boost converter steady state suggests that $I_{L\infty}\Delta T_{2\infty} - V_\infty/R \approx 0$, therefore the voltage error approaches zero, i.e. $\Delta v_O[k+1] \approx 0$ even when there is capacitance variations.

Variation of Inductance

Steady state inductor current according to (3.7) and (6.1)-(6.5) is given by following relation.

$$I_{L\infty} = \left(1 - \frac{r_L}{L}T_s\right) I_{L\infty} - \frac{1}{L}V_\infty \Delta T_{2\infty} + \frac{E}{L}T_s \tag{6.32}$$

Due to environmental or other reasons, the inductance might change by ΔL and cause the following inductance current perturbation.

$$I_{L\infty} + \Delta i_L[k+1] = \left(1 - \frac{r_L T_s}{L+\Delta L}\right) I_{L\infty} - \left(\frac{V_\infty \Delta T_{2\infty} - ET_s}{L+\Delta L}\right) \tag{6.33}$$

The subtraction of (6.32) from (6.33) gives following inductance current error.

$$\Delta i_L[k+1] = \left(\frac{\Delta L}{L(L+\Delta L)}\right)(ET_s - I_{L\infty} r_L T_s - V_\infty \Delta T_{2\infty}) \tag{6.34}$$

Theoretically the term $ET_s - I_{L\infty} r_L T_s - V_\infty \Delta T_{2\infty} \approx 0$. Thus the current error asymptotically approaches zero, i.e. $\Delta i_L[k+1] \approx 0$ even when there is inductance variations.

6.2.5 Stability During Disturbance Input

In preceding section stability analysis was carried out while assuming disturbance current $i_d[k]$ is zero. This section discusses the stability during occurrence of disturbance since it causes voltage dip. We modify (6.7) i.e. $i_d[k] \neq 0$, use (6.9)-(6.10) and substitute into (3.6) to produce the variation of output voltage in (6.35).

$$V_\infty + \Delta v_O[k+1] = \left(1 - \frac{T_s}{RC}\right)(V_\infty + \Delta v_O[k]) + \frac{1}{C} i_L[k]\Delta T_2[k] - \frac{T_s}{C} i_d[k] \tag{6.35}$$

Figure 6.4 is part of the proposed cNDB control block diagram (lower left blocks of Fig. 3.5) which comprises disturbance and load observer, and nonlinear filter. Figure 6.4 is used to explain the stability during disturbance input. Sum of estimated load current and estimated disturbance $\hat{i}_A[k] = \hat{i}_A^*[k] + \hat{i}_d[k]$ (in Fig. 6.4), when divided by duty ratio $\Delta T_2[k]/T_s$ results into average

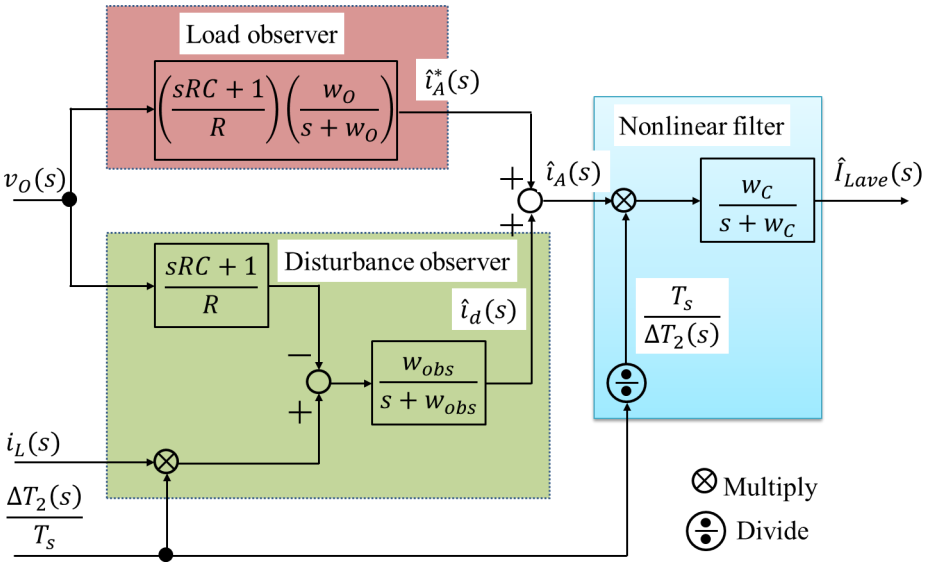


Figure 6.4: Part of Fig. 3.5 showing load, disturbance observer and nonlinear filter.

inductance current $\hat{I}_{Lave}[k]$ (in Fig. 6.4). Controller estimates the disturbance and adjusts the duty ratio such that the measured inductance current tracks the reference and average current in few sampling instants, as shown below.

$$i_L[k] \approx \hat{I}_{Lave}[k] = \left(\frac{\hat{i}_A^*[k] + \hat{i}_d[k]}{\Delta T_2[k]}\right) T_s \tag{6.36}$$

Substituting (6.36) into (6.35) above and after short calculation the following voltage error is obtained.

$$\Delta v_O[k+1] = \left(1 - \frac{T_s}{RC}\right) \Delta v_O[k] + \frac{T_s}{C}\left(\hat{i}_d[k] - i_d[k]\right) \tag{6.37}$$

Therefore disturbance is eliminated by the controller action through $\hat{i}_d[k] - i_d[k]$ of (6.37), as well as the voltage error decays asymptotically, also shown by Fig. 6.5. Previously in simulations of Fig. 5.5, Fig. 6.3 and experiments of Fig. 5.6 this disturbance elimination was observed. Even when load current was suddenly reduced/increased by 50% in Fig. 5.7-5.8 the voltage surge/dip was eliminated. Those results prove that with the implementation of the disturbance and load observer, the system is stable and robust against disturbances.

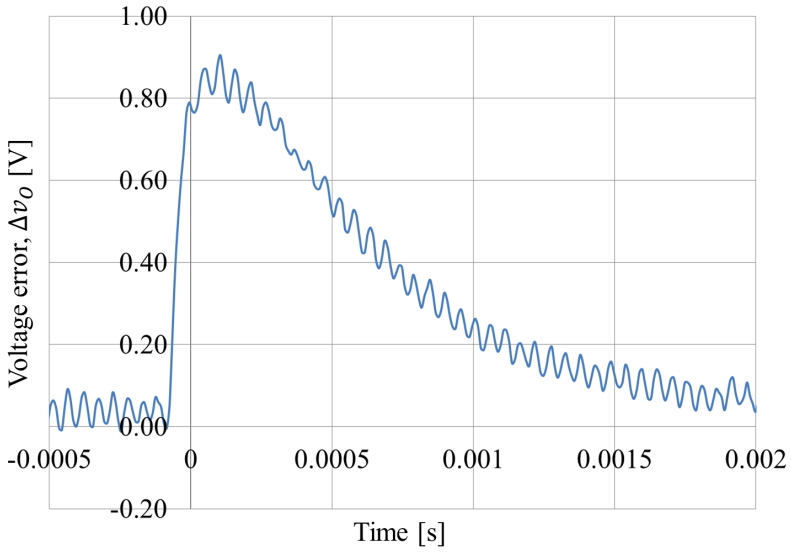


Figure 6.5: Voltage error when disturbance occurred (experiment).

6.3 Parameter Design

This section presents design of parameters for the proposed cNDB of Fig. 3.5, which are nonlinear reference current deadbeat controller gain A, load current observer cut off frequency w_O, disturbance observer cut off frequency w_{obs}, and nonlinear filter cut off frequency w_C.

6.3.1 Precise Design of Gain for Voltage Error Regulation

During the stability analysis in Section 6.2.3 it was shown that (6.28) gives the maximum limit of designing of gain A, and practically this gain cannot be lower than zero shown below.

$$0 < A < \frac{T_s}{RL}\frac{V_\infty}{I_{Lave\infty}} \tag{6.38}$$

Which is a trade off between output voltage overshoot, oscillations, fast settling time, and short recovery time to ensure asymptotic stability and voltage error elimination as well as less voltage surge/dip during disturbance event. Figures 6.2-6.3 demonstrate these characteristics.

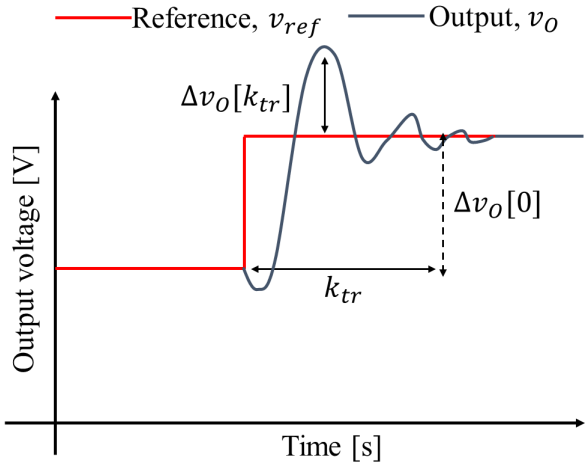


Figure 6.6: Overshoot and transient time.

6.3.2 Relation Between Gain for Voltage Error, Overshoot and Transient Time

Figure 6.6 is used to make short calculations with Eqs. (6.27)-(6.28) and (6.38) to arrive at the following relations.

$$\Delta v_O[k_{tr}] = \left(1 - \frac{T_s}{RC} + A_{tr}\frac{L}{C}\frac{I_{Lave\infty}}{V_\infty}\right)^{k_{tr}} \Delta v_O[0] \tag{6.39}$$

$$k_{tr} = \left|\frac{\ln \Delta v_O[k_{tr}] - \ln \Delta v_O[0]}{\ln\left(1 - \frac{T_s}{RC} + A_{tr}\frac{L}{C}\frac{I_{Lave\infty}}{V_\infty}\right)}\right| \tag{6.40}$$

Where k_{tr} is an integer multiple of sampling period T_s which covers the transient time for overshoot $\Delta v_O[k_{tr}]$. Initial voltage difference is represented by $\Delta v_O[0]$ and A_{tr} is the gain that causes overshoot in Fig. 6.6. Equation (6.39) shows that high gain A_{tr} increases output voltage overshoot $\Delta v_O[k_{tr}]$. At the same time Equation (6.40) shows that overshoot transient time k_{tr} reduces by increment of gain A_{tr}. Figure 6.2 has shown this characteristic.

6.3.3 Design of Filter Cut-Off Frequencies

The filters of the cNDB shown in Fig. 6.4 are designed in s domain in following explanations. In this figure the average inductance current $\hat{I}_{Lave}(s)$ is derived directly below.

$$\hat{I}_{Lave}(s) = Q_V(s)\frac{T_s}{\Delta T_2(s)}v_O(s) + Q_I(s)i_L(s) \tag{6.41}$$

Where the filters $Q_V(s)$ and $Q_I(s)$ are defined below in (6.40)-(6.41) showing they are functions of the cut off frequencies w_O, w_{obs} and w_C.

$$Q_V(s) = \frac{w_C\left(w_O - w_{obs}\right)\left(sRC+1\right)s}{R\left(s+w_C\right)\left(s+w_O\right)\left(s+w_{obs}\right)} \tag{6.42}$$

$$Q_I(s) = \frac{w_C w_{obs}}{\left(s+w_C\right)\left(s+w_{obs}\right)} \tag{6.43}$$

Around the equilibrium point the following s domain variations are introduced.

$$\hat{I}_{Lave}(s) = \hat{I}_{Lave\infty} + \Delta\hat{i}_{Lave}(s) \tag{6.44}$$

$$\Delta T_2(s) = \Delta T_{2\infty} + \delta(s) \tag{6.45}$$

$$v_O(s) = V_\infty + \Delta v_O(s) \tag{6.46}$$

$$i_L(s) = I_{L\infty} + \Delta i_L(s) \tag{6.47}$$

Variation from steady state duty ratio $\Delta T_{2\infty}$ of (6.45) is represented by $\delta(s)$, with the following approximation held to be valid.

$$\frac{1}{\Delta T_{2\infty}+\delta(s)} \equiv \frac{1}{\Delta T_{2\infty}}\left(1+\frac{\delta(s)}{\Delta T_{2\infty}}\right)^{-1} \approx \frac{1}{\Delta T_{2\infty}}\left(1-\frac{\delta(s)}{\Delta T_{2\infty}}\right) \tag{6.48}$$

Relationships (6.42)-(6.47) are substituted into (6.41), followed by separating low frequency terms from high frequency ones to give following relationships.

$$\hat{I}_{Lave\infty} = Q_V(s)\frac{T_s}{\Delta T_{2\infty}}V_\infty + Q_I(s)I_{L\infty} \tag{6.49}$$

$$\Delta\hat{i}_{Lave}(s) = Q_I(s)\Delta i_L(s) + Q_V(s)\frac{T_s}{\Delta T_{2\infty}}\left(\Delta v_O(s) - V_\infty\frac{\delta(s)}{\Delta T_{2\infty}}\right) \tag{6.50}$$

Note that $Q_V(s)$ is differentiating LPF while $Q_I(s)$ is LPF, thus with regards to (6.49) differentiating low frequency signal $(T_s/(\Delta T_{2\infty})V_\infty)$ produces zero and low pass filtering low frequency signal $(I_{L\infty})$ produces same signal thus $Q_V(s)$ and $Q_I(s)$ will change (6.49) into (6.51) which is the mentioned steady state similar to (6.8).

$$\hat{I}_{Lave\infty} \approx I_{L\infty} \tag{6.51}$$

Equation (6.50) was obtained after neglecting infinitesimal high frequency products. Therefore in (6.50) the second term can be made zero by appropriately selecting $w_O = w_{obs}$ thus

$$\Delta\hat{i}_{Lave}(s) = Q_I(s)\Delta i_L(s), \tag{6.52}$$

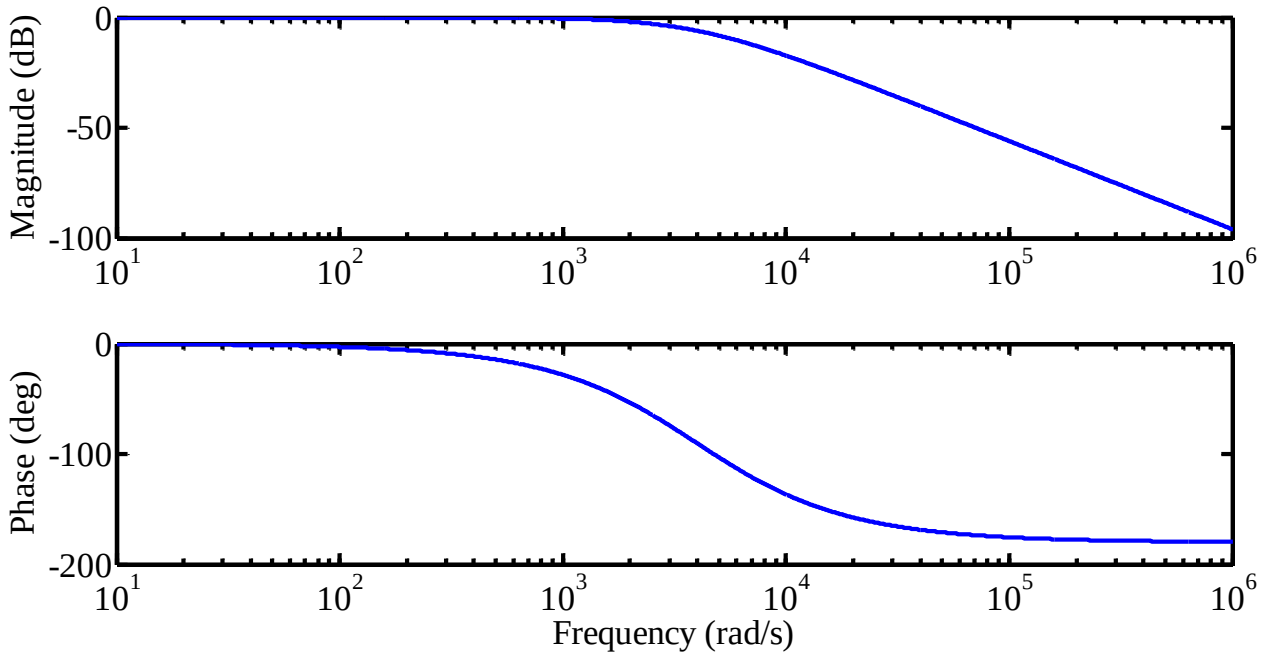


Figure 6.7: Bode plots of $Q_I(s)$ with experimental settings $w_C = w_O = w_{obs} = 4$ krad/s.

i.e. low pass filtered inductance current. Thus to show how these two filters ($Q_V(s)$ and $Q_I(s)$) behave in the experimental condition, bode plot of Fig. 6.7 shows $Q_I(s)$ attenuating the high frequency inductance current ($\Delta i_L(s)$) signal after the 3 dB at about 4 krad/s. Bode plot of Fig. 6.8 shows $Q_V(s)$ attenuating both magnitude and phase of the output voltage error signal ($\Delta v_O(s)$) and duty ratio ($\delta(s)/\Delta T_{2\infty}$), shown as very small magnitude close to zero (in linear scale) and zero phase.

6.4 Summary of Chapter Six

This chapter has discussed the reasons of nonlinear phenomena and oscillations observed in presented results of Chapter 5. Stability analysis was carried out and proved asymptotic stability with regards to different scenarios of the converter system, including inductance current deviations, voltage regulation gain limits, converter parameter variations, and disturbance input. Further controller parameters design was explained, where the gain A was designed based on the converter parameters and steady state condition. Frequency characteristics through bode diagrams showed that filters' cut off frequencies (poles i.e. w_O, w_{obs} and w_C) placement can be done so as to eliminate high frequency voltage and duty ratio error.

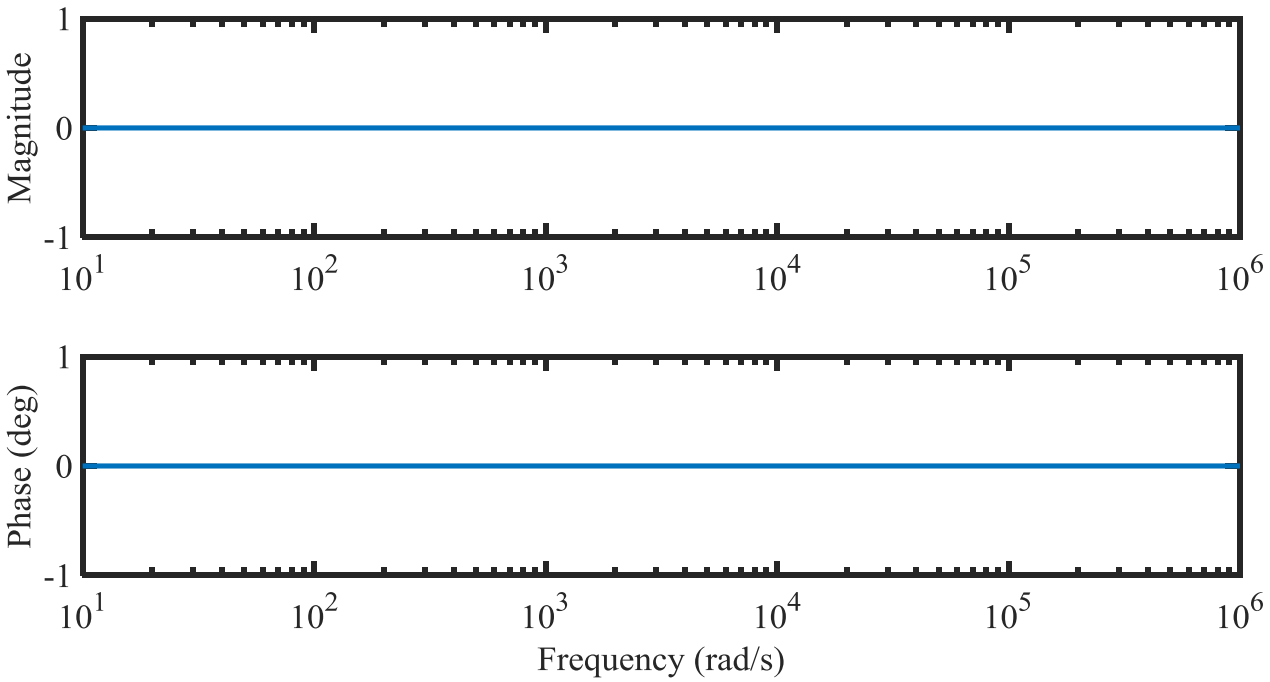


Figure 6.8: Bode plots of $Q_V(s)$ with experimental settings $w_C = w_O = w_{obs} = 4$ krad/s.

The voltage error regulation gain A (termed A_{tr} in (6.39) and (6.40)) was shown to influence both the decay rate and duration of the initial voltage error. This was shown by both simulation and experiment data.

Chapter 7

Conclusions

This thesis has achieved the following several contributions. We will discuss them and mention future research work direction.

7.1 Research Contributions

Firstly the research has developed the discrete time nonlinear state equations for a boost converter under CCM. Secondly it has used this modeling to develop nonlinear deadbeat control methods - namely voltage mode deadbeat control (vNDB) and current reference deadbeat control (cNDB) for a boost converter. The voltage mode deadbeat control was shown to be unstable and heavily parameter dependent. Therefore, a brief discussion was presented to show how it was sensitive to inductance value. Strong emphasis was instead focused on current mode deadbeat control.

Therefore, we mention the contributions of current mode deadbeat control. These contributions are the following. Firstly current reference is made of two terms, one of which is the output voltage regulation and the other is the estimated steady state inductance current. Secondly load disturbance observer is proposed and is added to the current reference term for load feedforward compensation. Experimentally a very quick reference voltage tracking was achieved among other literature while the disturbance recovery time is still in the reasonably quick range. After the verification by simulations and experiments, it was confirmed that under the conditions of input voltage 12 V, output voltage 20 V, the load resistor 4 Ω and 100 kHz sampling frequency, the voltage command tracking capability of 280 μs settling time was demonstrated together with 1.46 ms output voltage recovery time for a sudden unknown load change. When there was a sudden load decrease/increase by 50% the cNDB effectively eliminated the surge/dip voltage

within reasonable time ($t_{rec} \approx 1$ and $t_{rec} \approx 1.41$ ms). These data seems the best value among other digital control literature when compared.

Another contribution was stability confirmed by mathematical analysis and showed the control makes the system asymptotically stable for voltage perturbation, current perturbation, and robust during disturbance occurrence. The controllers robustness against converters parameter variation was confirmed mathematically. Controller parameters design was stipulated to be within the physical realization of the converter nominal parameters and can be extended to any application type boost converter. The simulation results were in excellent agreement to theory and experiment results, except for small differences in the oscillations observed between simulations and experiments. Those differences are attributed to two reasons. The first one is time delay of the switching device was not considered in the simulation. Second is the un-modeled nonlinear switching phenomena of the switching device.

7.2 Future Research Work

Proposal for future research work will be to develop precise account of the time delay of the switching device and include the un-modeled nonlinear switching phenomena of the switching device.

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Appendix A

List of Published Papers

This chapter mainly lists publications made during the Ph.D. study and others.

A.1 Journal Papers

A. Mushi, S. Nagai, H. Obara, and A. Kawamura, "Fast and robust nonlinear current reference deadbeat control for boost converter", IEEJ-IAS (2017).

A.2 Conference Papers

A. Mushi, S. Nagai, H. Obara, and A. Kawamura, "Design for nonlinear current reference deadbeat control for boost converter", IFEEC (2017).

A. Mushi, S. Nagai, and A. Kawamura, "Nonlinear deadbeat control for boost converter", SAMCON (2016).

A. Mushi, T. Nozaki, and A. Kawamura, "Proposal for faster disturbance rejection of boost DC-DC converter based on simplified current minor loop", IFEEC (2015).

Y. Watanabe, T. W. Kim, A. Mushi, and A. Kawamura, "Research on overall efficiency improvement of electric vehicle by MTHDPAM control method", EPE/PEMC (2012).

A.3 Other Conference

A. Thadei and A. Kyaruzi, "Surface resistivity of silicone rubber formulations tested in room ambient conditions: The case of silicone rubber with and without filler materials", ICRD (2008).

A.4 Unpublished Manuscripts

A. Mushi, S. Nagai, H. Obara and A. Kawamura, "Stability analysis and design for nonlinear reference current deadbeat control for boost converter," *Unpublished Manuscript*, Yokohama National University, Japan, 2017.

S. Nagai, A. Mushi, H. Obara and A. Kawamura, "Experimental verification of nonlinear deadbeat control for boost chopper and the sensitivity to inductor," *Unpublished Manuscript*, Yokohama National University, Japan, 2016.

Appendix B

Some Mathematical Derivations

Snapshot of mathematical derivations useful for the theories developed within the thesis are presented here.

B.1 Euler Method

Euler method is a first-order numerical procedure for solving ordinary differential equations (ODEs) when the initial value is known or can be guessed. Given an initial value problem (IVP)

$$y^{'}(t) = f(t, y(t)),\ y(t_0) = y(0) \tag{B.1}$$

where $y(t)$ is the curve to be estimated, $f(t, y(t))$ is the differential function, t is continous time, t_0 is the initial time, $y(t_0)$ and $y(0)$ represent the guessed or known initial value of the function. This curve can be estimated by selecting an enough small time step h such that

$$y[k+1] = y[k] + hf(k, y[k]) \tag{B.2}$$

$$h = \frac{t_k - t_0}{k} \tag{B.3}$$

Where t_k represent time at instant k. The value of $y[k]$ is an approximation of the solution of the ODE at time instant k.

B.2 Tustin Transformation

Tustin transform also known as trapezoidal rule maps the continous time domain s into discrete time domain z by following relation.

$$s \triangleq \frac{2}{T_s}\frac{z-1}{z+1}. \tag{B.4}$$

Using this transform s domain average inductance current $\hat{I}_{Lave}(s)$, estimated average load current $\hat{i}_A(s)$, and estimated disturbance $\hat{i}_d(s)$ were digitally implemented as following.

$$\begin{aligned} i_d[k] &= -i_d[k-1] + \left(\frac{\Delta T_2[k-1]}{T_s}\right) i_L[k-1] + \left(\frac{\Delta T_2[k]}{T_s}\right) i_L[k] \\ &\quad - \left(\frac{2R_nC_n + T_s}{R_nT_s}\right) v_O[k] + \left(\frac{2R_nC_n - T_s}{R_nT_s}\right) v_O[k-1] \end{aligned} \tag{B.5}$$

$$\hat{i}_d[k] = \left(\frac{2 - w_{obs}T_s}{2 + w_{obs}T_s}\right) \hat{i}_d[k-1] + \left(\frac{w_{obs}T_s}{2 + w_{obs}T_s}\right) (i_d[k-1] + i_d[k]) \tag{B.6}$$

$$i_A[k] = -i_A[k-1] - \left(\frac{2R_nC_n - T_s}{R_nT_s}\right) v_O[k-1] + \left(\frac{2R_nC_n + T_s}{R_nT_s}\right) v_O[k] \tag{B.7}$$

$$\begin{aligned} \hat{i}_A[k] &= \left(\frac{2 - w_OT_s}{2 + w_OT_s}\right) \hat{i}_A[k-1] + \left(\frac{w_OT_s}{2 + w_OT_s}\right) (i_A[k-1] + i_A[k]) \\ &\quad - \left(\frac{2 - w_OT_s}{2 + w_OT_s}\right) \hat{i}_d[k-1] + \hat{i}_d[k] \end{aligned} \tag{B.8}$$

$$\hat{I}_{Lave}[k] = \left(\frac{2 - w_CT_s}{2 + w_CT_s}\right) \hat{I}_{Lave}[k-1] + \left(\frac{w_CT_s^2}{2 + w_CT_s}\right) \left(\frac{\hat{i}_A[k-1]}{\Delta T_2[k-1]} + \frac{\hat{i}_A[k]}{\Delta T_2[k]}\right) \tag{B.9}$$