Doctoral Thesis

Current-Dependent Capacitor Voltage Control Technique for Parallel Autonomous Uninterruptible Power Supply Systems

並列自立無停電電源システムの電流依存型コンデンサ電圧制御方式

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by

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Abstract

The advancement in technology in the past few decades has resulted in greater dependency on electrical energy and the need to protect sophisticated equipment and important data. In the present day, high-technology devices are being used in houses, companies, industrial plants, and in many aspects of our daily lives. For this reason, disturbance in power networks has numerous impacts on out society.

Parallel uninterruptible power supply (UPS) modules have attracted considerable attention in the recent years. Paralleling of distributed energy sources is usually used to improve thermal management, reliability, redundancy, and for size reduction. Although the operation of inverters in parallel has many advantages, there are many challenges that need to be addressed in the system design stage in order to avoid problems that may lead to serious damage to the equipment. Some of these challenges include equal load distribution between energy sources. The load current should be distributed equally between the parallel converters, or proportional to their power ratings. Another constraint that is imposed by the paralleling process is that all parallel converters should have the same output voltage, frequency, and phase. Otherwise, large circulating current may flow between them.

Due to the above-mentioned challenges, and considering the ubiquity of distributed generation, control algorithms are imperative to ensure proper operation of modular UPS systems. Control schemes can be divided into two main categories, regarding the way of communication. The first method is based on active load-sharing (ALS), in which intercommunication among the UPS systems exists. Examples of this method include the average load sharing method, centralized control scheme, and master-slave control. All these methods are examples of communication-based control. Although these methods can achieve satisfactory performance in terms of load voltage regulation and current distribution, the existence of interconnections

between the modules puts limitations on the flexibility of the system and the physical locations of the modules, which adversely affects the reliability and expandability of the system due to the possibility of failure of communication links. As an alternative, another well-developed method discussed in the literature is the Droop method. This method is based on control of parallel distributed energy sources without exchanging information (also called independent control). The "droop" method is traditionally employed to mimic the performance of parallel generators. The control alters the frequency and voltage of each source as functions of its active and reactive power, respectively. However, this method achieves load sharing between energy sources with less accuracy and compromises the voltage and frequency of the system; additionally, it exhibits a slow transient response, and in case of non-linear load the harmonic currents are not equally distributed.

In contrast to the earlier development of control techniques for parallel inverters, we present a new, effective control scheme for parallel distributed generation systems. The proposed current-dependent capacitor voltage control (CCVC) scheme relies on controlling the capacitor voltage of the output LCL filter of the inverter to achieve autonomous control. The output current of each inverter is used to generate a reference capacitor voltage. The control does not require any information exchange between the inverters and relies only on local variables. Contrary to the widely used Droop control, the load voltage and frequency are constant in the proposed method. The validity of the proposed method has been verified by simulation and experimentally and the results are in good agreement with the theory.

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Chapter 1

Introduction

1.1 Background

The advancement in technology in the past few decades has resulted in more dependence on electrical energy and the need to protect sophisticated equipment and important data. In the present day, high-technology devices are ubiquitous and are being used in houses, companies, industrial plants, and in many aspects of our daily lives. For this reason, disturbance in power networks has numerous impacts on out societies. For example, estimates of the annual cost of power interruptions to U.S. electricity costumers is $79 billion [1].

The enormous number of sophisticated and sensitive devices connected to the network are vulnerable to the disturbance in the power system. There are various kinds of electrical disturbances that affect the electronic equipments. The IEEE Standards 1159-1959 and IEEE 1100-1994 provide references for the most common kinds of disturbances. Those include: transients (oscillatory/impulsive), sags (under-voltage), swell (over-voltage), waveform distortion (harmonics), voltage fluctuations, and frequency variations.

Disturbances in the power network can be caused by natural phenomena, such as lightning or bad weather conditions. Transmission line faults are another cause of disturbance. Faults in transmission lines can be symmetrical or unsymmetrical, such as three phase to ground and sin-

gle phase to ground, respectively. However, regardless of the cause and kind of disturbance, the effect could be serious, especially for sensitive equipments such as medical devices, computers, and other information technology and power electronic devices.

The Information Technology Industry Council (ITI) has published an application note which includes a curve representing the AC input voltage envelope that typically can be tolerated by most information technology equipment (ITE), without interruption in their functions. The curve has become a standard within the ITE industry and is usually referred to as ITI curve. The curve describes seven kinds of events in the steady state or transitory conditions. The following is a brief description of each event. All events are assumed to be mutually exclusive and may happen at any point in time:

1. Steady state tolerances: This range describes an RMS voltage which varies within the range of $\pm$ 10% from the nominal voltage. Any voltages in this range may be present for an indefinite period.

2. Line voltage swell: This region describes a voltage swell having an RMS amplitude of up to 120% of the RMS nominal voltage, with a duration of up to 0.5 seconds.

3. Low-Frequency Decaying Ringwave: This region describes a decaying ringwave transient. The frequency of this transient may range from 200 Hz to 5 KHz. The magnitude of the transient is expressed as a percentage of the peak 60 Hz nominal voltage (not the RMS value). The transient is assumed to be completely decayed by the end of the half-cycle in which it occurs.

4. High-Frequency Impulse and Ringwave: This region describes the transients which typically occur as a result of lightning strikes. Wave shapes applicable to this transient and general test conditions are described in ANSI/IEEE C62.41-1991. This region of the curve

deals with both amplitude and duration (energy), rather than RMS amplitude. The intent is to provide an 80 Joule minimum transient immunity.

5. Voltage Sags: Two different RMS voltage sags are described. Sags to 80% of nominal (maximum deviation of 20%) are assumed to have a typical duration of up to 10 seconds, and sags to 70% of nominal (maximum deviation of 30%) are assumed to have a duration of up to 0.5 seconds.

6. Dropout: A voltage dropout includes both severe RMS voltage sags and complete interruptions of the applied voltage, followed by immediate re-application of the nominal voltage. The interruption may last up to 20 milliseconds.

7. No Damage Region: Events in this region include sags and dropouts which are more severe than those specified in the preceding paragraphs, and continuously applied voltages which are less than the lower limit of the steady-state tolerance range. The normal functional state of the ITE is not typically expected during these conditions, but no damage to the ITE should result.

8. Prohibited Region This region includes any surge or swell which exceeds the upper limit of the envelope. If ITE is subjected to such conditions, damage to the ITE may result.

In an attempt to increase the quality and reliability of electric power, distributed generation (DG) offers an attractive new paradigm of power grids [2]. The concept of distributed generation is particularly important in microgrids. In microgrids, small DG plants and dispersed energy storage devices are integrated into the network, offering many advantages. Microgrids can incorporate different kinds of power generation units, including both conventional and renewable sources such as photovoltaic (PV) panels, wind farms, thermal power plants, fuel cells, and other sources.

The global electrical energy consumption is rising and there is a steady demand to increase power capacity. The increasing power demand necessitates efficient generation, distribution, and consumption of electrical energy. Conventional power systems rely on a large central power generation unit to meet the ever-increasing users demand. The bulk power generator is the only power source the users can receive energy from. Due to the enormous uncertainty and lack of feedback signals from the users, the amount of power demand cannot be accurately known at any given instant of time. Hence, traditional power generation systems relied on over-provisioning and excess capacity of power in order to guarantee service reliability [3]. Traditional power systems generate more power than the actual demand and deplete fossil fuel resources, hence it is an inefficient and an environmentally harmful system.

1.2 Motivation

Parallel UPS (Uninterruptible Power Supply) modules have attracted considerable attention in the recent years. Paralleling of distributed energy sources is usually used to improve thermal management, reliability, redundancy, and for size reduction [4]. Although the operation of inverters in parallel has many advantages, there are many challenges that need to be addressed in the system design stage in order to avoid problems that may lead to serious damage to the equipment. Some of these challenges include equal load distribution between energy sources. The load current should be distributed equally between the parallel converters, or proportional to their power ratings [5]. Another constraint that is imposed by the paralleling process is that all parallel converters should have the same output voltage, frequency, and phase. Otherwise, large circulating current may flow between them [5, 6, 7]. The circulating current is particularly dangerous at light-load condition, since inverters operate in rectification mode and absorb active power. This results in increase in the dc capacitors voltage and possibly damages the capacitors [4].

Due to the above-mentioned challenges, and considering the ubiquity of distributed generation, control algorithms are imperative to ensure proper operation of modular UPS systems. Control schemes can be divided into two main categories, regarding the way of communication [4, 5]: The first method is based on active load-sharing (ALS), in which intercommunication among the UPS systems exists. Examples of this method include the average load sharing method, in which the currents of all parallel modules is averaged and this average value becomes the reference to all modules so that they provide equal current [5]. The centralized control scheme is another control method in this category. The method depends on a central control unit which, based on the feedback from parallel units, calculates and sends reference commands to all units [8]. Another communication-based method is the master-slave control technique; the master unit usually regulates the output voltage and the slave units operate as current sources [9]. All these methods (and others) are examples of communication-based control.

Although these methods can achieve satisfactory performance in terms of load voltage regulation and current distribution, the existence of interconnections between the modules puts limitations on the flexibility of the system and the physical locations of the modules, which adversely affects the reliability and expandability of the system due to the possibility of failure of communication links [4, 5].

As an alternative, another well-developed method discussed in the literature is the Droop method [10]. This method is based on control of parallel distributed energy sources without exchanging information (also called independent control). The "droop" method is traditionally employed to mimic the performance of parallel generators. The control alters the frequency and voltage of each source as functions of its active and reactive power, respectively. However, this method achieves load sharing between energy sources with less accuracy and compromises the voltage and frequency of the system; additionally, it exhibits a slow transient response, and in

case of non-linear load, the harmonic currents are not equally distributed [4, 5, 10].

Many attempts have been made recently to improve the accuracy of the conventional droop method. For example, in [11], the reactive power sharing accuracy has been improved by changing the voltage bias on the basis of the conventional droop control, which is activated by a sequence of synchronization events through a low-bandwidth communication network. In reference [12] information about output reactive power is injected into the output voltage reference of each unit. The output reactive power is regulated to improve the accuracy of power sharing. However, these two methods require a low-bandwidth communication network to synchronize the parallel units, which affects the stability of the system. In reference [13], three regulators are used: voltage, reactive power, and active power regulators. Each controller processes its local and neighbours information to update its voltage magnitude and frequency. The system utilizes a sparse communication network across the network to exchange information. Moreover, the structure of the control system with three levels increases the complexity of the system. Reference [14] employs a direct flux control algorithm to regulate the virtual flux according to droop controller. The method achieves power sharing with lower frequency deviation than conventional droop, but does not seem to reduce the voltage deviation.

Although the mentioned methods improved the traditional droop method, the trade-off between power sharing, complexity of the system, and regulation of frequency, voltage, and phase seems to always be present [5, 15]. Han *et al.* [15] did a comprehensive review of the state of the art control schemes and concluded that it is difficult for one control scheme to overcome all the drawbacks for all applications. In contrast, the authors in references[16, 17] proposed a different approach for parallel distributed control for three phase and single phase VSIs, in which the system only receives a reference signal from a communication bus, but does not exchange any information between the parallel modules.

In contrast to the earlier development of control techniques for parallel inverters, we present a

new, effective control scheme for parallel distributed generation systems. The proposed current-dependent capacitor voltage control (ccvc) scheme relies on controlling the capacitor voltage of the output LCL filter of the inverter to achieve autonomous control. The output current of each inverter is used to generate a reference capacitor voltage. The control does not require any information exchange between the inverters and relies only on local variables. Contrary to the widely used Droop control, the load voltage and frequency are constant.

1.3 Objectives

The main objectives of this dissertation are as follows:

1. Development of an autonomous control technique for power distribution between parallel inverters.

2. Development of a communication-based technique for power distribution between parallel inverters.

3. Verification of the proposed control schemes by simulation tools and experiments.

1.4 Organization of the Thesis

The present chapter aims at introducing the motivation and applications of the results presented in this dissertation. Before introducing the main contribution of this thesis, a useful introduction of some main concepts related to three phase inverters and UPS systems and their control techniques is presented. The dissertation is organized into the following chapters:

- Chapter 2 introduces the main structure and types of UPS systems. Discussion of distributed generation and the conditions required for parallel operation of inverters is also

provided. The main control techniques available in the open literature are presented along with a brief description of each method.

- Chapter 3 discusses the main principles of three phase inverters and the average model of the inverter in the dq synchronous frame. A useful introduction about phase locked loop (PLL) systems and the transformation of three phase variables to dc synchronous quantities is also available. Moreover, resonance damping techniques of output filters, such as multi-loop control and the virtual impedance concept are presented.

- In Chapter 4 a communication-based control technique for parallel UPS and DG sources is presented. The control technique relies on exchanging information between the power sources to achieve proper load current distribution. Stability analysis and simulation results are available.

- The main contribution of the dissertation is in Chapter 5. An autonomous control technique which can achieve load current distribution between parallel inverters is presented here. The new control techniques is callel current-dependent capacitor voltage control technique (CCVC). Stability analysis and simulation results are presented.

- Chapter 6 presents the experimental setup used to verify the validity of the proposed control methods. The two proposed control techniques in Chapter 4 and Chapter 5 are verified experimentally using a system of two parallel inverters under different load conditions, including no-load condition, step-load condition, and non-linear load condition.

- Chapter 7 summarizes the dissertation and suggests future research prospects.

Chapter 2

Uninterruptible Power Supply Systems Configuration and Control Strategies

In this chapter, the basic types of UPS systems and their construction is provided. As will be explained later, the choice of the UPS depends on the application. A brief review of the main energy storage devices is also included, since the battery is an important component of the UPS system that is used to supply power to the load in case of failure in the main power supply. The Chapter also provides mathematical equations for calculating the circulating current between parallel inverters. Finally, the basic control strategies used in the literature today are introduced. Ultimately, the goal of this chapter is to establish the fundamentals of UPS systems and control of parallel inverters.

2.1 Introduction

The UPS technology has been around for a long time, and many kinds of configurations have been developed. On the basic level, there are two kinds of UPS systems: static and dynamic (or rotary). Both kinds are explained in this chapter along with their different configurations and applications.

While a UPS system can protect sensitive devices and prevent data loss, the battery run-time is usually short and can last only for a few minutes for most UPS systems. When the main power fails, a backup generator is usually activated and the UPS supplies energy until the backup system is ready to take over [4]. To avoid interruption in the system due to the switching from the normal mode (where main power is available) to the emergency mode (where the battery is used), some industrial systems use on-line UPS systems. In this case, the power is always supplied through the UPS unit, even when the main power is available. To further increase the reliability, many units are connected in parallel.

Connecting inverters in parallel is an inherently challenging problem that requires advanced control techniques. For parallel inverters, and similar to parallel generators, all units must have the same voltage level, frequency, and phase. To tackle this problem, many control techniques are proposed. Although it is difficult to develop an ideal control scheme, the drawbacks can be minimized by the careful choice of the control technique depending on the application.

2.2 UPS Structure and Types

The fundamental structure of a UPS system is shown in Fig. 2-1. There are three main elements in every UPS system, as follows:

- Energy storage element: necessary to supply power to the load in the event of grid failure until the emergency generator is activated.
- AC/DC converter (rectifier): used to convert the ac voltage at the input to dc voltage in order to charge the battery.
- DC/AC converter (inverter): used to convert the dc voltage again to controlled ac voltage.

At the output of the inverter, a filter is connected to mitigate the high frequency harmonics generated by the switching action at the inverter. Moreover, a bypass switch is connected

in parallel to the UPS. This switch is used for UPS maintenance reasons. Furthermore, the reliability of a single UPS unit is significantly increased with the addition of the bypass switch [18].

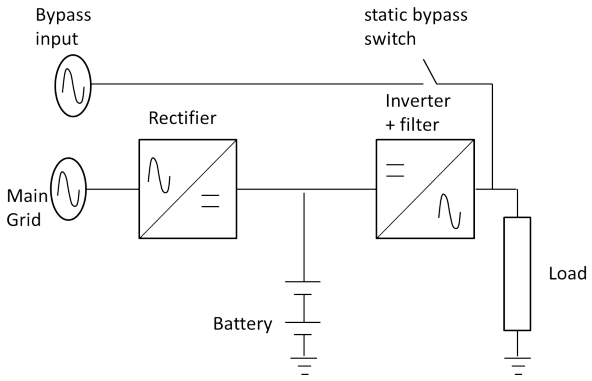


Figure 2-1: Fundamental structure of a single UPS with bypass switch.

2.2.1 Types of UPS Systems

The necessity of uninterruptible power supply (UPS) systems has been discussed in Chapter 1; public utility grids encounter many kinds of problems that may not be tolerated by many equipment. UPS provides instantaneous protection from power interruptions of the main grid. There are mainly two classifications of UPS systems, static and dynamic. A static UPS relies on power electronic converter with semiconductor devices. A rotary (or dynamic) UPS system, on the other hand, uses the inertia of a high-mass flywheel to deliver power to the load for a short period in case of power loss from the main utility. The main configuration of a rotary UPS is shown in Fig. 2-2. The operation principle is simple: A motor is connected to the main grid and its shaft is connected to a high-mass flywheel. A generator is connected to the flywheel and the load is connected to the output of the generator. The high inertia of the flywheel makes it possible to supply power for a short time (ride-through time). In case of power disturbances, the inertia of the flywheels maintains power for several seconds which is enough to activate a stand-by generator [4].

Rotary UPS systems have been used in the industry for a long time and they are reliable. However, the drawbacks of this system is the loss in the motor-generator combination. Other drawbacks include the noise and the requirement of maintenance [19].

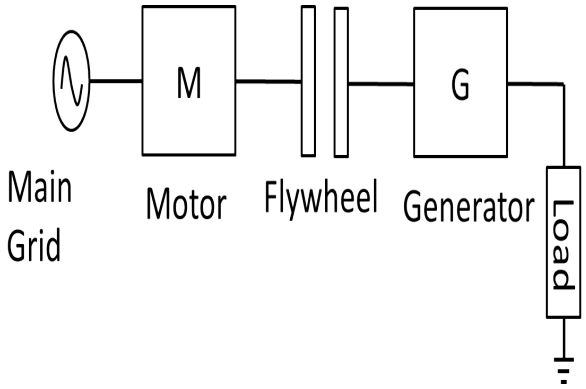


Figure 2-2: Block diagram of a typical rotary UPS.

The fast development of semiconductor materials such as insulated-gate bipolar transistor (IGBT) allowed the operation of switching power electronic devices at high frequency. This advancement paved the way to develop static UPS systems based on power electronic devices. A static UPS unit consists of a dc power source (battery set, supercapacitor, fuel cell, PV cell, etc), a dc/ac inverter, and a filter. An inverter consists of a combination of switching semiconductor devices (IGBT, MOSFET, etc) that convert the dc voltage to ac voltage. The ac voltage contains high-frequency harmonics which are filtered out by the output filter of the UPS. Due to the advancement in power semiconductor electronic devices, it is possible to reach high switching frequencies. Static UPS systems have fast transient response and low total harmonic distortion (THD) in output voltage and current [4, 19]. For these reasons, static UPS systems are the most common type nowadays. Their practical applications range from low power devices, such as personal computers and telecommunication devices, to medium range systems such as medical systems and sensitive equipments at hospitals, to high power systems such as utility systems and microgrids. Microgrids are small scale power systems that are designed to operate independent of the main utility (stand alone), or parallel to the main grid. They

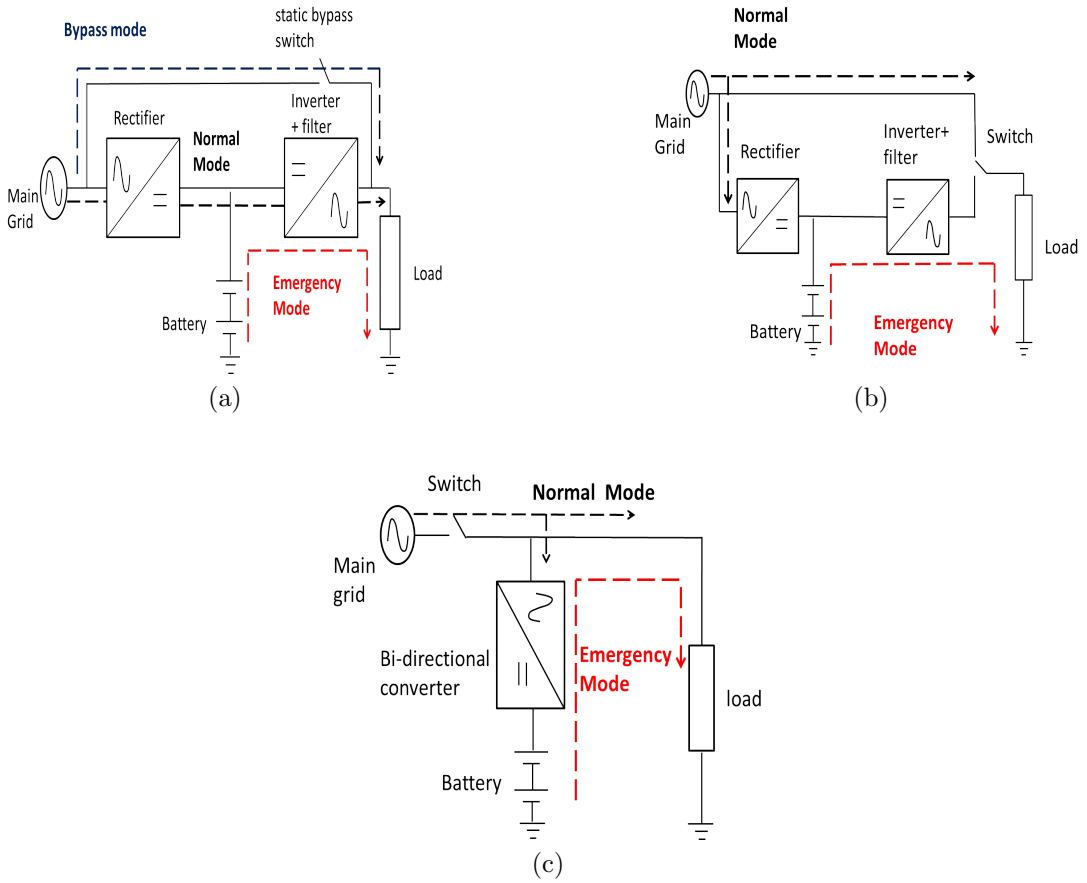


Figure 2-3: Three circuit configurations of UPS systems: a) online UPS, b) offline UPS, and c) line interactive UPS.

integrate storage unit, distributed energy sources, and possibly different kinds of renewable energy sources [13]. It is important to provide the microgrid with reliable, high quality power.

There are mainly three kinds of static UPS systems in terms of circuit configuration. Each type has advantages and disadvantages, the choice of a particular configuration depends on the application itself.

1. On-line UPS (double conversion, or inverter-preferred):

   Fig. 2-3a shows the configuration of this type. The power flows through the rectifier and the inverter (hence the name double conversion). The rectifier also continuously charges the batteries. The power rating of the rectifier should be more than 100% of the load demand, as well as the power power required to charge the batteries. If the main power

fails, the batteries supply power to the load through the inverter. In case of overload or maintenance, the main grid can be connected in parallel to the inverter after synchronizing the phase of the inverter with the phase of the grid voltage.

This is the most reliable UPS configuration since it provides total independancy between the input and output voltage in terms of amplitude and frequency, and therefore a high quality output voltage can be obtained. Moreover, the batteries are always charged and ready to supply power in case of emergencies. There is no transfer time during the transition from normal to stored energy mode. Most of the commercial UPS units of 5 kVA power and above are online [4]. However, due to the existence of two converters, the efficiency of the system is limited. Typical efficiency of online UPS systems is 94%. In addition, the THD of the input current is relatively high due to the existence of the rectifier. Another disadvantage of this topology is the low input power factor [19]. A power factor correction (PFC) circuit can be added at the input to solve this problem, but this adds to the total cost of the system.

2. Off-line UPS (standby or line-preferred):

   The configuration of an off-line UPS is shown in Fig. 2-3b. Similar to on-line UPS systems, the off-line UPS consists of a battery set, a rectifier, an inverter, and a switch. In normal operation mode, the switch connects the main grid directly to the load while at the same time charges the batteries. During abnormal conditions of the grid, the switch connects the load to the inverter and the power flows from the battery. The transition time is typically less than 10 ms which can be tolerated by computers. This configuration is suitable for home applications and are commonly rated at 600 VA.

   The fact that the main power grid is connected directly to the load in the normal mode means that there is no power conditioning. Unlike the on-line UPS, the rated power of

the rectifier in off-line systems should be equal only to the power required to charge the battery set because it is not connected directly to the load. This results in lower cost compared to on-line systems [19]. The rated power of the inverter is 100% of the load demand.

The main advantages of this configuration are the low cost, simple design, and small size. The main disadvantages are the lack of isolation between the main utility and load in normal load, switching time between normal mode and emergency mode, and poor performance with nonlinear loads [19].

3. Line-interactive UPS:

Fig. 2-3c shows the circuit diagram of the line-interactive UPS. It consists of a single bi-directional converter which operates as a rectifier in normal mode to charge the battery, and as an inverter in case of disturbances in the main grid to supply power from the battery to the load.

This configuration is considered as a midway between on-line and off-line UPS systems [4]. Since there is only one converter in this configuration, the efficiency is higher than double-conversion UPS systems. Other advantages of this UPS is the simplicity and low cost in comparison to on-line UPS systems. Typically, line interactive systems use a voltage regulator to step up or down the mains voltage. Thus, long-term over voltage and under voltage can be corrected without the need to switch to emergency mode and drain the battery, which extends the lifetime of the battery set.

However, this configuration lacks effective isolation between the grid line and the load. Therefore, it is not possible to regulate the output frequency. Typical power rating of this type is between 0.5 kVA and 5 kVA for small server systems [4], and typical efficiency is 97%.

The main advantages and disadvantages of each UPS configuration are summarised in Table 2.1.

Table 2.1: Specifications of one inverter unit.

Configuration	Advantages	Disadvantages
On-line	• No transfer time from normal mode to emergency mode. • High tolerance to input voltage distortion. • Precise control of output voltage.	• High THD at the input. • Low input power factor (requires power factor correction circuit). • Low efficiency.
Off-line	• Low cost	• Lack of isolation of the load from the main grid. • No output voltage regulation. • Existence of transient time between modes. • Poor performance with non-linear loads.
Line-interactive	• Lower cost compared to on-line UPS. • Good harmonic suppression to input current. • High efficiency.	• Lack of isolation of the load from the main grid. • Poor voltage conditioning.

2.2.2 Energy Storage Systems

One of the important features of UPS systems is the ability to store energy. High-capacity storage facilities are traditionally based on hydropower technology [20]. Water from a lake or a river is transferred using pumping systems to an artificial lake on a high place. The motor-driven turbines for pumping water use inexpensive utility energy at night and discharge during periods of peak load by reversing the turbines to operate as generators [21]. Although these systems have high storage capacity (the equivalent of hundreds of megawatt-hours of energy) and are relatively inexpensive, finding a feasible site to install such systems is becoming difficult [21]. Hence, the focus has shifted to other forms of energy storage systems. One of the candidates is electrochemical solutions for storage of renewable energy. However, due to the limitations on

the life cycles of such systems, many alternative solutions have been presented. Reference [20] presented a comparison of different storage systems and their energy efficiency and life cycles as shown in Table 2.2.

Table 2.2: Different types of energy storage systems and their life cycles and efficiencies [20].

Storage system	Life time [cycles]	Efficiency [%]
Pumped hydro	75 Years	70-80
compressed air	40 Years	-
Flow batteries	1500-2500	75-85
Metal-air	100-200	50
Sodiumsulfur battery (NAS)	2000-3000	89
Lead-acid	200-300	75
Super capacitors	10000-100000	93-98

The traditional water-pumped systems have large capacities and long life time. Modern energy storage systems such as supercapacitors, on the other hand, have a large number of large cycles but the stored energy is limited. From the table, it is evident that the electrochemical batteries have a limited performance in terms of the number of life cycles. This section summarizes some of the energy storage systems used today.

Battery Energy Storage System (BESS)

Typical UPS systems consist of chemical rechargeable batteries, such as lead-acid and nickel-cadmium (Ni-Cd) due to their availability and reliability [4]. Other kinds of batteries are sodium-sulfur (NAS), Zinc-Bromine, and Lithium-Air batteries. Flow batteries (regenerative fuel cells) are also demonstrating technical feasibility [21]. Flow batteries include many types, such as [4]: polysulfide bromide (PSB), vanadium redox (VRB), zinc bromine (ZnBr), and hydrogen bromine (H-Br) batteries. However, batteries contain toxic heavy metals such as cadmium, mercury, and lead and may cause environmental problems if they are not discarded in a proper way [22].

Flywheels

This storage system relies on using the kinetic energy of a rotating wheel as an electricity storage medium. When the main power is present, it is used to spin the flywheel at a certain speed until the main power is cut. The stored energy is then used to operate a generator and feed the load until the emergency generator is activated. Typically, flywheels provide a fly-through time between 1 s and 30 s. For commercial UPS applications, lower-speed flywheels running under 10,000 rpm with steel rotors have been used in applications up to several megawatts. High-speed flywheels operating at speeds 40,000-60,000 rpm with carbon fiber rotors and magnetic bearings are also available in the market [4]. In some cases, flywheels are used as short-term energy supplies coupled with lead-acid batteries [21].

Fuel Cells

Fuel Cells (FCs) are static energy conversion devices that convert the chemical energy of fuel directly into electrical energy. They have many advantages compared to conventional power plants, such as high efficiency, low emission of pollutant gases, and flexible modular structure [23]. Additionally, unlike photovoltaic and wind generation systems, they have no geographic limitations and can be places at any place. However, due to their slow internal electrochemical and thermodynamic characteristics, they cannot respond quickly to to load transients [4, 23]. This problem can be solved by using supercapacitors or BESS in order to improve the dynamic response of the system.

There are many kinds of FCs. For example, Proton exchange membrane FCs (PEMFCs), solid oxide FCs (SOFCs), and molten carbonate FCs (MCFCs) [23]. PEMFCs are suitable for UPS applications due to their compact light weight and room temperature operating range. While SOFCs and MCFCs require operating temperature of around 800°C-1000°C [4].

Supercapacitors

Supercapacitors use a different mechanism to store energy than batteries. While batteries store energy as a form of chemical energy, supercapacitors store the energy electrostatically on the surface of its plates and does not involve chemical reactions. Supercapacitors have high power densities, long life time and low maintenance. They are available typically in the range of hundreds of Farads with low voltages (about 3 V) [4].

Compressed Air Energy Storage (CAES)

CAES is a method that uses mechanical-hydraulic conversion (also called liquid-piston principle), to store energy at one time and use it at another [4]. The advantage of this system is that it does not generate any waste. CAES can be combined with other energy storage systems to optimize their performance and efficiency.

2.3 Distributed UPS Systems

UPS systems in many cases are not only desirable, but also a requirement. To further increase the reliability of the system, UPS units are often connected in parallel. Fig. 2-4 shows the block diagram of on-line distributed UPS system. Distributed UPS systems can also be line-interactive.

This approach offers many advantages compared to a single centralized UPS unit, such as [4]:

- Flexibility to increase the power capability of the system: In case of a centralized system, a single UPS unit supplies the power demand of the load. If the power demand increases beyond the rated power of the UPS, the unit have to replaced with one that has a higher power rating. On the other hand, UPS units can easily be connected in parallel to meet

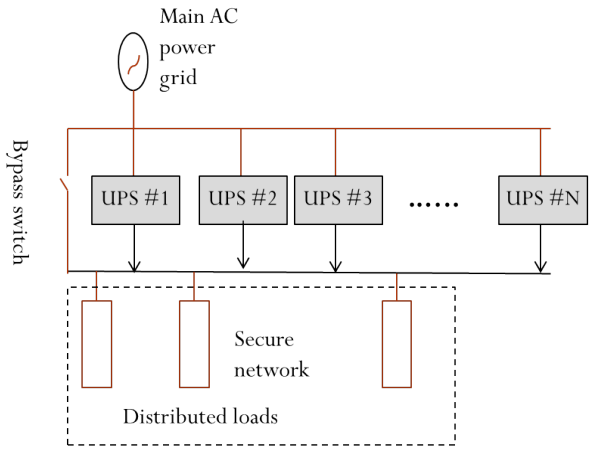


Figure 2-4: Block diagram of distributed UPS systems.

the power demand of the load in case of distributed approach.

- Reliability and Redundancy (*N+1* or *N+X*): Distributed UPS systems are highly reliable and have higher tolerance to faults compared to centralized systems. In case of fault of one unit, the other units can share the load of the malfunctioning unit without disturbing the system. *N+1* or *N+X* redundancy adds immense advantage to the system. In this case, N UPS units supply the load, and 1 or X units stay in reserve. If one or more (X) of the units are damaged or disconnected, this/these units can automatically be connected to supply the power of that unit. The redundancy can reduce the single point failure. A parallel redundant system can typically provide up to 99.99% availability, which means that the system does not operate for less than 1 h/year [5].

- Ease of maintenance: Due to the redundant configuration of distributed UPS systems, it is easier to perform maintenance on the system.

- Size reduction and thermal management.

- Reduced repair and replacement cost of each failure [26].

According to [26], the installation cost of inverters is a constant value, regardless of the

number of parallel units N. However, the choice of N is related to the system reliability index. The reliability of the system influences the operational cost, including cost of power losses, maintenance and repair cost, and downtime cost [26]. It has been shown that increasing the number of redundant units X beyond a certain value will not increase the reliability of the system. The mean time between failures (MTBF) is often used as a reliability index [26, 18]. MTBF provides a prediction of the elapsed time between failures of a system during operation due to the inherent imperfections in the system components. MTBF is related to the failure rate of the system (λ), which is the frequency with which a system fails and is expressed in failures per unit of time.

$$MTBF = \frac{1}{\lambda}. \tag{2.1}$$

It is shown in [26], MTBF of PV module is 552 years. On the other hand, MTBF of an inverter system is usually one to ten years. Therefore, the key to increase the reliability of inverter systems is the careful choice of the number of redundant UPS units and the reduction of common elements (such as common control unit, common reference oscillator, etc.).

Paralleling of UPS systems is a challenging problem that requires robust control techniques. The control strategies of current sharing have to be fast and precise because of the fast dynamic response of static UPS systems and their low overload limits. Paralleling of UPS systems is more complex than paralleling dc sources, since every module must share the load properly while staying synchronized. Under ideal conditions, the load can be shared equally if every UPS unit has the same output voltage, frequency, and phase. However, in practical situation there might exist some differences between the units and mismatch in line impedances. These differences may cause circulating current between the parallel modules, as shown in Fig. 2-5 [5, 6].

Circulating current is dangerous and could be damaging especially under light load or no-

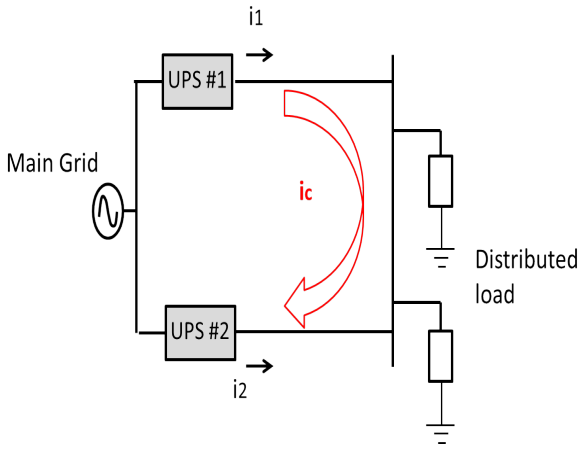


Figure 2-5: Circulating current between two parallel UPS units.

load conditions. In Fig. 2-5 the circulating current (i_c) flows from UPS 1 to UPS 2. This may cause UPS 2 to absorb active power and operate in rectification mode, resulting in increase in the dc voltage and possibly damages the dc capacitors.

To avoid the possible consequences of circulating currents, generally, a distributed UPS system should achieve the following features [5]:

1. All parallel UPS modules must have the same output voltage, frequency, and phase.

2. Equal current sharing between the modules, or current sharing proportional to the power their relative power ratings.

3. Flexibility to increase the number of parallel units in case of increase of power demand of the load.

4. Plug-and-play operation capability (also known as hot swap capability).

2.4 Parallel inverters and circulating current

Fig. 2-6 shows the circuit diagram of n parallel-connected ac voltage sources (E_1, E_2,...,E_n). And suppose that the output impedance of each voltage source is Z, and Z_L is the impedance

of the load.

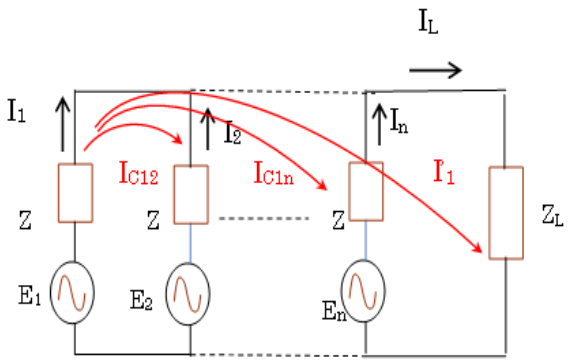


Figure 2-6: Circulating current components between n parallel inverters.

Each source supplies part of the load current. For source 1, this current is I_1'. The circulating current components between this source and other parallel sources are I_{c12}, I_{c13}, ..., I_{c1n} [?]. These current components of source 1 are shown in Fig. 2-6. The following equations show the details of output currents from each inverter:

$$\begin{cases} I_1 = I_{c12} + I_{c13} + ... + I_{c1n} + I_1' \\ I_2 = -I_{c12} + I_{c23} + ... + I_{c2n} + I_2' \\ I_3 = -I_{c13} - I_{c23} + I_{c34} + ... + I_{c3n} + I_3' \\ I_n = -I_{c1n} - I_{c2n} - I_{c3n} - ... - I_{c(n-1)n} + I_n' \end{cases} \tag{2.2}$$

where I_{cij} is the circulating current from unit i to unit j, and I_i' is the load-current component from unit i.

The circulating current components of each unit can be lumped into a single term, and (2.2) is alternatively written as:

$$\begin{cases} I_1 = I_{c1} + I_1^{'} \\ I_2 = I_{c2} + I_2^{'} \\ I_3 = I_{c3} + I_3^{'} \\ I_n = I_{cn} + I_n^{'}. \end{cases} \tag{2.3}$$

Notice that the load current (I_L), which is equal to the summation of all individual currents from the parallel units, will include only the summation of the last terms in (2.3) since the circulating current components will cancel each other out.

$$I_L = I_1 + I_2 + ... + I_n = I_1^{'} + I_2^{'} + ... + I_n^{'}. \tag{2.4}$$

Applying KVL to the circuit in Fig.2-6:

$$\begin{cases} E_1 = ZI_1 + Z_L I_L \\ E_2 = ZI_2 + Z_L I_L \\ E_3 = ZI_3 + Z_L I_L \\ E_n = ZI_n + Z_L I_L, . \end{cases} \tag{2.5}$$

Applying the superposition principle to the circuit in Fig. 2-6 by taking each voltage source individually and calculating the equivalent current, the total current of source 1 is expressed as [27]:

$$I_1 = \frac{E_1}{Z + \frac{Z}{n-1} // Z_L} - \frac{\frac{Z}{n-1} // Z_L}{Z\left(Z + \frac{Z}{n-1} // Z_L\right)} \left[E_2 + ... + E_n\right]. \tag{2.6}$$

Similarly, equations of output currents of all other units can be derived in the same manner as in (2.6).

Equation (2.6) can be simplified and written in a more general form. For n parallel ac voltage sources with output voltages $E_1, E_2, ..., E_n$, output impedance equals to Z, and a load

impedance of Z_L, the output current of unit i is:

$$I_i = \frac{E_i}{Z + nZ_L} + \frac{Z_L}{Z\left(Z + nZ_L\right)}\left[nE_i - \sum_{j=1}^{n} E_j\right]. \tag{2.7}$$

The current of unit i can be divided into two components as follows:

1. Load current component ($I_i^{'}$): This is the contributed current from source i to the load current.

$$I_i^{'} = \frac{E_i}{Z + nZ_L}. \tag{2.8}$$

2. Circulating current component: This is the summation of all circulating currents between this source and all other parallel sources.

$$I_{ci} = \frac{Z_L}{Z\left(Z + nZ_L\right)}\left[nE_i - \sum_{j=1}^{n} E_j\right]. \tag{2.9}$$

The circulating current component depends on the difference between the output voltages of the parallel sources. If all voltage sources had the same voltage amplitude, frequency, and phase, then the circulating current will be zero, which is the ideal case.

2.5 Basic Control Strategies of Parallel UPS Systems

The advancement of Digital Signal Processors (DSPs) has caused the development of many control techniques for UPS systems. Control techniques of parallel UPS systems can be classified into two main categories, with regard to the communication between the parallel units [4]. The first control scheme is based on active load sharing (ALS) and is based on intercommunication links between the modules [4]. The second one is independent control; it does not require communication links.

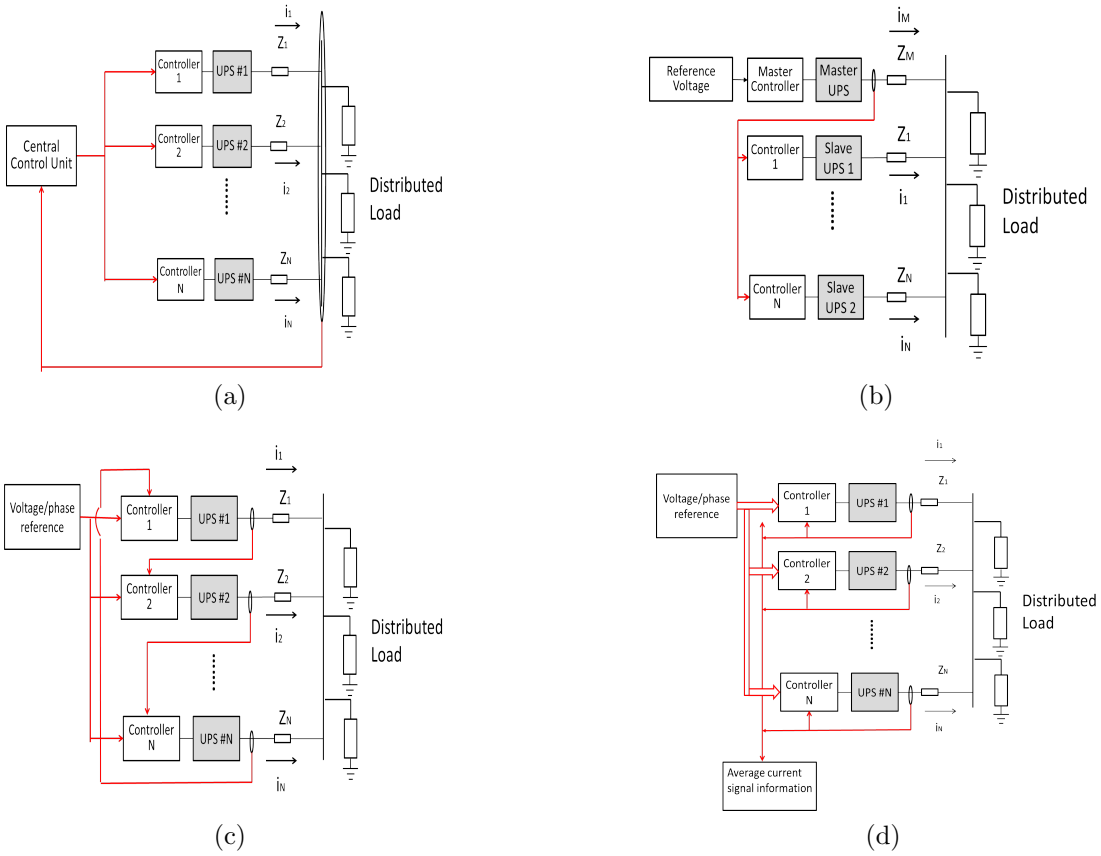


Figure 2-7: Different control techniques for UPS systems: a) centralized control, b) master-slave, c) 3c and d) average load sharing.

2.5.1 Active load sharing techniques

Centralized control

In this method a central control unit sends reference commands to all parallel connected UPS modules based on the feedback of output currents of the units [8]. A block diagram of n parallel-connected UPS units is shown in Fig. 2-7a. The average current of all parallel units is divided by the number of modules, n, and this average value becomes the reference current to all modules.

Master-slave control

In this control scheme, one of the parallel units is a Master unit. This unit has a Phase-locked-loop (PLL) which is used to synchronized the load voltage and phase with the grid voltage. The

Master unit regulates the load voltage. All other parallel UPS units are considered as Slave units, which take the reference current command from the Master unit [9]. In case of failure of the Master unit, one of the Slave units takes the role of the Master to avoid total system failure. A block diagram of the system is shown in Fig. 2-7b.

Circular Chain Control (3c)

In this method, each provides the reference current for the next unit forming a chain. The last unit in the system provides the reference current for the first unit. The block diagram of the system is shown in Fig. 2-7c.

Average load sharing

A current bus is used in this method to calculate the average current of all parallel modules [28, 29, 30]. The reference current is used as the reference for each individual unit, so that all currents are equal. A block diagram of the system is shown in Fig. 2-7d.

2.5.2 Independent Control (Droop Control)

Although communication-based control techniques can achieve satisfactory performance in terms of load voltage regulation and current distribution, the existence of interconnections between the modules puts limitations on the flexibility of the system and the physical locations of the modules, which adversely affects the reliability and expandability of the system due to the possibility of failure of communication links [4, 5].

As an alternative, another well-developed method discussed in the literature is the Droop method [10]. This method is based on control of parallel distributed energy sources without exchanging information (also called independent control). The "droop" method is traditionally employed to mimic the performance of parallel generators. The control alters the frequency and voltage of each source as functions of its active and reactive power, respectively. Independent

control strategies are based on the same concept of parallel generators, in which the generator drops its frequency when its output power increases. This method has the advantage of control of load sharing between UPSs without the need of any interconnections between them.

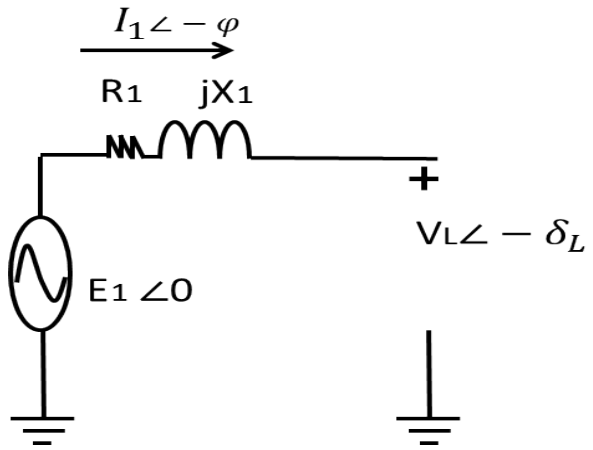


Figure 2-8: Voltage source connected to a bus through an impedance.

Consider a voltage source connected to a bus through a line impedance as shown in Fig. 2-8. The voltage of the source is $E_1 \underline{/0}$, the voltage of the load bus is $V_L \underline{/-\delta_L}$, and the impedance of the line is $R_1 + jX_1$. The current flowing from the source to the load is $I_1 \underline{/-\phi_1}$, and can be calculated as:

$$\begin{aligned} \bar{I}_1 &= \frac{E_1 \underline{/0} - V_L \underline{/-\delta_L}}{R_1 + jX_1} \\ &= \frac{R_1 \left(E_1 - V_L \cos(\delta_L)\right) + X_1 V_L \sin(\delta_L) + j \left[R_1 V_L \sin(\delta_L) + X_1 \left(V_L \cos(\delta_L) - E_1\right)\right]}{R_1^2 + X_1^2}. \end{aligned} \tag{2.10}$$

The complex power delivered from the source can now be calculated as:

$$S_1 = \bar{E}_1 \bar{I}_1^{\,*}. \tag{2.11}$$

By substituting the equation of the current from (2.10) into (2.11), the active and reactive power delivered from the source can be written as:

$$P = \frac{E_1}{R_1^2 + X_1^2} \left[R_1 \left(E_1 - V_L \cos \delta_L \right) + X_1 V_L \sin \delta_L \right]. \tag{2.12}$$

$$Q = \frac{E_1}{R_1^2 + X_1^2} \left[-R_1 V_L \sin \delta_L + X_1 \left(E_1 - V_L \cos \delta_L \right) \right]. \tag{2.13}$$

Depending on the impedance of the line, the relationships between the active and reactive power and the system parameters will vary. The following two cases will be discussed:

1. Inductive line:

   In this case the inductive part of the line impedance is much larger than the resistive part, $X_1 >> R_1$, R_1 is ignored in this case. Moreover, the power angle δ_L is assumed to be very small, so it can be assumed that $\sin \delta_L \approx \delta_L$ and $\cos \delta_L \approx 1$. Then, the equations of active and reactive power can be estimated as:

$$P \approx \frac{E_1}{X_1} \left[V_L \sin \delta_L \right] \rightarrow \delta_L \approx \frac{X_1 P}{E_1 V_L}. \tag{2.14}$$

$$Q \approx \frac{E_1}{X_1} \left[E_1 - V_L \cos \delta_L \right] \rightarrow E_1 - V_L \approx \frac{X_1 Q}{E_1}. \tag{2.15}$$

   It can be seen, from (2.14) and (2.15) that the active power delivered from the source has a roughly direct relationship with the power angle ($P \sim \delta_L$), and the reactive power has a roughly direct relationship with the voltage difference ($Q \sim (E_1 - V_L)$). Hence, it is possible to regulate the grid frequency and the voltage at the point of connection of the power source by controlling the active and reactive power of the source. The well-known droop control strategy is developed based on this concept; that is, to droop the frequency when the active power increases and to droop the voltage when the reactive

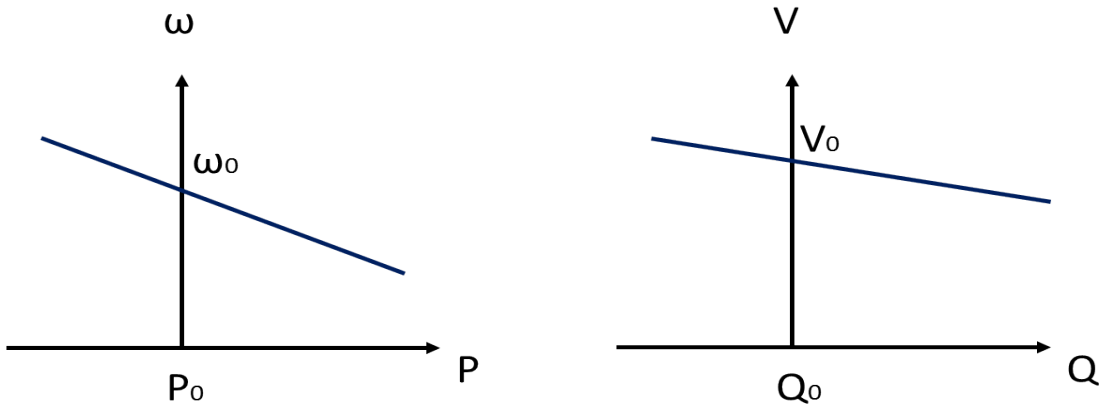
power increases. Therefore, the following droop equations can be written for inductive lines:

$$f = f_0 - k_p \left(P - P_0\right) \tag{2.16}$$

$$V = V_0 - k_q \left(Q - Q_0\right) \tag{2.17}$$

where f_0 and V_0 represent the rated grid frequency and grid voltage, respectively. P_0 and Q_0 are the rated active and reactive power of the source. k_p and k_q are the slopes of the frequency and voltage droop lines.

Equations (2.16) and (2.17) can be represented graphically as shown in Fig. 2-9. Notice that each power source adjusts its active and reactive power reference according to its P/ω and Q/V droop characteristics to regulate the frequency and voltage of the grid.



(a) (b)

Figure 2-9: Droop control for an inductive line (a) Active power vs. frequency, (b) reactive power vs. voltage.

2. Resistive line:

The line impedance is mainly resistive in case of LV (Low Voltage) networks. As a consequence, the resistive part of the line impedance is assumed to be much larger than the reactive part ($R_1 >> X_1$), and hence, X_1 can be neglected. Based on the same equations (2.12) and (2.13), and maintaining the assumption that the power angle δ_L is small, the active and reactive power equations become as follows:

$$P \approx \frac{E_1}{R_1}\left[E_1 - V_L \cos\delta_L\right] \rightarrow E_1 - V_L \approx \frac{R_1 P}{E_1}. \tag{2.18}$$

$$Q \approx -\frac{E_1 V_L}{R_1}\sin\delta_L \rightarrow \delta_L \approx -\frac{R_1 Q}{E_1 V_L}. \tag{2.19}$$

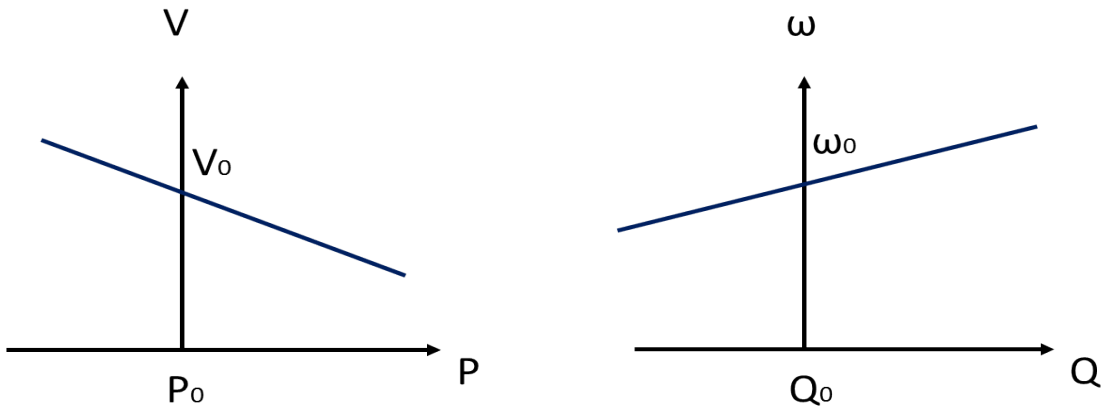
Contrary to the inductive line impedance case, for a resistive line impedance, the voltage amplitude depends on the active power flow, and the frequency depends on the reactive power flow. The following droop equations can be written for this case:

$$V = V_0 - k_p\left(P - P_0\right) \tag{2.20}$$

$$f = f_0 + k_q\left(Q - Q_0\right) \tag{2.21}$$

The droop charactersitics for a resistive line impedance is depicted in Fig. 2-10. Notice that the characteristics exhibit P/V and Q/ω droop controls.

The block diagram of a UPS module with the droop control mechanism implementation is shown in Fig. 2-11. The voltage and current signals are measured and used to calculate the active and reactive power. Then, the reference frequency and voltage amplitude are determined based on the droop equations. The reference signal is then sent to the UPS module.



(a) (b)

Figure 2-10: (Droop control for a resistive line (a) Active power vs. voltage, (b) reactive power vs. frequency.

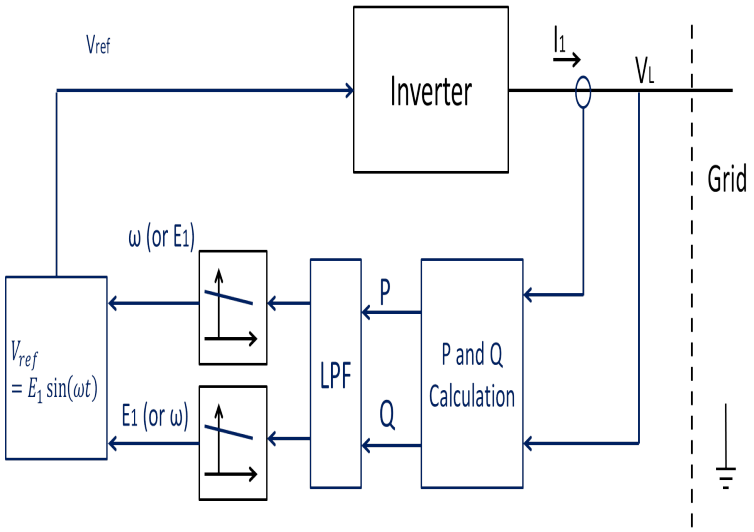


Figure 2-11: Block diagram of Droop control.

Using this scheme, it is possible to control parallel UPS modules without the need for interconnecting wires.

The active load sharing technique and the droop control method have been widely used to control parallel distributed generation systems. However, both methods exhibit some disadvantages. The choice of a control scheme depends on the requirements and the application. The following are the advantages and disadvantages of each method:

- Active load sharing:

  This method achieves excellent current sharing between parallel modules with high accuracy, as well as good voltage regulation. However, the existence of communication links between the units puts limitations on the distances between them and reduces the flexibility of the system. Moreover, the reliability of the system is reduced due to the possibility of failure of communication lines that may cause shut down of the complete system.

- Droop control:

  The droop method achieves higher reliability and flexibility than the active load sharing method since it does not rely on intercommunication lines to achieve power sharing. Instead, it relies on local power measurements. However, the traditional droop method also has disadvantages that limits its applications. Some of the disadvantages are slow dynamic response compared to ALS; since the method depends on continuous calculation of active and reactive power. Another disadvantage is that there is a trade-off between the voltage and frequency regulation, and the current sharing accuracy. The droop method has generally less accuracy than the ALS. Although the accuracy can be improved, the deviation of the voltage amplitude and frequency from the nominal values will increase. Other drawbacks include unbalanced harmonic current distribution and dependency on the output impedance of the inverter.

2.6 Literature review of modern control techniques

This section shows some related control techniques used in parallel UPS systems. Mainly, this section is focused on techniques used to improve the traditional droop control to mitigate its disadvantages.

The mismatch in the line impedance of the inverters affects the reactive power sharing accuracy of the droop method. The authors in [11] improved the traditional droop technique by adding to functions: Error reduction function and voltage recovery function. The method improves the reactive power sharing by changing the voltage bias on the basis of the conventional droop control, which is activated by a sequence of synchronization events through the low-bandwidth communication network. A DG unit can communicate with other DG units by RS232 serial communication. The error reduction operation will result in a decrease in output voltage amplitude. Therefore, the second operation is performed to restore the output voltage to its rated value.

The virtual impedance concept is widely used in the literature as a mean to control the power sharing by varying the output impedance of the inverter [31]. The proper design of the virtual impedance can mitigate the effect unbalance of the line impedance. The virtual impedance is implemented by dropping the reference voltage proportionally to the output current of the inverter, as shown in the following equation:

$$v_{ref} = v_o^* - Z_V(s) i_o \tag{2.22}$$

where v_o^* is the output reference voltage at no-load, $Z_V(s)$ is the virtual impedance, and i_o is the output current.

To mitigate the steady-state reactive power sharing errors, the authors in [12] implemented an enhanced control strategy that estimates the reactive power control error through injecting

small real power disturbances, which is activated by a low bandwidth synchronizations signals from a central controller. A slow integration term of reactive power sharing error is also integrated into the controller to eliminate this error.

Some control techniques focus on grid-connected inverters applications. The authors in [73] used grid impedance estimation techniques to automatically adjust the control parameters. The control has two main structures. The first one is the grid parameter estimation, which calculates the amplitude and frequency of the grid, as well as the magnitude and phase of the grid impedance. The second one is a droop-control scheme, which uses these parameters to inject independently active and reactive power to the grid.

Virtual flux droop method is also used sometimes [14]. Virtual flux technique can achieve similar results as the conventional droop with less frequency deviations.

Han *et al.* [15] did a comprehensive review of various control techniques (including communication-based and autonomous techniques), and divided them into different categories. The authors classified the variants of the droop techniques into four groups: 1) conventional and variants of the droop control; 2) virtual framework structure-based control; 3) "construct and compensate" based methods; and 4) hybrid droop/signal injection methods.

2.7 Summary

A review of the difference classifications and configurations of UPS systems was introduced in this chapter. The conditions for parallel operation of parallel inverters were explained along with a brief literature review of the modern control techniques that are most pertinent to this dissertation were introduced. The concept of distributed generation and its advantages were explained. Mathematical equations for the circulating current between parallel inverters were derived.

Chapter 3

Three Phase Inverter Principles and DQ Synchronous Frame Controller

The present chapter discusses the basic concepts of three phase inverters, including pulse width modulation (PWM) and the average model of the inverter with the output filter in the direct-quadrature synchronous frame. The basic structure of phase-locked loop (PLL) and its variations are also introduced. Resonance damping of the *LCL* filter using multi-loop control is also discussed in detail.

3.1 Introduction

The advent of digital control and digital signal processors (DSPs) has resulted in the introduction of advanced complex control techniques of static converters in real time. Digital control adds many advantages into the system, such as: Ease of addition/integration of new functions into the system without the need to add new parts or to alter the structure of the system, but rather, the underlying software can be updated/modified without limitations. Other advantages brought by digital control include increased reliability and robustness of the system, and reduced cost. As a result, control techniques, as as PWM, has become more efficient due to the increased

switching frequencies and reduced totalharmonic distortion (THD) under linear and nonlinear loads [32, 33].

3.2 Three Phase AC/DC Inverter Model

An inverter is the basic block in UPS systems and power converting devices. An accurate model of the voltage source inverter (VSI) is vital for the simplification of the analysis and the design of control circuits. In this section, generalized analysis of the average model of three phase inverters are presented. Fig. 3-1 shows the circuit configuration of a three phase inverter connected to a load. There are six switching devices labelled as S_1, S_2,...,S_6. The inverter can be modelled as a multi-frequency ac generator.

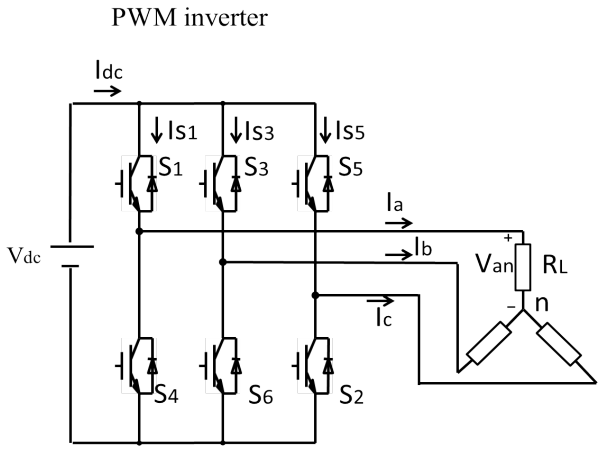
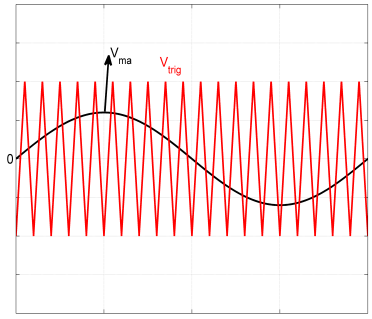
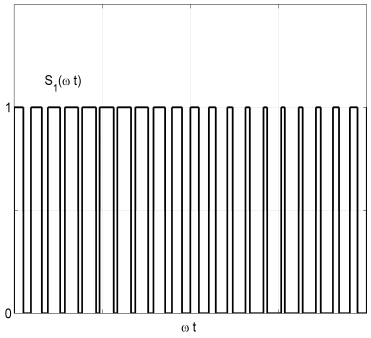


Figure 3-1: Three phase inverter connected to a Y three phase load.

There are many switching functions that can be applied to the switches to generate output voltage. The switching functions are generated by comparing a triangular carrier waveform to a reference modulating signal. The amplitude, phase, and frequency of the modulating signal are used to control the output ac voltage of the inverter. The modulating signal of phase a (V_{ma}) along with the triangular high frequency signal (V_{trig}) are shown in Fig. 3-2a. Two switching functions are shown in Fig. 3-2b and Fig. 3-2c, which are obtained by comparing the two signals



(a)



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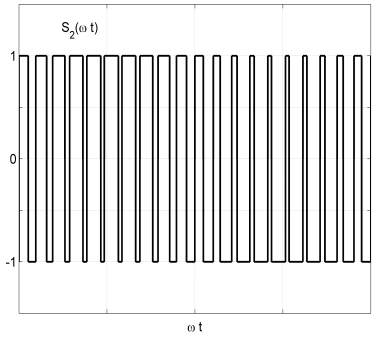


(c)

Figure 3-2: a) Modulating signal (V_{ma}) and triangular signal (V˙trig), b) switching function $S_1(\omega t)$, and c) switching function $S_2(\omega t)$.

in Fig. 3-2a.

The switching function $S_2(\omega t)$ represents the switching function of one of the inverter legs (S_1 and S_2), and is used to calculate the output line-to-line voltages and phase voltages of the inverter. The switching function $S_1(\omega t)$, on the other hand, designates the voltage across one of the six switches of the inverter (i.e., S_1) the switch, and hence, is more effective in calculating the current ratings of the components [34].

The switching patterns are effective in deriving analytical expressions for the voltage and current waveforms. Therefore, mathematical expressions are required in order to facilitate the analysis of the inverter. Such mathematical expressions can be obtained by deriving the Fourier expansion of the switching functions. The following are mathematical representation for S_1 and

S_2:

$$S_1 = A_0 + \sum_{n=1}^{\infty} A_n \sin(n\omega t) \tag{3.1}$$

$$S_2 = \sum_{n=1}^{\infty} B_n \sin(n\omega t). \tag{3.2}$$

Notice that S_1 has a dc component that is not present in S_2.

For a three phase VSI, six switching functions are required. Three phase modulating signals are compared with a triangular wave to generate the six switching patters, as shown in Fig. 3-3. The output line-to-line voltage (V_{ab}) is shown in Fig. 3-4.

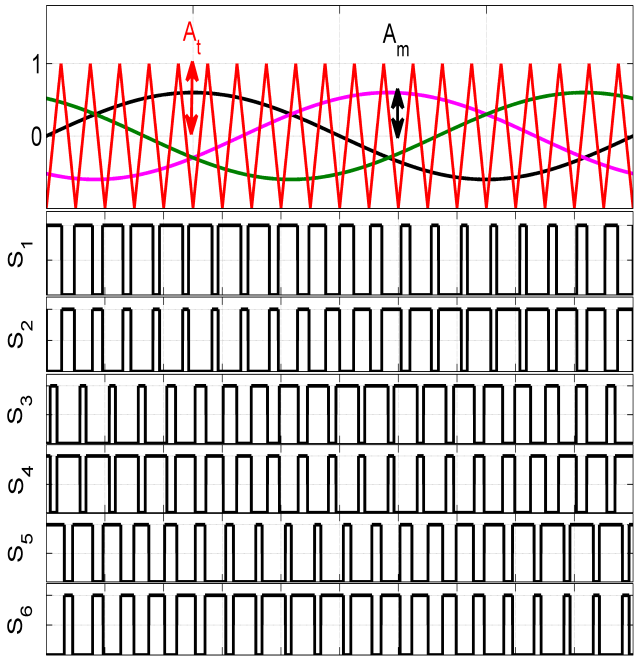


Figure 3-3: Three phase modulating signals are compared with a triangular wave to generate six switching functions.

After analytical expressions for the switching functions are specified, the inverter phase voltages (V_{a0}, V_{b0}, and V_{c0}) are obtained as:

Figure 3-4: Output line-to-line voltage of a three phase inverter.

$$V_{a0}(\omega t) = \frac{V_{dc}}{2} S_2 = \frac{V_{dc}}{2} \sum_{n=1}^{\infty} B_n \sin(n\omega t) \tag{3.3}$$

$$V_{b0}(\omega t) = V_{a0}(\omega t - 120^\circ) \tag{3.4}$$

$$V_{c0}(\omega t) = V_{a0}(\omega t + 120^\circ) \tag{3.5}$$

Next, the inverter line-to-line voltages are obtained from the phase voltages as follows:

$$V_{ab}(\omega t) = V_{a0}(\omega t) - V_{b0}(\omega t) = \frac{\sqrt{(}3)V_{dc}}{2} \sum_{n=1}^{\infty} B_n \sin[n(\omega t + 30^\circ)] \tag{3.6}$$

$$V_{bc}(\omega t) = V_{b0}(\omega t) - V_{c0}(\omega t) = \frac{\sqrt{(}3)V_{dc}}{2} \sum_{n=1}^{\infty} B_n \sin[n(\omega t - 90^\circ)] \tag{3.7}$$

$$V_{ca}(\omega t) = V_{c0}(\omega t) - V_{a0}(\omega t) = \frac{\sqrt{(}3)V_{dc}}{2} \sum_{n=1}^{\infty} B_n \sin[n(\omega t + 150^\circ)] \tag{3.8}$$

The voltage V_{n0} is calculated as:

$$V_{n0}(\omega t) = \frac{1}{3}\left[V_{a0} + V_{b0} + V_{c0}\right]. \tag{3.9}$$

The phase voltages at the output can now be calculated as:

$$V_{an}(\omega t) = V_{a0} - V_{n0} \tag{3.10}$$

$$V_{bn}(\omega t) = V_{b0} - V_{n0} \tag{3.11}$$

$$V_{cn}(\omega t) = V_{c0} - V_{n0}. \tag{3.12}$$

For a three phase balanced load, the inverter line currents can be calculated from the phase voltages:

$$I_a(\omega t) = \frac{V_{an}(\omega t)}{Z(\omega t)} \tag{3.13}$$

$$I_b(\omega t) = \frac{V_{bn}(\omega t)}{Z(\omega t)} = I_a(\omega t - 120^\circ) \tag{3.14}$$

$$I_c(\omega t) = \frac{V_{cn}(\omega t)}{Z(\omega t)} = I_a(\omega t + 120^\circ) \tag{3.15}$$

where $Z(\omega t)$ is the impedance of the load.

Next, the current flowing in the ideal switches is calculated by multiplying the line current with the respective switching function:

$$I_{s1}(\omega t) = I_a(\omega t).S_{1a}(\omega t) \tag{3.16}$$

$$I_{s3}(\omega t) = I_b(\omega t).S_{1b}(\omega t) \tag{3.17}$$

$$I_{s5}(\omega t) = I_c(\omega t).S_{1c}(\omega t). \tag{3.18}$$

Each of the six ideal switches consists of a controlled switch (e.g., thyristor, transistor) and an anti-parallel diode. Hence, each switch current consists of two components: I_{s1s} and I_{s1d}, representing the switch and diode currents, respectively.

$$I_{s1}(\omega t) = I_{s1s}(\omega t) - I_{s1d}(\omega t) \tag{3.19}$$

$$I_{s3}(\omega t) = I_{s3s}(\omega t) - I_{s3d}(\omega t) \tag{3.20}$$

$$I_{s5}(\omega t) = I_{s5s}(\omega t) - I_{s5d}(\omega t). \tag{3.21}$$

Finally, the inverter input current (I_{dc}) can now be obtained:

$$I_{dc} = I_{s1}(\omega t) + I_{s2}(\omega t) + I_{s3}(\omega t); \tag{3.22}$$

The average model of the inverter is used to derive the mathematical equations which govern its operation. The line output voltages of the inverter can be derived using the switching state functions:

$$\begin{bmatrix} u_{ab} \\ u_{bc} \\ u_{ca} \end{bmatrix} = \frac{V_{dc}}{2} \begin{bmatrix} S_a - S_b \\ S_b - S_c \\ S_c - S_a \end{bmatrix} \tag{3.23}$$

where S_a, S_b, and S_c are the switching functions described in (3.2).

The following equations describe the voltage and current relations for an inverter with output LCL filter:

$$\frac{di_{o1abc}}{dt} = -\frac{R_0}{L_0} i_{o1abc} - \frac{1}{L_0} e_{1abc} + \frac{1}{L_0} u_{1abc} \tag{3.24}$$

$$\frac{de_{1abc}}{dt} = \frac{1}{C} i_{o1abc} - \frac{1}{C} i_{1abc} \tag{3.25}$$

$$\frac{di_{1abc}}{dt} = -\frac{R_1}{L_1} i_{1abc} + \frac{1}{L_1} e_{1abc} - \frac{1}{L_1} v_L. \tag{3.26}$$

3.3 Phase Locked Loop and Synchronization

The phase-locked loop (PLL) is a fundamental concept used in various applications in electrical engineering, such as [35, 37, 36]: controlled AC/DC converters, static VAR compensators, cycloconverters, active harmonic filters, communication, motor servo control systems, and many other applications. The fundamental concept of PLL is to generate a signal whose phase angle tracks the phase of the input signal. This information is used to synchronize power devices, control the flow of power, and transform voltage and current variables to a synchronous reference frame. The quality of PLL directly affects the control performance of the application. Hence, it is imperative to design a PLL system that can not only phase-lock to the utility voltage, but also provide a stable phase output with low distortion.

Under ideal conditions, a PLL system should provide fast and accurate synchronization information with a high degree of immunity and insensitivity against various common utility distortion conditions, such as voltage unbalance, frequency variations, disturbances, harmonics, sags/swells, line notching, and other types of distortions in the input signal.

The basic block diagram of a conventional PLL is shown in Fig. 3-5 [35]. The main purpose of this system is to estimate the difference in phase angle between the input signal and the output signal and to minimize this error signal as much as possible. The phase detector (PD) is usually a multiplier that generates an error signal that corresponds to the phase difference. This error signal is passed to a loop filter (LF) or a loop controller, and the voltage controller oscillator (VCO) generates the output signal.

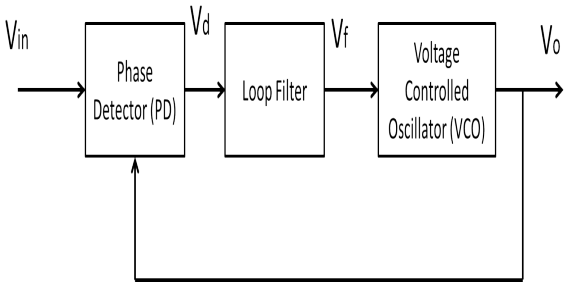


Figure 3-5: Block diagram of a basic PLL structure.

3.4 Three Phase PLL Circuit

3.4.1 PLL Basic Concept

Based on the simplified structure of the basic PLL in Fig. 3-5, for three phase systems the same structure can be used after making some modifications. Suppose that the input signal V_{in} and the output signal V_o are represented as space vectors as follows:

$$v_{in}(t) = V_{in}e^{j(\omega_{in}t+\theta_{in})} \tag{3.27}$$

$$v_o(t) = V_o e^{j(\omega_o t+\theta_o)} \tag{3.28}$$

where V_{in} and V_o are the amplitudes of the input and output signals, respectively, ω_1 and ω_2 are their frequency, respectively, and θ_{in} and θ_o are their phase angles.

Three phase signals can be transformed to stationary (α-β) reference frame by means of Clarke transformation. For a three phase grid voltage space vector $\vec{v}_{abc}$ is defined as:

$$\vec{v}_{abc} = [v_a, v_b, v_c]^T = \begin{bmatrix} \sqrt{2}V\sin\theta \\ \sqrt{2}V\sin(\theta - 120^\circ) \\ \sqrt{2}V\sin(\theta + 120^\circ) \end{bmatrix} \tag{3.29}$$

where V is the RMS value of the grid voltage and θ is the phase angle.

The Clarke transformation of the time-domain signals from abc to $\alpha - \beta$ frame can be represented as follows:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & -\sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}. \tag{3.30}$$

Fig. 3-6 shows the vector representation of the three phase signals in the stationary abc frame, and the coordinates transformation to the stationary $\alpha - \beta$ frame. Notice that the α axis is synchronized with the a axis. Notice also that the α and β axes are orthogonal to each other.

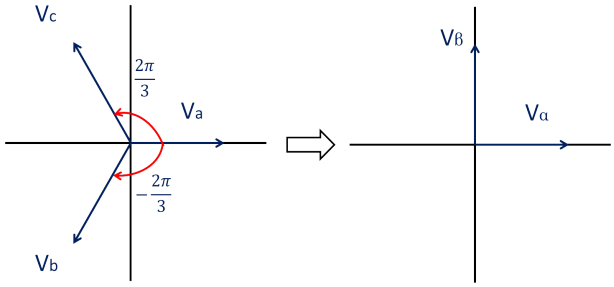


Figure 3-6: Vector representation of three phase signals in stationary abc frame and equivalent two phase signals in stationary $\alpha - \beta$ frame.

Both the input and output signals in (3.27) and (3.28) can be represented in the form $v(t) = v_\alpha + jv_\beta$, where $v_\alpha(t) = V\sin(\omega t + \phi$, and $v_\beta(t) = V\cos(\omega t + \phi)$. The PD in Fig. 3-5 operates by multiplying two signals (the input and the output signals), then estimates the phase

difference between them. There are many ways to build the PD. One of the methods is based on the imaginary (q) power component. In this case, the method is called q-PLL. The real part can also be used as in the p-PLL scheme, however, the q-PLL will be used in the analysis.

The output of the PD, based on the q-PLL scheme, is as follows:

$$\begin{aligned} v_d(t) &= v_{in\alpha} v_{o\beta} - v_{in\beta} V_{o\alpha} \\ &= V_{in} \sin(\omega_{in} t + \phi_{in}) V_o \cos(\omega_o t + \phi_o) - V_{in} \cos(\omega_{in} t + \phi_{in}) V_o \sin(\omega_o t + \phi_o) \\ &= V_{in} V_o \sin[(\omega_{in} - \omega_o)t + (\phi_{in} - \phi_o)]. \end{aligned} \tag{3.31}$$

Considering that the PLL is nearly locked at the nominal frequency ($\omega_{in} \approx \omega_o$), and by normalizing the amplitudes to unity, the error signal can be simplified to:

$$v_d(t) \approx \sin(\phi_{in} - \phi_o). \tag{3.32}$$

Furthermore, for a small difference in the phase angle between the input and the output, (3.32) can be approximated as:

$$v_d(t) \approx \phi_{in} - \phi_o. \tag{3.33}$$

The representation of the PLL is shown in Fig. 3-7. The three phase signals are transformed to the synchronous ($\alpha - \beta$) frame as in (3.30). Then, the phase difference between the reference input phase and the output phase is calculated based on equation (3.31). The error signal passes through a PI controller. An integrator is used to obtain the phase angle from the frequency signal.

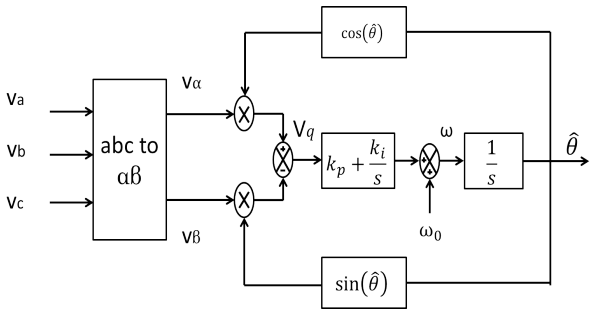


Figure 3-7: Block diagram of Q-PLL.

3.4.2 Direct-Quadrature-Zero (dq0) Transformation

In an effort to further simplify the analysis of three phase systems, the AC quantities in the stationary $\alpha - \beta$ reference frame can be transformed to dc quantities in a rotating synchronous frame. The dq0 transform, often referred to as Park's transformation, reduces the ac voltage and current quantities to two dc signals in case of balanced three phase systems. This enables performing simplified calculations on dc quantities before performing inverse transformation to recover the original three phase signals.

The transformation equations from $\alpha - \beta$ to dq-frame is given below [39, 38]:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \sin\theta_{ref} & \cos\theta_{ref} \\ \cos\theta_{ref} & -\sin\theta_{ref} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{3.34}$$

where θ_{ref} is the reference phase angle of the grid which can be extracted by means of PLL. The vector in the dq synchronous frame has the same amplitude as the space vector in the three phase frame. In the dq-frame, the phase is γ, where $\gamma = \theta - \theta_{ref}$. θ_{ref} is the phase difference between the d-axis and the α-axis (which is the same as the a-axis). If $\theta = \theta_{ref}$, as in the case of load voltage which is synchronized with the grid, then $v_{dq} = [\sqrt{2}V, 0]^T$. For other voltage/current quantities, their equivalent dc values in the synchronous frame will depend on their phase shift from the reference frame.

Reverse transformation from the dq synchronous frame to the $\alpha - \beta$ frame can be obtained

by taking the inverse of (3.34):

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \sin\theta_{ref} & \cos\theta_{ref} \\ \cos\theta_{ref} & -\sin\theta_{ref} \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \tag{3.35}$$

Finally, the three phase quantities can now be obtained:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{3.36}$$

Suppose that three phase positive sequence signals are connected to a PLL system, as shown in Fig. 3-7. Fig. 3-8 shows the three phase signals (v_a, v_b, and v_c) as well as the $\alpha - \beta$ signals obtained from the transformation matrix in (3.30). Notice that v_α is synchronized with v_a and the two signals are essentially the same. Notice also that v_β is shifted by 90° from v_α.

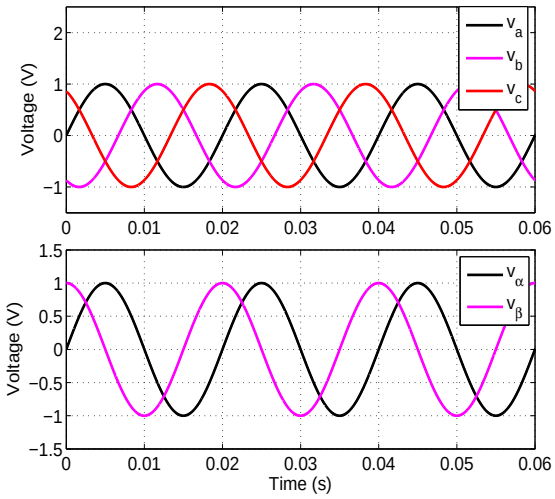


Figure 3-8: Three phase positive sequence voltages and equivalent α-β signals.

Fig. 3-9 shows the error signal (V_q in Fig. 3-7), the frequency, and the output phase of the PLL. The quadrature component of the voltage is zero and the frequency is constant and equals the frequency of the input voltage signals (50 Hz). The phase, which is the integral of the frequency, is a linear function with a constant slope.

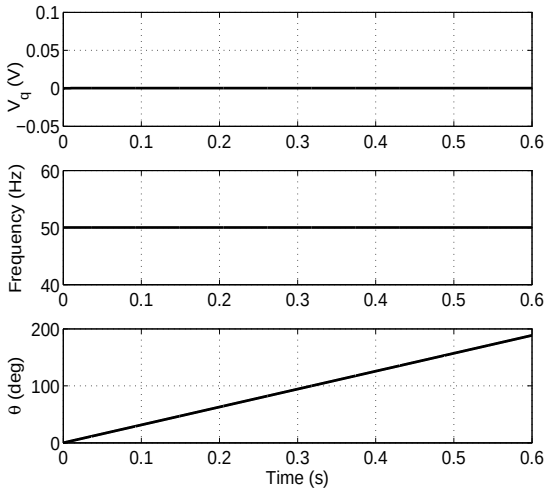


Figure 3-9: Quadrature component of the voltage, frequency, and output phase signal of PLL.

3.4.3 Other Variations of PLL

PLL in the frequency domain usually obtain the phase and frequency of the grid through a discrete-time Fourier transform (DFT), or fast Fourier transform (FFT). Although these algorithms achieve high precision, their heavy computational burden prevents them from achieving high dynamic performance [40, 41]. PLL methods in the time-domain, on the other hand, measure the instantaneous values of the grid voltage to detect the phase of the fundamental frequency component. The synchronous reference frame PLL (SRF-PLL) is one of the fundamental time-domain PLL schemes. It is commonly used in many applications to tack the phase of the utility voltage because it offers many advantages, such as ease of implementation, robustness, fast and accurate phase/frequency detection [42]. However, under non-ideal grid voltage conditions such as unbalanced or distorted voltage conditions, the performance of the SRF-PLL is degraded. One solution to counter this problem is to reduce the bandwidth of the PLL at the expense of dynamic performance, or to add additional low-pass filter in the feed-forward control loop. This section summarizes some of the techniques used in the literature to obtain a stable operation of PLL under distorted and unbalanced grid voltage conditions [42, 43].

1. SRF-PLL with additional LPF

   This techniques uses the same structure as the SRF-PLL, with an additional LPF in the control loop to increase the disturbance rejection of the harmonics. Careful design and tuning the filter parameters and cut off frequency of the filter are required.

2. Multiple Reference Frame PLL (MRF-PLL)

   This techniques employs two synchronous reference frames rotating at the same angular speed, but in opposite directions, and a decoupling network in the natural abc reference frame to extract and separate the fundamental-frequency positive/negative sequence components. In this way, the steady-state detection error caused by the fundamental negative-sequence component is eliminated [42].

3. Dual Second-Order Generalized Integrator Based PLL (DSOGI-PLL)

   This method is based on the instantaneous symmetrical components (ISC) theory in the stationary ($\alpha\beta$) reference frame. After transforming the three phase signals to the stationary frame, two SOGI-based quadrature signal generators are used filter the stationary components. The positive-sequence $\alpha\beta$ components are then extracted using the ISC theory in the $\alpha\beta$ domain. A conventional SRF-PLL is then used to extract the phase angle and frequency information. The estimated frequency is fed back to the DSOGI/PSC structure to make it frequency adaptive.

4. Type I Frequency Locked Loop (FLL)

   The conventional SRF-PLL is a type-II control system due to the use of proportional-integral controller as loop filter (a type-X control system has a transfer function with X poles at the origin [44]). To further increase the distrurbance rejection capability of the PLL, another approach is proposed based on FLL where the control system locks the

frequency of the input signal and the phase is estimated by integrating the frequency signal. This type of PLL is called type-I. By locking to the frequency, it is possible to achieve the performance of type-II PLL using type-I feedback control system [44]. However, type-I PLL cannot achieve the zero steady-state phase error during the step change in frequency. In [45], the authors introduced a technique that ensures the advantages of the type-I control system (i.e., improved dynamics performance with increased stability margins) and simultaneously achieves a zero steady-state phase error during the step change in frequency (i.e., the performance of a type-II PLL system).

5. Type-II and Type-III Frequency Locked Loop (FLL)

   type-III PLLs have been developed recently, either by adding a feed-forward path to the PLL structure or by using a second-order controller as the loop filter [44]. However, designing a type-III PLL intensifies the problem of stability. In addition, type-II SRF-PLL has lesser settling time compared to type-III PLL. In [44], a type-II FLL is proposed with similar performance to type-III PLL system (i.e. zero steady-state error in phase when the input signal frequency is subjected to a ramp change), without compromising the benefits of type-II control system.

3.4.4 Single Phase PLL

In single phase systems the process of synchronization is more complex than three phase systems because less information is available [41]. Designing a single phase PLL usually involves the generation of a fictitious orthogonal signal (called quadrature signal generation (QSG)) [41, 46]. Many approaches to generate the orthogonal signal have been proposed, the simplest perhaps being the transfer delay-based method. In the transfer delay-based PLL (TD-PLL), the orthogonal signal is generated by delaying the original single-phase signal by $T/4$ (one quarter of a period). The single phase signal and its orthogonal one are treated as stationary $\alpha\beta$-

frame components, so detection methods designed for three-phase systems, such as synchronous dq-frame PLLs, can be used [41]. There are many other approaches used to generate the orthogonal signal. Some of these approaches are [46]: Hilbert transform, Kalman filter, second-order generalized integrator, and inverse Park technique.

3.5 Output Filter and Resonance Damping

Filters are widely used at the outputs of the inverters to mitigate the switching harmonics and obtain a high quality output voltage. Initially, first order L filters were widely used. However, first order filters suffered from poor harmonic attenuation and dynamic performance, high voltage drop on the inductor, heavy weights and large size [47]. Many types of filters have been introduces, with the LCL filters being the most popular of them for grid-connected inverters due to their excellent performance in terms of harmonic attenuation ability at lower switching frequencies, and less total inductance compared with L filters [47, 48]. The proper design of the filter should take many factors into consideration. For example [47]: minimum voltage drop across the filter, high power factor operation, robustness to filter parameter variations as well as to external parameter variations (such as output impedance), low power loss, and minimum stored energy in the filter.

Compared to L filters, high-order passive filters provide a more cost-effective solution to PWM switching harmonics [49, 50]. Fig.3-10 shows the configuration of one inverter with LCL or LC filter connected at its output. The capacitor voltage is E and the load voltage is V_L. Normally, inverters operate in current-controlled or voltage-controlled modes, or a combination of both. Current controlled inverters often use LCL filters at the output [51]. The output current is controlled in a single loop [49] or double loops with a minor capacitor current or inductor current loop [52, 49, 53, 54], as shown in Fig. 3-11a. On the other hand, voltage controlled inverters normally use LC filters and control the capacitor voltage directly (Fig. 3-11b), while

incorporating a capacitor current or inductor current minor loops [5, 51, 31, 55, 56]. The voltage of the capacitor in this case is equal to the load voltage, if the impedance of the feeder is ignored. Applications of voltage-controlled inverters include UPS systems and distributed generation systems in island mode. Current controlled inverters, on the other hand, are used in grid-connected converters, active filters, and active rectifiers.

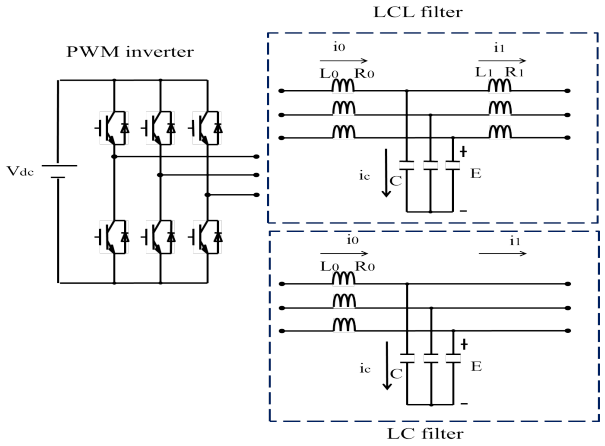


Figure 3-10: A three phase inverter with LC or LCL filter.

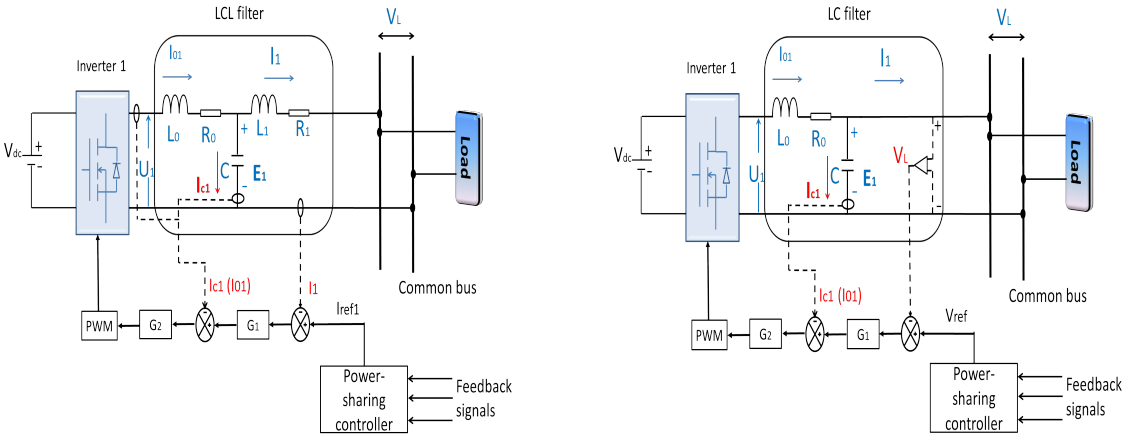


Figure 3-11: (a) Current-controlled inverter, (b) voltage-controlled inverter.

However, the inherent resonance of the *LCL* filter has the tendency to destabilize the system [49]. A direct way to damp the *LCL* resonance is to add a passive resistor. This solution is

simple for implementation and reliable, but introduces additional power loss into the system [52].

Another method to improve the system stability is active damping, such as multiloop control. Compared to single loop control, dual-loop control has more stability range and larger bandwidth [51]. There are various kinds of multiloop control schemes that have been discussed in the literature. Dual-loop control with capacitor voltage and capacitor current in the minor loop with LC filter has been used in [29]. Dual-loop control with load voltage in the outer loop (V_L in Fig. 3-11), and output current in the inner loop (i_1 in Fig. 3-11), can be used [57]. Single loop control with inverter current or grid current in the feedback loop has been employed in [49]. Single-loop current control with a hybrid damper is proposed for a single-phase LCL or $LLCL$ filter-based inverters in [50]. It has been demonstrated in [58] that grid current active damping is equivalent to the insertion of a virtual impedance in parallel with the grid-side inductance. Current-controlled inverters can also be employed [51, 49, 58, 52, 59], especially for grid-connected inverters. In [28] and [60] the authors controlled the capacitor voltage of LC filters, taking into account the impedance of the cable connecting the load. They also have proposed methods to ensure stability for different output impedance conditions.

When multiloop control is considered, the gains of the controllers have to be chosen carefully since they have direct effects on the damping capability of the controller. For an inverter with an output LCL filter, the transfer function of the inner capacitor current loop, as will be shown in the next section, is as follows [62]:

$$G_{in}(s) = \frac{k_c}{CL_0s^2 + (C * R_0 + C * k_c)s + 1} \tag{3.37}$$

where k_c is the gain of the capacitor current loop, L_0 and R_0 are the inverter-side inductance and its series resistance, and C is the capacitance.

The natural frequency and damping ratio of (3.37) are: $\omega_n = 1/(\sqrt{CL_0})$, $\zeta = (CR_0 +$

$Ck_c)/(2\sqrt{CL_0}$. Hence, the filter parameters affect the natural frequency and the gain affects the damping ratio. Fig. 3-12 shows the Bode plot of the transfer function (3.37) for different gain values. Increasing the gain will increase the resonance damping. However, this comes at the expense of increasing the error in the phase at the fundamental frequency. This error should be compensated by the outer voltage control loop [62].

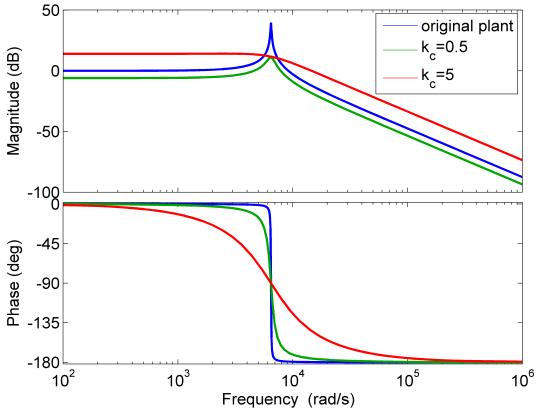


Figure 3-12: Effect of inner current loop gain on the Bode plot.

3.6 Multi-loop Control of VSI with *LCL* Filter

Multi-loop control of one inverter with output LCL filter will be considered in this section. The control block diagram of the system is shown in Fig. 3-13. The reference capacitor voltage of inverter 1 is E_{ref1}. There are two feedback loop in Fig. 3-13: inner capacitor current loop (I_{c1}), and outer capacitor voltage loop (E_1). U_1 is the PWM output voltage of the inverter, I_{01} is the inverter-side inductor current, I_1 is the output current, R_L is the load, and V_L is the load voltage.

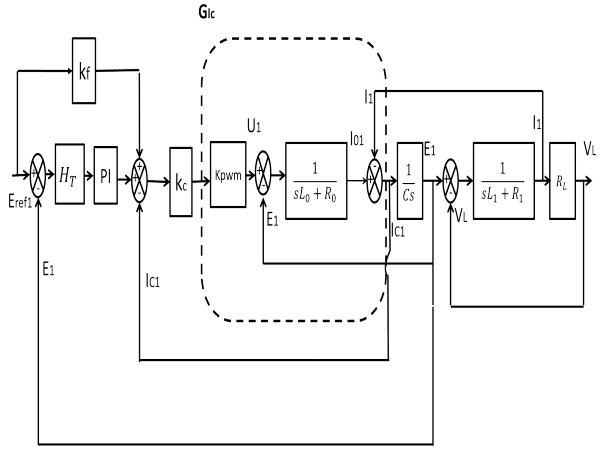


Figure 3-13: Block diagram of multi-loop control with capacitor current minor loop and capacitor voltage outer loop.

3.6.1 Inner current loop

Comparison between capacitor and inductor feedback schemes

Both inductor current (i_{01}), or capacitor current (i_{c1}) can be used in the inner feedback loop (see Fig.3-11). However, capacitor current exhibits more satisfactory steady-state and transient performance, especially under nonlinear load conditions [61]. Fig. 3-13 shows the block diagram of one inverter with capacitor current in the inner loop and capacitor voltage in the outer loop. For this configuration, the transfer function from the reference input to the filter capacitor voltage is expressed as:

$$E_1 = \frac{G_{PI}k_c k_{pwm}}{CL_0s^2 + Cs(R_0 + k_c k_{pwm}) + G_{PI}k_c k_{pwm} + 1}E_{ref1} - \frac{sL_0 + R_0}{CL_0s^2 + Cs(R_0 + k_c k_{pwm}) + G_{PI}k_c k_{pwm} + 1}I_1. \quad (3.38)$$

For inductor current feedback, the transfer function is:

$$E_1 = \frac{G_{PI}k_c k_{pwm}}{CL_0 s^2 + Cs(R_0 + k_c k_{pwm}) + G_{PI}k_c k_{pwm} + 1} E_{ref1} - \frac{k_c k_{pwm} + sL_0 + R_0}{CL_0 s^2 + Cs(R_0 + k_c k_{pwm}) + G_{PI}k_c k_{pwm} + 1} I_1. \quad (3.39)$$

In equations (3.38) and (3.39), the capacitor voltage depends on both the reference voltage and the output current of the inverter. In the ideal case, the capacitor voltage should track the reference at the fundamental frequency with unit gain and zero phase offset, while rejecting any influence from the load. Hence, the output current (I_1) can be viewed as a disturbance to the system, and the transfer function from the output current to the reference input should be minimized. The PI controller holds an infinite gain at the fundamental frequency, and therefore the capacitor voltage can track the reference value and the transfer function from the output current is zero. However, the controller has a limited bandwidth and hence, at harmonic frequencies the gain is reduced. The influence of the output current can be reduced by decreasing the value of the inverter-side inductor, but this will reduce the effectiveness of the filter in mitigating the harmonics.

For inductor current feedback system, there is an additional term in the numerator of the second term of equation (3.39) compared to the capacitor current feedback system (3.38). Hence, the harmonic currents have more significant effect on the voltage and exhibits a less satisfactory performance. The second term in (3.38) and (3.39) are written below with the inductor resistance ignored.

$$E_1 = -H(s)sL_0 I_1 \quad (3.40)$$

$$E_1 = -k_c k_{pwm} H(s) I_1 - H(s)sL_0 I_1 \quad (3.41)$$

where:

$$H(s) = \frac{1}{CL_0s^2 + Csk_ck_{pwm} + G_{PI}k_ck_{pwm} + 1}. \tag{3.42}$$

Notice that in both equations (3.41) and (3.41) the output current is multiplied by the Laplace operator s. In the time domain, this is equivalent to differentiation of the output current. This result suggests that the capacitor voltage is affected by the rate of change in the current. In other words, a change in the load will result in a dip or surge in the capacitor voltage, depending on whether it is an increase or a decrease in the load. However, the transfer function for inductor current feedback (3.40) includes an additional term (the first term). Which means that the capacitor voltage is affected not only by the rate of change, but also by the magnitude of the current. Hence, the inductor current feedback has a more severe effect on the transfer function.

Considering a capacitor current feedback system, the open-loop transfer function of inner loop (G_{Ic}) is:

$$G_{Ic} = \frac{Cs(sL_1 + R_1 + R_L)}{as^3 + bs^2 + es + d} \tag{3.43}$$

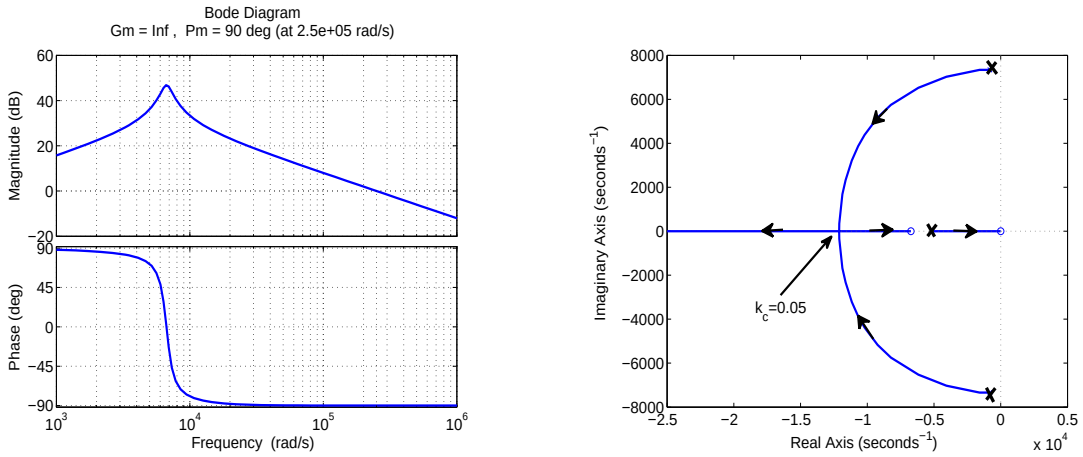
where $a = CL_0L_1$, $b = L_1R_0+L_0(R_1+R_L)$, $e = L_0+L_1+R_0C(R_1+R_L)$, and $d = R_0+R_1+R_L$. R_L is the load resistance.

To analyse the Bode plot of the inner current loop transfer function, the specifications shown in Table 3.1 will be used. The Bode plot of the open-loop transfer function G_{Ic} is shown in Fig. 3-14a. The Bode diagram of the inner capacitor current exhibits a theoretical gain margin of infinity and a phase margin of 90°. The root locus of G_{Ic} is shown in Fig. 3-14b. Notice that all poles are on the left-hand plane and two complex poles move towards the real axis and merge at $k_c = 0.05$. However, to avoid over compensation in the current loop, and because

digital implementation of the system puts limits on the maximum allowable gain to maintain stability of the system due to time delay and Zero Order Hold (ZOH) effect [49], a value of 0.02 for the proportional gain of the inner loop is chosen in this paper.

Table 3.1: Specifications of one inverter unit used in simulation.

Specification	Value	Component	Value
V_{dc}	300 V	R_0	55.6 mΩ
V_L	100 Vrms	L_0	0.6 mH
Switching frequency	15 kHz	C	40 μF
Output frequency	50 Hz	R_1	39 mΩ
Rated power	5 kVA	L_1	1.2 mH



(a) (b)

Figure 3-14: (a) Bode plot of open loop transfer function of capacitor current loop, (b) root locus of capacitor current transfer function.

3.6.2 Outer voltage loop

The open-loop transfer function of the outer voltage loop with a PI controller is:

$$G_v = G_{PI}.\frac{k_c G_{Ic}}{1 + k_c G_{Ic}}.\frac{1}{Cs} \tag{3.44}$$

where G_{PI} is the transfer function of the PI controller:

$$G_{PI} = k_p \left(1 + \frac{k_i}{s}\right). \tag{3.45}$$

In Fig. 3-13, k_f is the feed-forward gain, added to improve the dynamic performance of the system. H_T is a lead compensator added in the capacitor voltage forward loop. The lead compensator is used to advance the phase of the voltage transfer function in the vicinity of the 0 dB point in order to increase the phase cut-off frequency, resulting in increase in the phase margin of the system. The transfer function of the lead compensator is:

$$H_T = \frac{1 + \tau_1 s}{1 + \tau_2 s} \tag{3.46}$$

where $\tau_1 > \tau_2$. In this paper $\tau_1 = 100 \times 10^{-6}$, $\tau_2 = 20 \times 10^{-6}$.

The open-loop transfer function of the capacitor voltage loop including the lead compensator is:

$$G_{vd} = H_T.G_v. \tag{3.47}$$

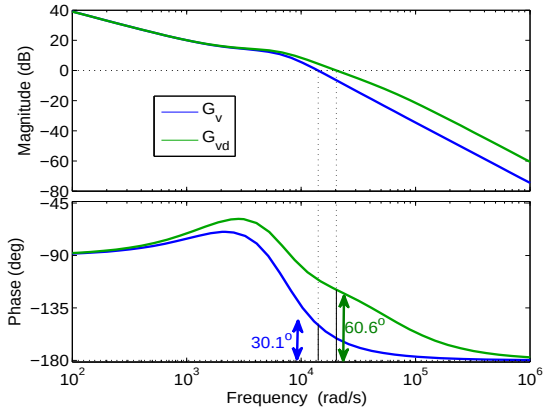


Figure 3-15: Bode plot open-loop transfer function of capacitor current loop.

Fig. 3-15 shows the Bode plots of both G_v and G_{vd}. Notice that the phase margin of the open-loop transfer function with the lead compensator is significantly larger than that without

compensation.

3.6.3 Digital Control and Time Delay

Digital implementation of the control system introduces two kinds of time delay into the system [52, 49]: pulse width modulation (PWM) delay and computation delay. Synchronous sampling refers to the sampling scheme in which the signal is sampled at the beginning or in the middle of the switching period [49]. Computation delay in synchronous sampling is one sampling period. The PWM delay, on the other hand, is caused by the zero-order hold (ZOH), which keeps the PWM reference constant after it has been sampled [52]. The delay might have substantial effects on the performance of inverters with LCL filters, and may cause instability problems. Particularly, many researchers have concluded that the frequency $f_s/6$ (where f_s is the sampling frequency) is a critical value and that the resonance frequency of the filter has to be designed away from this critical value to avoid instability problems [52].

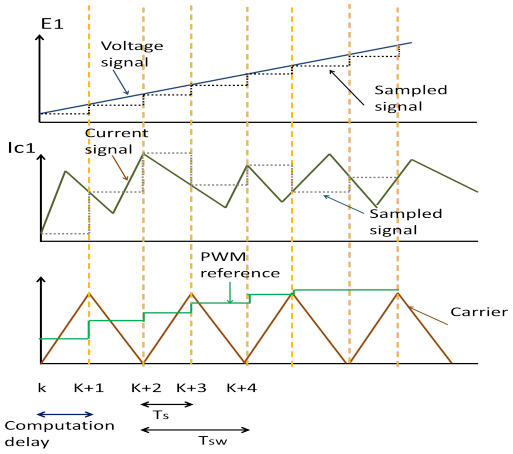


Figure 3-16: Sampling of voltage and current signals, and computation delay.

Fig. 3-16 shows the sampling process of the capacitor voltage and capacitor current of LCL filter. Sine-triangle synchronous sampling is used in this case, with a sampling period of T_s and a switching period of T_{sw}. Notice that since the signals are sampled twice every switching period, the sampling frequency is twice the switching frequency. The actual signals and the

sampled signals are shown for every signal. The triangular carrier is shown at the bottom of the figure along with the PWM reference signal. At the sampling instant k, the sampled voltage and current signals are used to calculate the reference PWM. The reference PWM is updated at the sampling instant *k+1* [52]. Hence, a computation delay of one sampling period is introduced into the system. The computation delay is expressed in the s domain as:

$$G_d(s) = e^{-T_s s}. \tag{3.48}$$

The block diagram of one inverter considering the delay is shown in Fig. 3-17. The sensors delay and analogue-to-digital conversion delay are represented as τ_d. A lead compensator H_d is added in the feedback loop.

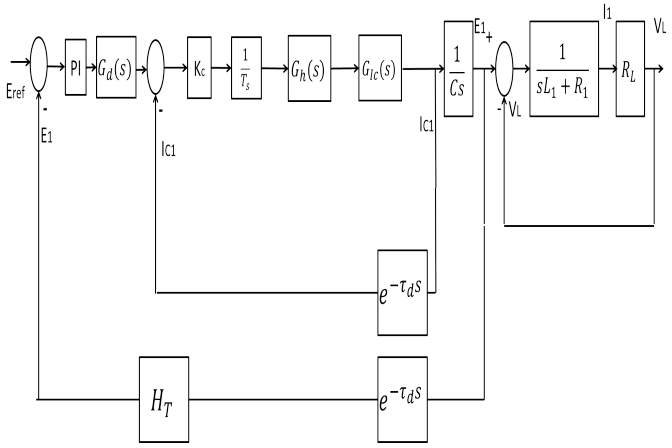


Figure 3-17: Control block diagram with consideration of time delay.

After the PWM reference is calculated, this value is held using a ZOH and used to calculate the duty ratio [52]. The transfer function of the ZOH is given as follows:

$$G_h(s) = \frac{1 - e^{-T_s s}}{s}. \tag{3.49}$$

$G_h(s)$ can be simplified in the frequency domain as follows:

$$G_h(j\omega) = \frac{1 - e^{-j\omega T_s}}{j\omega} = \frac{\sin(0.5\omega T_s)}{0.5\omega} e^{-j0.5\omega T_s} \approx T_s e^{-j0.5\omega T_s}. \tag{3.50}$$

From (3.50), the ZOH introduces a delay of half sampling period. The sampler is represented as $1/T_s$ in Fig. 3-17.

3.7 Three Phase Inverter Average Model in DQ Synchronous Frame

The three phase quantities calculated in (3.24), (3.25), and (3.26) can be transformed to the rotating (dq) synchronous frame by applying the transformation matrix:

$$\begin{bmatrix} X_d \\ X_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t + 2\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{3.51}$$

Applying the transformation matrix to the current and voltage quantities, we obtain the following:

$$i_{01d} = \frac{2}{3} \left[i_{01a} \sin(\omega t) + i_{01b} \sin(\omega t - 2\pi/3) + i_{01c} \sin(\omega t + 2\pi/3) \right] \tag{3.52}$$

$$i_{01q} = \frac{2}{3} \left[i_{01a} \cos(\omega t) + i_{01b} \cos(\omega t - 2\pi/3) + i_{01c} \cos(\omega t + 2\pi/3) \right] \tag{3.53}$$

$$i_{1d} = \frac{2}{3} \left[i_{1a} \sin(\omega t) + i_{1b} \sin(\omega t - 2\pi/3) + i_{1c} \sin(\omega t + 2\pi/3) \right] \tag{3.54}$$

$$i_{1q} = \frac{2}{3} \left[i_{1a} \cos(\omega t) + i_{1b} \cos(\omega t - 2\pi/3) + i_{1c} \cos(\omega t + 2\pi/3) \right] \tag{3.55}$$

$$e_{1d} = \frac{2}{3}\left[e_{1a}\sin(\omega t) + e_{1b}\sin(\omega t - 2\pi/3) + e_{1c}\sin(\omega t + 2\pi/3)\right] \tag{3.56}$$

$$e_{1q} = \frac{2}{3}\left[e_{1a}\cos(\omega t) + e_{1b}\cos(\omega t - 2\pi/3) + e_{1c}\cos(\omega t + 2\pi/3)\right]. \tag{3.57}$$

Taking the derivative of equations (3.52) and (3.53):

$$\begin{aligned}\frac{di_{01d}}{dt} = \frac{2}{3}\left[\frac{di_{01a}}{dt}\sin(\omega t) + \frac{di_{01b}}{dt}\sin(\omega t - 2\pi/3) + \frac{di_{01c}}{dt}\sin(\omega t + 2\pi/3)\right] \\ + \frac{2}{3}\omega\left[i_{01a}\cos(\omega t) + i_{01b}\cos(\omega t - 2\pi/3) + i_{01c}\cos(\omega t + 2\pi/3)\right]\end{aligned} \tag{3.58}$$

$$\begin{aligned}\frac{di_{01q}}{dt} = \frac{2}{3}\left[\frac{di_{01a}}{dt}\cos(\omega t) + \frac{di_{01b}}{dt}\cos(\omega t - 2\pi/3) + \frac{di_{01c}}{dt}\cos(\omega t + 2\pi/3)\right] \\ - \frac{2}{3}\omega\left[i_{01a}\sin(\omega t) + i_{01b}\sin(\omega t - 2\pi/3) + i_{01c}\sin(\omega t + 2\pi/3)\right]\end{aligned} \tag{3.59}$$

Substituting the derivatives in (3.24) into (3.58) and (3.59), and taking into account that the second terms in (3.58) and (3.59) are (3.53) and (3.52), respectively, the following equations are obtained:

$$\frac{dI_{01d}}{dt} = \omega I_{01q} - \frac{R_0}{L_0}I_{01d} - \frac{1}{L_0}\left[E_{1d} - U_d\right]. \tag{3.60}$$

$$\frac{dI_{01q}}{dt} = -\omega I_{01d} - \frac{R_0}{L_0}I_{01q} - \frac{1}{L_0}\left[E_{1q} - U_q\right]. \tag{3.61}$$

Similarly, the other DQ equations of the inverter can be derived in a similar manner by taking the derivative of the d and q equations of the variable, then, substituting the previous

equations. The following equations for the other output DQ currents and capacitor DQ voltages are shown:

$$\frac{dI_{1d}}{dt} = \omega I_{1q} - \frac{R_1}{L_1} I_{1d} + \frac{1}{L_1} \left[E_{1d} - V_{Ld} \right]. \tag{3.62}$$

$$\frac{dI_{1q}}{dt} = -\omega I_{1d} - \frac{R_1}{L_1} I_{1q} + \frac{1}{L_1} \left[E_{1q} - V_{Lq} \right]. \tag{3.63}$$

$$\frac{dE_{1d}}{dt} = \omega E_{1q} + \frac{1}{C} I_{01d} - \frac{1}{C} I_{1d}. \tag{3.64}$$

$$\frac{dE_{1q}}{dt} = -\omega E_{1d} + \frac{1}{C} I_{01q} - \frac{1}{C} I_{1q}. \tag{3.65}$$

Fig. 3-18 shows the DQ equivalent circuit model of a three phase inverter. All quantities in Fig. 3-18 are dc, hence, in the steady state inductors appear as short-circuits and capacitors as open-circuits. Notice that the equivalent circuit model in the synchronous frame includes cross-coupling terms. There are many decoupling techniques that can be used in the controller to eliminate these terms. The final equations of one inverter in the synchronous frame are shown below.

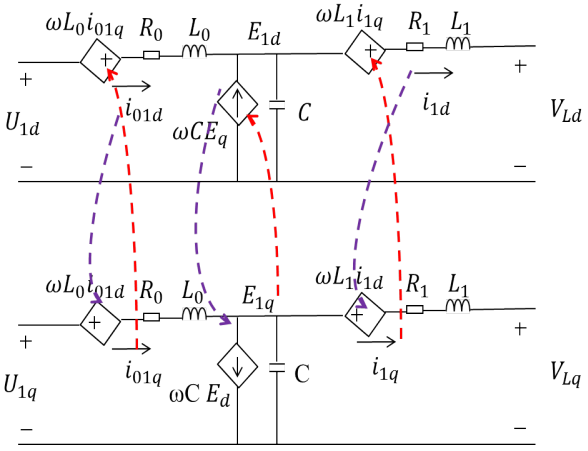


Figure 3-18: Equivalent circuit of a three phase inverter in the dq synchronous frame.

$$\frac{d}{dt}\begin{bmatrix} I_{01d} \\ I_{01q} \end{bmatrix} = \begin{bmatrix} -\frac{R_0}{L_0} & \omega \\ -\omega & -\frac{R_0}{L_0} \end{bmatrix} \begin{bmatrix} I_{01d} \\ I_{01q} \end{bmatrix} - \frac{1}{L_0} \begin{bmatrix} E_{1d} - U_d \\ E_{1q} - U_q \end{bmatrix} \tag{3.66}$$

$$\frac{d}{dt}\begin{bmatrix} E_{1d} \\ E_{1q} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \begin{bmatrix} E_{1d} \\ E_{1q} \end{bmatrix} + \frac{1}{C} \begin{bmatrix} I_{01d} - I_{1d} \\ I_{01q} - I_{1q} \end{bmatrix} \tag{3.67}$$

$$\frac{d}{dt}\begin{bmatrix} I_{1d} \\ I_{1q} \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L_1} & \omega \\ -\omega & -\frac{R_0}{L_0} \end{bmatrix} \begin{bmatrix} I_{1d} \\ I_{1q} \end{bmatrix} + \frac{1}{L_1} \begin{bmatrix} E_{1d} - V_{Ld} \\ E_{1q} - V_{Lq} \end{bmatrix} \tag{3.68}$$

3.8 Inverter Virtual Impedance Design

To improve the stability of parallel inverters in microgrids, many techniques have been proposed in the literature. Current-limiting techniques operate by limiting the reference voltage or current of voltage source or current source inverters, respectively [63]. Virtual impedance is another method that can be used to improve the control performance of inverters [51]. Virtual impedance control is used to adjust the output impedance of the inverter, resulting in better current distribution between the inverters, resonance damping, and harmonics mitigation at the point of common coupling (PCC) [64]. Control of virtual impedance can be divided into two categories:

1. Internal virtual impedance [62]: this concept is used for damping of filter resonance by modifying the PWM control signal directly.

2. External virtual impedance [31]: can be achieved by modifying the control reference of the inverter to improve the overall stability of the system and the power distribution.

3.8.1 Virtual Impedance and Resonance Damping

The load connected a the output of VSI may affect the resonance of the output filter. The effect of the load resistance on the damping can be explained from an energy point of view as explained in [62]: A small load resistance (assuming a fixed load voltage) will dessipate the resonance energy more quickly, and thus provides better damping than a large resistor. However, the effect of the load resistance on the damping is limited, and therefore an additional virtual impedance can be designed to further mitigate the resonance effect.

Fig. 3-19 shows an LCL filter with different possible locations of the virtual impedance. For virtual impedance parallel to the inductors or the capacitor (Z_{v2}, Z_{v4}, and Z_{v5}), differentiators are required in the controller [62, 65]. The virtual impedance in this case can be realized by dividing the voltage across the inductor or the capacitor over the required virtual impedance. On the other hand, the virtual impedance in series with the inductors or the capacitor (Z_{v1}, Z_{v3}, and Z_{v6}) can be realized by multiplying the current of the inductor or the capacitor by the required virtual impedance. Implementing a series virtual impedance is therefore considered easier than the parallel one since the former can be directly applied to the PWM modulator with simple multiplication and does not require extra voltage sensors. The differentiators in the case of parallel virtual impedance can be avoided by using multiloop control.

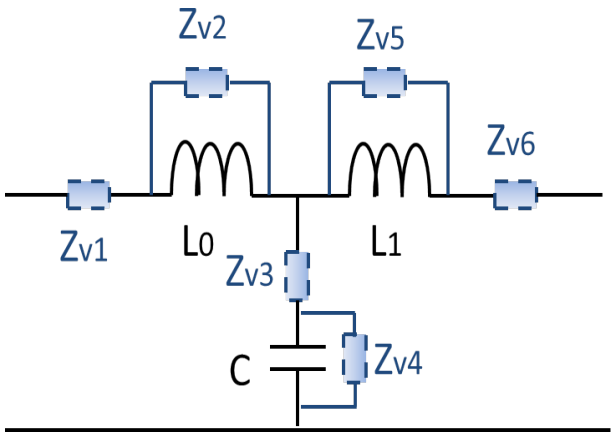


Figure 3-19: LCL filter with six possible locations of virtual impedance.

3.8.2 Virtual Impedance and Current Distribution

In the traditional Droop control method, the output impedance of the inverter may affect the power distribution between parallel inverters [66, 67]. This problem can be solved by controlling the output impedance of the parallel inverters in microgrids to achieve the desired power distribution [64, 67]. A proper design of the virtual impedance can alleviate the output impedance imbalance between the inverters [31].

A stable virtual impedance design can be achieved by dropping the reference voltage in proportion to the output current of the inverter, as follows:

$$V_{ref}^{*} = V_{ref} - Z_D(s) i_o \tag{3.69}$$

where $Z_D(s)$ is the virtual output impedance, V_{ref}^{*} is the reference voltage after adding the virtual impedance, V_{ref} is the no-load reference voltage, and i_o is the output current.

Fig. 3-20 shows the block diagram of a UPS with multiloop control and an additional loop for virtual impedance control. $Z_D(s)$ is the transfer function of the virtual impedance. The virtual impedance is added in series with the inverter. By multiplying the output current with the virtual impedance, the voltage drop is calculated. This voltage drop is then subtracted from the reference voltage.

The virtual impedance can be programmed to be resistive or reactive. A virtual resistive impedance can be implemented as:

$$Z_D(s) = R_D. \tag{3.70}$$

The virtual resistive impedance can be used to adjust the output impedance of the inverter to become more resistive, which in return reduces the mismatch and improves the current sharing without adding any power loss into the system [64]. The virtual impedance can also

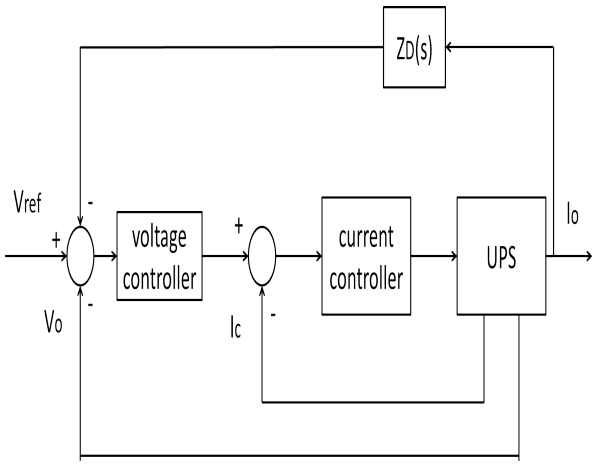


Figure 3-20: Block diagram of a UPS with multiloop control and virtual impedance control loop.

be designed so that the output impedance is predominantly inductive. In this case, a virtual output inductance is produced by emulating a real inductor by drooping the reference voltage proportional to the time derivative of the output current. The inductive virtual impedance is expressed as follows:

$$Z_D(s) = sL_D \tag{3.71}$$

where L_D is the virtual inductance.

In this case, the THD in the output voltage is normally high for nonlinear load since the virtual reactance is frequency-dependant [31, 64]. This problem can be avoided by replacing the pure derivative term in (3.71) with a high-pass filter. The reference voltage now becomes:

$$V^*_{ref} = V_{ref} - L_D \frac{s}{s + \omega_c} i_o \tag{3.72}$$

where ω_c is the cutoff frequency of the high-pass filter.

3.9 Summary

This chapter presented the average model of three phase inverter in the dq synchronous frame. Multi-loop control is used to damp the resonance of the output LCL filter. The multi-loop control considered in this work consists of a capacitor current minor loop and a capacitor voltage outer loop. The Bode plot was used to analyse the stability of the inverter. The control is performed in the synchronous frame because the PI controller has a zero error for DC quantities. A PLL is used to transform the three phase quantities to their equivalent dc signals.

Chapter 4

Communication-Based Current Distribution Control Scheme

In this chapter, a communication-based control scheme for parallel UPS systems is introduced. The control method is effective in sharing the load current equally between parallel inverters while minimizing the circulating current between them. It is assumed that the inverters can obtained information about the operating condition of other inverters. Specifically, the UPS units exchange information about their output currents. The information is exchanged by means of CAN bus, Ethernet, WiFi/WiMAX, Internet, power line communication (PLC), fiber-optic cables, or by means of other methods [68, 69].

4.1 Introduction

As discussed in Chapter 2, active load sharing (ALS) control techniques rely on information exchange of certain variables in the system between parallel inverters. Each UPS unit includes a control unit to calculate the reference voltage for that UPS. There is no Master or central control unit in the system. Any UPS can be connected or disconnected from the system without interruption in its operation. We consider a UPS unit with an output LCL filter connected to

the load. The control scheme relies on controlling the reference capacitor voltage of each inverter based on the measurement of its output current as well as the output currents of other parallel units.

Low bandwidth communication networks are often used to exchange information between the DG units. However, communication links have inherent time delays that might affect the performance of the system, any may cause stability problems in some cases [68]. In this section, the effect of communication delay between parallel UPS systems is investigated. The maximum limits on the time delay above which the system becomes unstable are calculated by recasting the system as a Cauchy problem, and calculating the eigenvalues of the system. Compensation techniques to solve this problem are presented and verified by simulation.

4.2 System Configuration

As mentioned previously, inverters operate in current-controlled or voltage-controlled modes, or a combination of both. Voltage-controlled inverters control the output voltage of the LC filter while current-controlled inverters control the output current. In the proposed configuration, an LCL filter is used at the output. The output current is indirectly controlled by regulating the capacitor voltage. The circuit configuration of the system is shown in Fig. 4-1a.

The main structure consists of a capacitor voltage outer loop and capacitor current inner loop. The output current (I_1) and load voltage (V_L) are indirectly controlled by calculating the reference value of the capacitor voltage and phase continuously based on current feedback signals from other modules. The system is distributed, which has the advantage that it is independent from a central unit that is vulnerable to failure. Each unit has its own current-sharing control unit to generate a voltage reference.

Fig. 4-1b shows the single phase equivalent circuit diagram of one inverter. The voltage of the capacitor is E_1 and the output current is i_1. The impedance of the load-side inductor

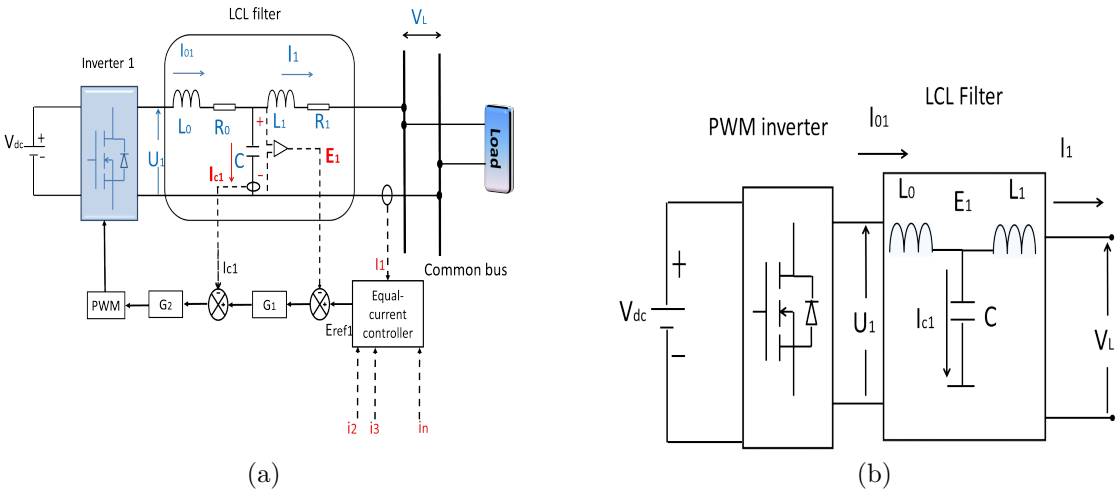


Figure 4-1: (a) Dual loop control of capacitor voltage and current in synchronous frame, (b) control block diagram.

is denoted as Z_1, which represents the impedance of the inductor L_1 and its equivalent series resistance R_1, and is calculated as:

$$Z_1 = R_1 + j\omega L_1 \tag{4.1}$$

where ω is the angular frequency ($\omega = 2\pi f$, f=50 Hz).

4.3 Control Algorithm

The following steps explain the control scheme of the current sharing method. For each inverter, the operation principle of the current-sharing controller (see Fig. 4-1a) is as follows:

1. The output currents of all inverters are measured and the average current is calculated:

$$\bar{I}_{ref1} = \frac{\bar{I}_1 + \bar{I}_2 + ... + \bar{I}_n}{n} = |I_{ref1}| \underline{/\beta_{ref1}} \tag{4.2}$$

where $\bar{I}_{ref1}$ is the reference current calculated at the controller of inverter 1, β_{ref_1} is the reference current phase, and n is the number of parallel inverters.

2. Convert the reference current to the dq-frame: $\bar{I}_{ref1} = I_{ref1d} + jI_{ref1q}$. Then, by applying KVL principle, the reference capacitor voltage ($\bar{E}_{ref1}$) is calculated as:

$$\begin{aligned} \bar{E}_{ref1} &= |E_{ref1}|\underline{/\delta_{ref1}} \\ &= V_{Lref} + \bar{Z}_1\bar{I}_{ref1} \\ &= V_{Lref} + (R_1 + j\omega L_1)(I_{ref1d} + jI_{ref1q}) \end{aligned} \tag{4.3}$$

where: $\bar{E}_{ref1}$ is the reference capacitor voltage of inverter 1, $\bar{Z}_1$ is the impedance of the output inductor of inverter 1 ($\bar{Z}_1 = |Z_1|\underline{/\theta_{Z1}} = R_1 + j\omega L_1$), and $|V_{Lref}|$ is the phase-to-ground reference load voltage (100 V rms in this paper).

The phase of load voltage is synchronised with the grid voltage, which is extracted by the PLL unit, and hence it is considered as the zero reference.

3. Finally, the dq-components of the reference capacitor voltage can be calculated based on (4.3) as follows:

$$E_{ref1d} = V_{Lref} + R_1 I_{ref1d} - \omega L_1 I_{ref1q} \tag{4.4}$$

$$E_{ref1q} = R_1 I_{ref1q} + \omega L_1 I_{ref1d} \tag{4.5}$$

The dq components of the reference voltage are used for local multi-loop control at each inverter as discussed in Section 3.

The phasor diagram in Fig. 4-2 shows the reference load voltage, reference current, and the construction of the reference capacitor voltage for inverter 1 with an inductive load. The

reference current is calculated using (4.2), and has a phase equal to β_{ref1}. The voltage drop on the load-side inductor is $(\bar{I}_{ref1}(R_1 + j\omega L_1))$. E_{ref1} is then calculated by adding the voltage drop on the inductor with the reference load voltage (V_{Lref}). This process enables indirect control of the output current by regulating the capacitor voltage of the inverter.

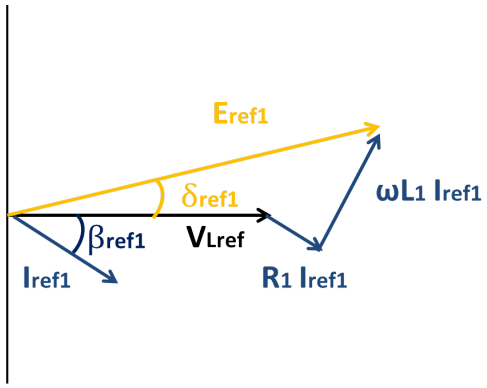


Figure 4-2: Phasor diagram showing the construction of reference capacitor voltage.

For n parallel inverter, by applying the proposed control algorithm, at steady-state, the system converges to one equilibrium state:

$$\begin{cases} I_1 = I_2 = ... = I_n = I_{load}/n \\ \overline{E}_1 = \overline{E}_2 = ... = \overline{E}_n = \overline{V}_{Lref} + \overline{Z}_1.\overline{I}_{ref} \\ \overline{V}_L = \overline{V}_{Lref}. \end{cases} \tag{4.6}$$

Notice that in the steady state all parallel inverters have equal capacitor voltages. The state guarantees that the circulating current is zero.

For inverters with different capacities, the current sharing can be controlled by controlling the ratio of the output inductors. Based on (4.3), and taking into consideration that the capacitor voltages of all inverters must be equal to eliminate the circulating current, the following equation is obtained:

$$\frac{I_1}{I_2} = \frac{Z_1}{Z_2}. \tag{4.7}$$

4.4 Small Signal Stability Analysis

The time average model of a system of two parallel inverters in synchronous DQ reference frame is used to investigate the stability margins of the system. The following set of equations

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} I_{0id} \\ I_{0iq} \end{bmatrix} = \dfrac{1}{L_0}\begin{bmatrix} U_{id} - E_{id} \\ U_{iq} - E_{iq} \end{bmatrix} + \begin{bmatrix} -R_0/L_0 & \omega \\ -\omega & -R_0/L_0 \end{bmatrix}\begin{bmatrix} I_{0id} \\ I_{0iq} \end{bmatrix} \\ \dfrac{d}{dt}\begin{bmatrix} E_{id} \\ E_{iq} \end{bmatrix} = \dfrac{1}{C}\begin{bmatrix} I_{0id} - I_{id} \\ I_{0iq} - I_{iq} \end{bmatrix} + \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}\begin{bmatrix} E_{id} \\ E_{iq} \end{bmatrix} \\ \dfrac{d}{dt}\begin{bmatrix} I_{id} \\ I_{iq} \end{bmatrix} = \dfrac{1}{L_1}\begin{bmatrix} E_{id} - V_{Ld} \\ E_{iq} - V_{Lq} \end{bmatrix} + \begin{bmatrix} -R_1/L_1 & \omega \\ -\omega & -R_1/L_1 \end{bmatrix}\begin{bmatrix} I_{id} \\ I_{iq} \end{bmatrix} \end{cases} \tag{4.8}$$

where $i = 1, 2$ denotes the index of the inverter, L_0 and R_0 are the inverter-side inductance and resistance, L_1 and R_1 are the output-side inductance and resistance, and C is the capacitance. For simplicity, the two inverters have the same LCL filters parameters. Other current and voltage variables are as shown in Fig. 4-1b. The PWM output voltage of inverter i in the synchronous frame, U_{idq}, is represented as:

$$U_{idq} = K_{pwm}\left[k_c k_p e_{idq} + k_i \int e_{idq} + C\frac{de_{idq}}{dt}\right] \tag{4.9}$$

where e_{idq} is the voltage error signal ($e_{1dq} = E_{ref1dq} - E_{1dq}$, $e_{2dq} = E_{ref2dq} - E_{2dq}$). E_{ref1dq} is as shown in (4.4).

A complete state space model of two parallel inverters operating under the proposed scheme can now be derived based on the time average model around the equilibrium point. Using (4.4), (5.14), and (5.15), and applying small signal perturbations, the state space model in matrix form can be described as:

$$\Delta\dot{X} = A\Delta X + \frac{1}{L_0}\Delta U \tag{4.10}$$

where ΔX is the state vector,

$\Delta X = [\Delta i_{01d}\ \Delta i_{01q}\ \Delta E_{1d}\ \Delta E_{1q}\ \Delta i_{1d}\ \Delta i_{1q}\ \int \Delta e_{1d}\ \Delta e_{1q}\ \Delta i_{02d}\ \Delta i_{02q}\ \Delta E_{2d}\ \Delta E_{2q}$ $\Delta i_{2d}\ \Delta i_{2q}\ \int \Delta e_{2d}\ \Delta e_{2q}\ ]^T$.

ΔU is the system input,

$\Delta U = [\Delta U_{1d}\ \Delta U_{1q}\ \Delta U_{2d}\ \Delta U_{2q}\ ]^T$, A is the state matrix.

$$A = \begin{bmatrix} A_{ii} & A_{ij} \\ A_{ij} & A_{ii} \end{bmatrix}, A_{ii} = \begin{bmatrix} \frac{-R_0}{L_0} & \omega & \frac{-1}{L_0} & 0 & 0 & 0 & 0 & 0 \\ -\omega & \frac{-R_0}{L_0} & 0 & \frac{-1}{L_0} & 0 & 0 & 0 & 0 \\ \frac{1}{C} & 0 & 0 & \omega & -\frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & -\omega & 0 & 0 & -\frac{1}{C} & 0 & 0 \\ 0 & 0 & \frac{1}{L_1} & 0 & -\frac{R_1-R_L}{L_1} & \omega & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_1} & -\omega & -\frac{R_1-R_L}{L_1} & 0 & 0 \\ 0 & 0 & -1 & 0 & \frac{R_1}{2} & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & \frac{\omega L_1}{2} & 0 & 0 & 0 \end{bmatrix},$$

$$A_{ij} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{-R_L}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{-R_L}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{R_1}{2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{\omega L_1}{2} & 0 & 0 & 0 \end{bmatrix}. \tag{4.11}$$

The system input, ΔU, can be represented in terms of the state variables. Based on (4.4), (5.14), and (5.15), the system input is represented as:

$$\Delta U = B\Delta X \tag{4.12}$$

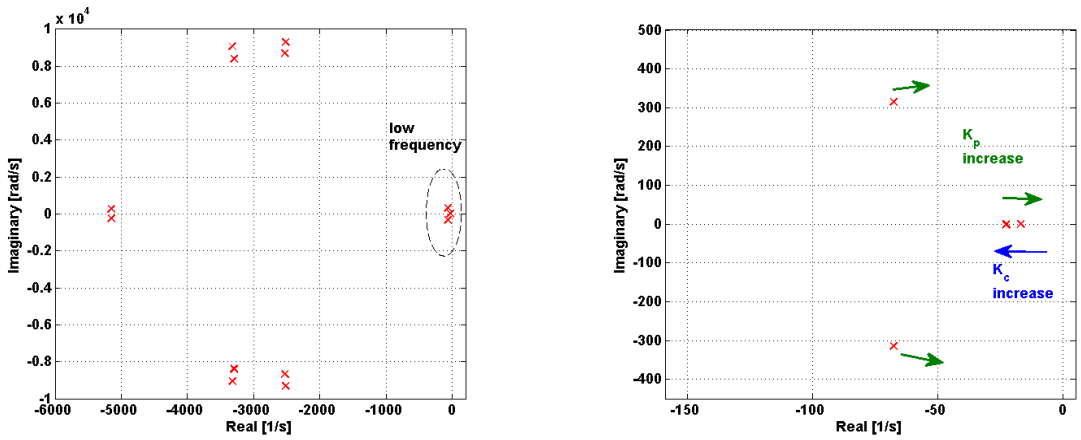
$$B = \begin{bmatrix} B_1 & B_3 & 0 & B_2 & B_4 \\ B_2 & B_4 & 0 & B_1 & B_3 \end{bmatrix}^T,$$

$$\begin{bmatrix} B_1 \\ B_2 \\ B_3 \\ B_4 \end{bmatrix} = \begin{bmatrix} -k_c & 0 & -k_c k_p & 0 & k_c(1 + \frac{R_1 k_p}{2} - \frac{\omega^2 L_1 C k_f}{2}) & 0 & k_c k_i & 0 \\ 0 & -k_c & 0 & -k_c k_p & k_c \omega (k_p L_1 + C k_f R_1) & k_c & 0 & k_c k_I \\ 0 & -k_c & 0 & -k_c k_p & \frac{k_c}{2}(k_p \omega L_1 + \omega C k_f R_1) & k_c & 0 & k_c k_i \\ 0 & 0 & 0 & 0 & \frac{k_c}{2}(k_p \omega L_1 + \omega C k_f R_1) & & & \end{bmatrix}. \tag{4.13}$$

The closed-loop system can now be represented as:

$$\Delta \dot{X} = (A + B)\, \Delta X. \tag{4.14}$$

The stability of the system can be investigated by calculating the eigenvalues of (5.20). Fig. 4-3a shows the poles of the system for $k_c = 0.02$, $k_p = 50$, $k_i = 2000$. All poles are in the left hand plane, which proves that the system is stable. To investigate the effect of the gains in the inner current loop and outer voltage loop on the stability of the system, the low-frequency poles will be considered since they are close to the imaginary axis. Fig. 4-3b shows the dominant poles of the system (marked with a circle in Fig. 4-3a). Increasing the gain of the current loop (k_c) moves the poles to the left, resulting in faster response. Increasing the proportional gain of the voltage loop (k_p), on the other hand, moves the eigenvalues to the right, which means that excessive gain in the voltage loop results in slow dynamic response and reduces the stability margin of the system.



(a) (b)

Figure 4-3: (a) Eigenvalues of a system of two parallel UPS units with $k_c = 0.02$, $k_p = 50$, $k_i = 2000$, (b) effect of k_c and k_p on low-frequency eigenvalues.

4.5 Communication Delay

4.5.1 Effect of communication delay on dynamic performance of the system

Exchanging information about operating condition between inverters inevitably includes time delay. The delay increases with the increase of distance between the units [30, 49]. Time delay also depends on the method used to send information (for example: wires, CAN bus, Wi-Fi, PLC (Power Line Communication), etc). Thus, the delay is expected to affect the dynamic performance of the system, and might result in deviation of load voltage and current from their reference values, or might cause instability in some extreme cases. The problem can also be extrapolated to micro-grids where the delay is significantly larger [10, 24].

Suppose that two UPS units are connected in parallel. Equation (4.2) is used to calculate the reference current for each inverter. For UPS 1, the delay in measuring its own output current is negligible, but there will be delay in acquiring the value of output current of UPS 2 (I_2). Suppose that this delay is τ_c, then, the reference current at UPS 1 is:

$$\bar{I}_{ref1} = \frac{\bar{I}_1 + \bar{I}_2.e^{-j\frac{2\pi\tau_c}{T}}}{2} \tag{4.15}$$

where T is the time period of the fundamental signal (20 ms for frequency 50 Hz).

Similarly, for UPS 2, the reference current is calculated as:

$$\bar{I}_{ref2} = \frac{\bar{I}_1.e^{-j\frac{2\pi\tau_c}{T}} + \bar{I}_2}{2}. \tag{4.16}$$

To highlight the effect of communication delay on the dynamic performance of the system, two parallel inverters will be considered with two different values of delay: 5 ms and 11 ms. Fig. 4-4 shows the magnitudes of the output currents of the inverters for the two cases. Notice that for a delay of 5 ms, the system is stable and the output currents coalesce to the equilibrium point with equal value. On the other hand, for a delay of 11 ms, the system is unstable.

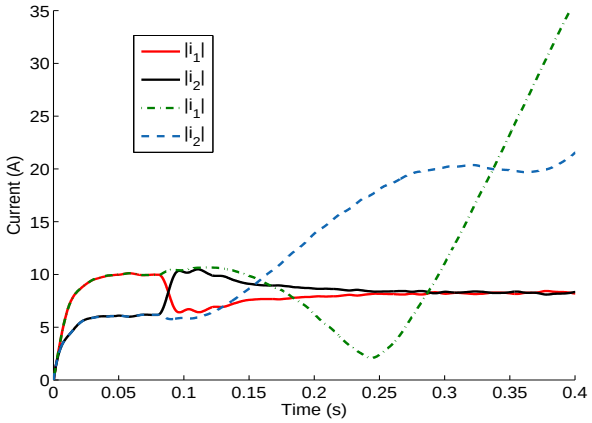


Figure 4-4: Output currents of two parallel inverters under proposed control for two cases: delay=5 ms (solid lines) and 11 ms (dashed lines).

4.5.2 Compensation of communication delay

To solve the problem of time delay between UPSs, the following approach is proposed:

1. Each inverter adds intentional delay to its own measured output current that is equal to

the delay in the signal from the other unit (τ).

2. The reference phase at the PLL is compensated to take into account the delay. The new reference phase is:

$$\theta_{new} = \theta_{ref} - \frac{\tau}{T}.2\pi \tag{4.17}$$

where T is the time period of the fundamental signal (20 ms for 50 Hz).

Fig. 4-5a and Fig. 4-5b demonstrate the time delay compensation as well as the phase compensation at the PLL.

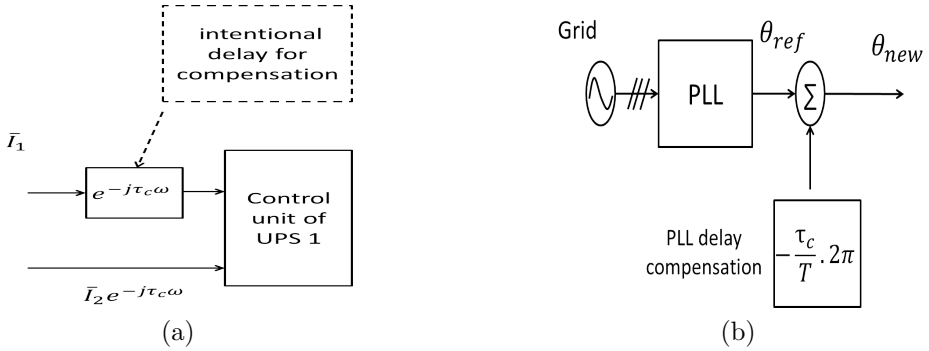


Figure 4-5: (a) Time delay compensation at UPS 1, (b) phase compensation at PLL.

By applying the compensation techniques the system can operate even with a large time delay. Fig. 4-6 shows the output currents of the two parallel inverters with a 15 ms delay.

4.6 Control scheme simulation and verification

4.6.1 Two parallel inverters

MATLAB Simulink is used to generate all the simulation results. First, two parallel UPS units are connected in parallel to a load. The specifications of the inverters are shown in Table 4.1. The two inverters are identical. For the first part of simulation verification, the inverters are

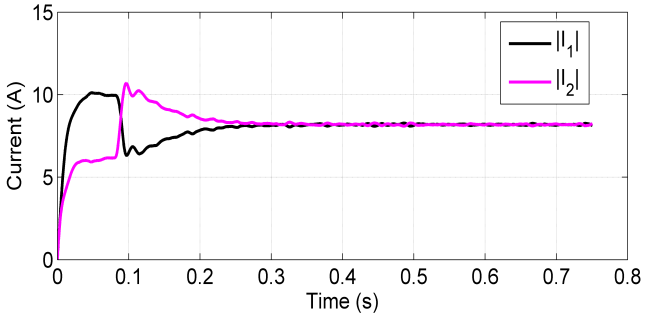


Figure 4-6: Output currents of two parallel inverters under proposed control with 15 ms time delay with compensation

connected to a 5 kW load, then, a step load is applied where the load is increased to 8 kW. Fig. 4-7 shows the results of simulation for this case.

Table 4.1: Specifications of one inverter unit.

Specification	Value	Component	Value
V_{dc}	400 V	R_0	0.04 Ω
V_L	100 V_{rms}	L_0	0.6 mH
Switching frequency	15 kHz	C	40 μF
Output frequency	50 Hz	R_1	0.08 Ω
Rated power	5 kVA	L_1	1.2 mH

The magnitude and phase angle of the output currents are shown in Fig. 4-7a. The output currents are equal and have a zero phase angle. The reference phase is the grid and a PLL is used to generate this reference. Hence, a zero phase indicates that the currents are in-phase with the utility voltage. The load voltage is also synchronized with the utility as shown in Fig. 4-7d which shows the rms value of the load voltage and its phase angle. Since the load is resistive, the currents are in-phase with the load voltage. Notice that the output currents quickly coalesce to the steady state. Notice also that load variation does not cause disturbance on the system. At t=0.5 s the output currents increase at the same rate and the operation point moves to a new state with equal load current distribution.

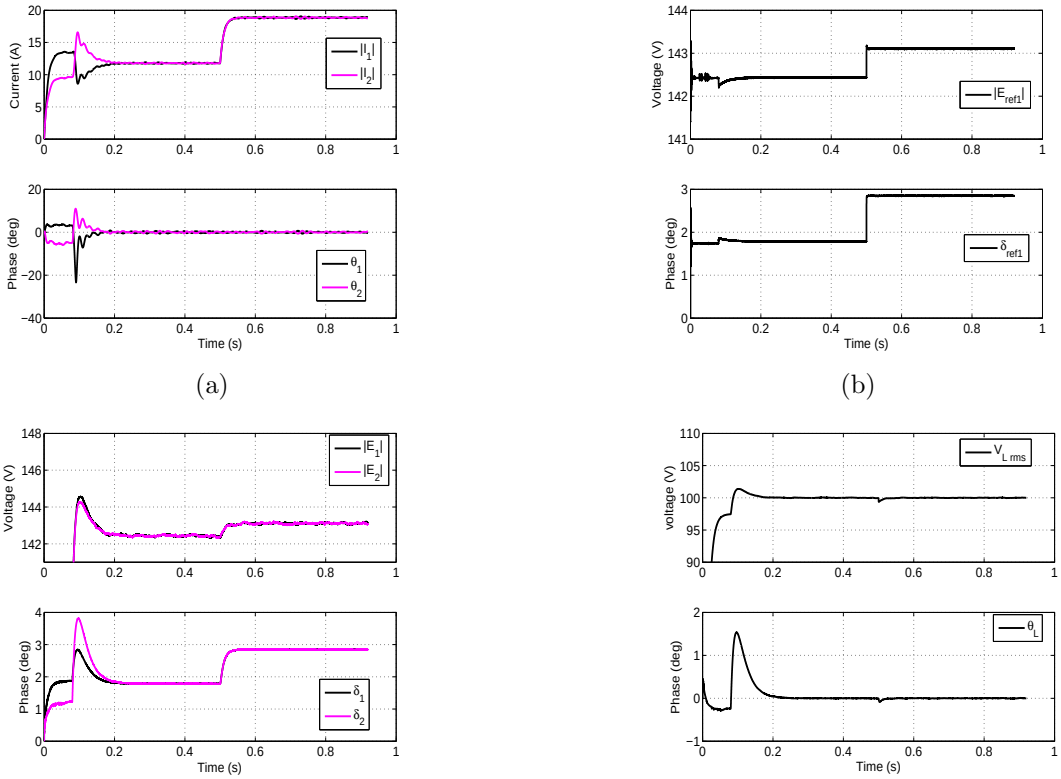


Figure 4-7: Two parallel inverters operating under the proposed communication-based control a) output currents and phase, b) reference capacitor voltage and phase of inverter 1, c) capacitor voltages and phase angles of the two inverters and d) load voltage and phase.

The capacitors voltages and phase angles of the two inverters are shown in Fig. 4-7c. The reference capacitor voltage and phase for inverter 1 are shown in Fig. 4-7b. The reference capacitor voltage and phase angles are calculated using (4.4) and(4.5) at the controller of each UPS. For a load of 5 kW and a load phase voltage of 100 V_{rms}, and using the parameters in Table 4.1, the dq components of the reference capacitor voltage are calculated as: E_{ref1d} = 142.36 V and E_{ref1q} = 4.438 V, which is converted to polar coordinates as $|E_{ref1}|$= 142.43 V and δ_{ref1} = 1.785°. The capacitors voltages and phase angle of both inverters are shown in Fig. 4-7c, which follow the reference commands. Notice that the change in the load does not cause disturbance in the load voltage and current. When the load is increased, the reference capacitor voltage is increased as well. The waveforms of the capacitor voltages, output currents, capacitor currents, inverter-side inductors currents, and load voltage and current are shown in Fig. 4-8.

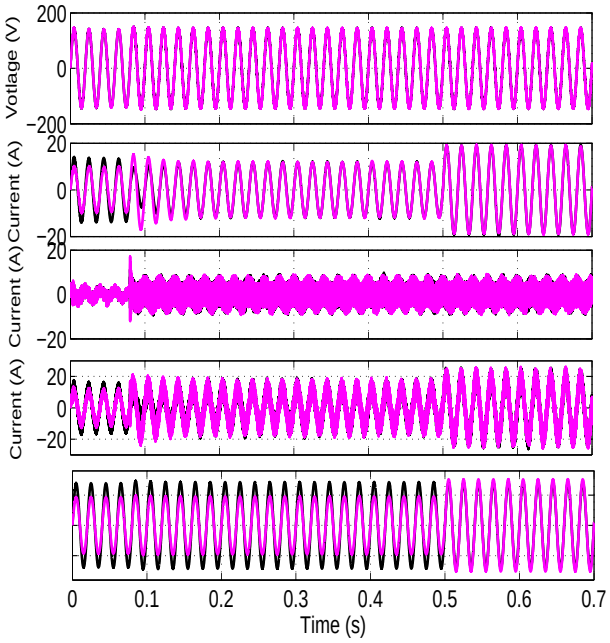


Figure 4-8: Waveforms from top to bottom: capacitor voltages, output currents, capacitor currents, inverter-side currents, and load voltage (black, 100 v/div) and load current (purple, 25 A/div)

4.6.2 Connecting and disconnecting units

One of the attractive features of parallel redundant UPS systems is the plug-and-play capability, which enables connecting additional parallel units to the system to meet the load demand while the system is operating. Moreover, there is a possibility that some units have to be disconnected from the system for maintenance or due to a fault. It is essential that the system can detect the fault and adjust the control so that continuous power is delivered to the load. In this subsection, a load of 4 kW is connected to one UPS. Then, a second UPS is added to the system to assist UPS 1 for a period of time before it is disconnected again. The purpose of this simulation case is to test the capability of the system to add or remove units without interruption in the power.

The results are summarized in Fig. 4-9, Fig. 4-10, and Fig. 4-11, which show the output currents, capacitor voltages, and load voltage, respectively. The procedure to connect units to the system is explained in the following steps:

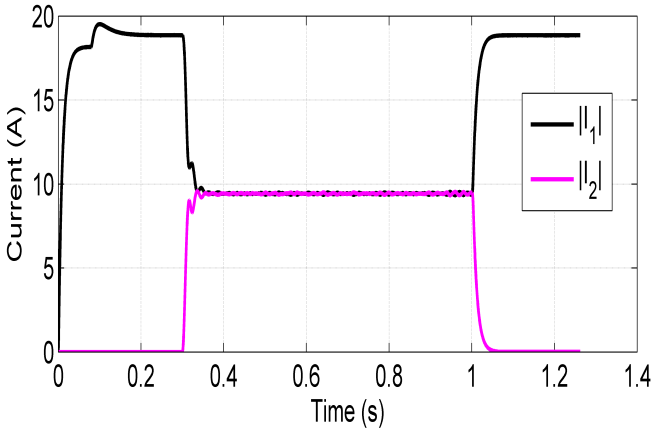


Figure 4-9: Output currents of two inverters, inverter 2 is connected at t=0.3 s and disconnected at t=1 s

1. The capacitor voltage of the new UPS is fixed at a constant value, equal to the reference load voltage (V_{Lref}).

2. The UPS is connected to the common load node. Since the capacitor voltage is equal to

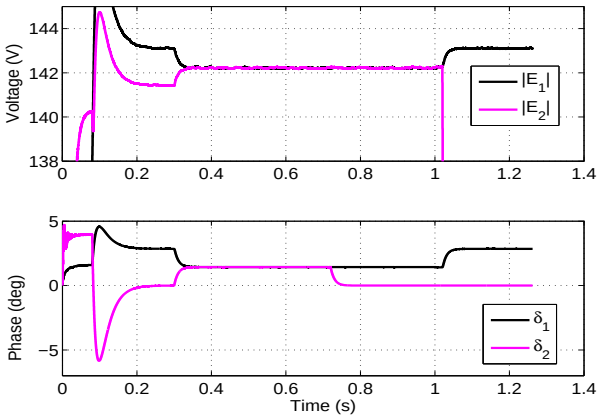


Figure 4-10: Capacitor voltages of two inverters, inverter 2 is connected at t=0.3 s and disconnected at t=1 s

the load voltage, the output current of the new UPS is zero.

3. The new UPS sends signals to all active units in the system to establish that it is ready to operate. In return, all operating units send information about their output currents to the new UPS.

4. The UPS calculates the reference current and reference capacitor voltage based on the information from other units and the number of units according to equations (4.15) and (4.3). At the same time, the operating units calculate update the number of units n in the controller, and calculate a new reference accordingly. The operating units remain operating in the current state waiting for a signal from the new UPS to adjust the reference voltage according to the new state.

5. The new UPS sends a signal to all parallel units indicating the beginning of its operation and the system operates at a new state with equal currents.

Disconnecting on unit might be done intentionally (for maintenance or due to light load condition), or due to a fault in one unit. In both cases, the operating units need to update the number of parallel inverters in the controller n. In the case of fault, the process must be fast

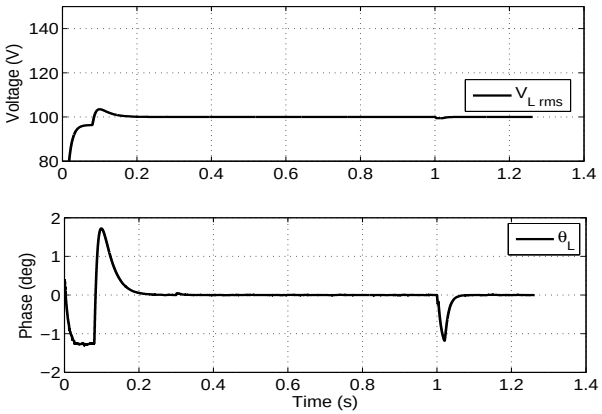


Figure 4-11: Load voltage and phase when two inverters are connected in parallel, inverter 2 is connected at t=0.3 s and disconnected at t=1 s

enough to avoid any interruption in the system. The procedure to disconnect a unit from the system is summarized in the following steps:

1. When the signal from the UPS with fault is lost, the other UPS units update n and calculate the new reference.

2. The reference is updated immediately and the system keeps operating.

4.6.3 Inverters with different capacities

For inverters with different capacities, the current sharing can be controlled by controlling the ratio of the output inductors. Based on (4.3), and taking into consideration that the capacitor voltages of all inverters must be equal to eliminate the circulating current, the following equation is obtained:

$$\frac{I_i}{I_j} = \frac{Z_j}{Z_i} \tag{4.18}$$

where i and j indicate the indices of the inverters.

Equation (4.18) shows that the ratio of output currents of two inverters is inversely propor-

tional to the ratio of their inductors. If the total load current is I_L, and the number of parallel inverters is n, then the following equations are deduced:

$$I_1 + I_2 + \cdots + I_n = I_L. \tag{4.19}$$

Assume that all parallel inverters have the same inductor (with impedance Z_1), except inverter j, which has an inductor with impedance Z_j. Then, equation (4.19) reduces to the following form:

$$(n-1)I_1 + I_j = I_L. \tag{4.20}$$

Next, multiply the equation by Z_j/Z_1, and taking into consideration equation (4.18), the following equations for I_1 and I_j are obtained:

$$I_1 = \frac{Z_j}{Z_1 + (n-1)Z_j} I_L \tag{4.21}$$

$$I_j = \frac{Z_1}{Z_1 + (n-1)Z_j} I_L. \tag{4.22}$$

Consider the case that $Z_j = 0.5Z_1$. Then, the output currents of the inverters become:

$$I_1 = \frac{1}{1+n} I_L \tag{4.23}$$

$$I_j = \frac{2}{1+n} I_L. \tag{4.24}$$

To demonstrate the case when some inverters have different capacities, we consider the case that three parallel inverters with inverters 1 and 2 have the same capacity and their inductors are equal to the value in Table 4.1, and inverter 3 has twice the capacity of inverter 1 (its

inductor has half the value of inverters 1 and 2). The inverters are connected to a 10 kW load, which is then increased to 14 kW. The output currents of the inverters are shown in Fig. 4-12. The currents of inverter 1 and 3 are equal, while the current of inverter 2 is twice the value of the other inverters. The change in the load does not change the distribution between the inverters.

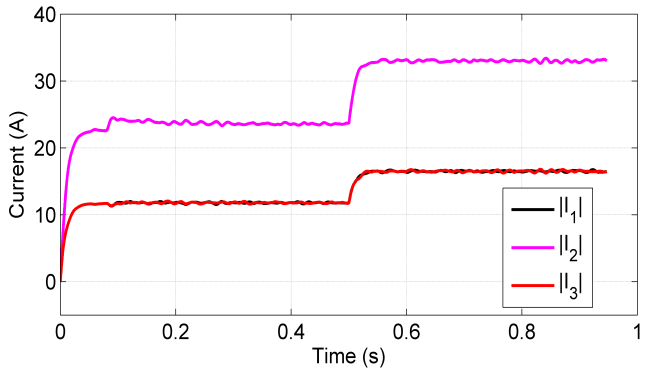


Figure 4-12: Output currents for three inverters controlled using communication-based control scheme with inverters 1 and 3 have the same capacity and inverter 2 have twice the capacity of inverter 1.

The capacitors voltages and phase angles are shown in Fig. 4-13 and are all equal which means that there is not circulating current. Finally, the load voltage and phase as shown in Fig. 4-14 follow the reference value.

4.7 Summary

A control scheme for parallel redundant UPS systems was introduced in this chapter. The control technique offers the following advantages:

- Each UPS has a control unit to govern its operation without relying on a secondary control or commands from a central controller.

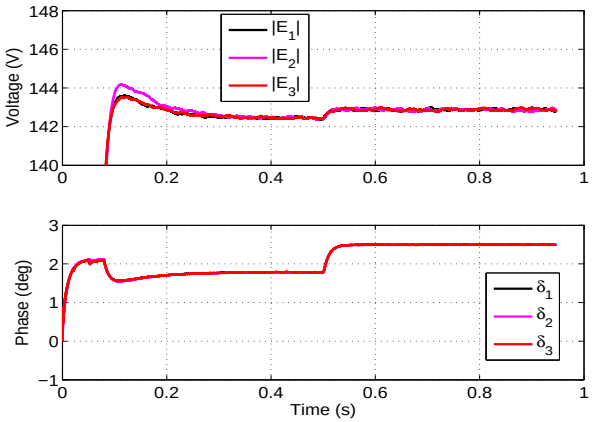


Figure 4-13: Capacitors voltages for three inverters controlled using communication-based control scheme with inverters 1 and 3 have the same capacity and inverter 2 have twice the capacity of inverter 1.

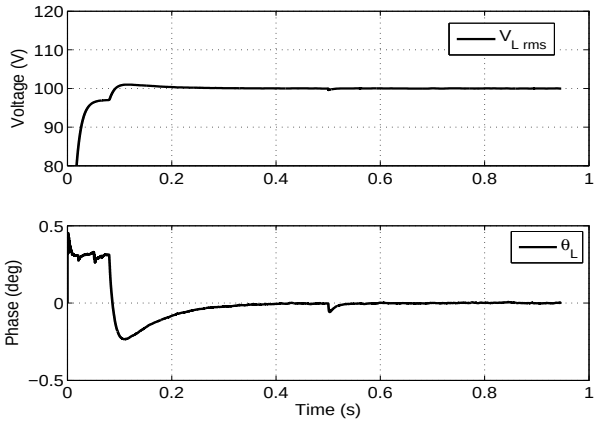


Figure 4-14: Load voltage for three inverters controlled using communication-based control scheme with inverters 1 and 3 have the same capacity and inverter 2 have twice the capacity of inverter 1.

- The system enables the connection/disconnection of the UPS units from the system without interruption.
- The circulating current is mitigated due to the fact that all parallel units are controlled such that their capacitors' voltages are equal.
- The system is robust against load variations.

Chapter 5

Autonomous Control of Parallel UPS Systems

In Chapter 4, a communication-based current distribution control scheme is presented. The method enables load current distribution between parallel UPS units while minimizing the circulating current to zero. Although the method is effective in distributing the currents, the fact that the system requires exchange of information between the UPS units limits the expandability and the physical locations of the UPSs. For a system with UPS units distributed over a relatively large area, this system adds limitations. Moreover, the reliability of such systems is reduced due to the existence of communication links [18]. In this chapter, the method developed in Chapter 4 is extrapolated to operate without information exchange. The parallel inverters do not need to exchange any information. The same inverter configuration used in Chapter 4 is used here. The control scheme uses the output current of each inverter to automatically adjust the reference capacitor voltage, such that the load voltage remains constant and equal to the reference value. Hence, the control scheme is called current-dependent capacitor voltage control (CCVC).

5.1 Introduction

The basic principle of the Droop method is to alter the system's voltage and frequency to achieve equal power distribution between parallel inverters. The Droop is an autonomous control technique and can be viewed as an improvement on the communication-based schemes in terms of increased reliability and flexibility. However, as mentioned in Chapter 2, there are disadvantages to this method.

In an attempt to overcome some of the disadvantages of the Droop, we present in this chapter a new control technique that is fundamentally different from the available schemes in the open literature. Instead of controlling the voltage level and frequency of the system (Droop control), we control the voltage of the filter capacitor. This results in a constant load voltage regardless of the load conditions. The second difference from the droop control is that instead of the system frequency, the phase of the capacitor voltage is changed. The output current of each inverter is used to control the voltage and phase of the capacitor.

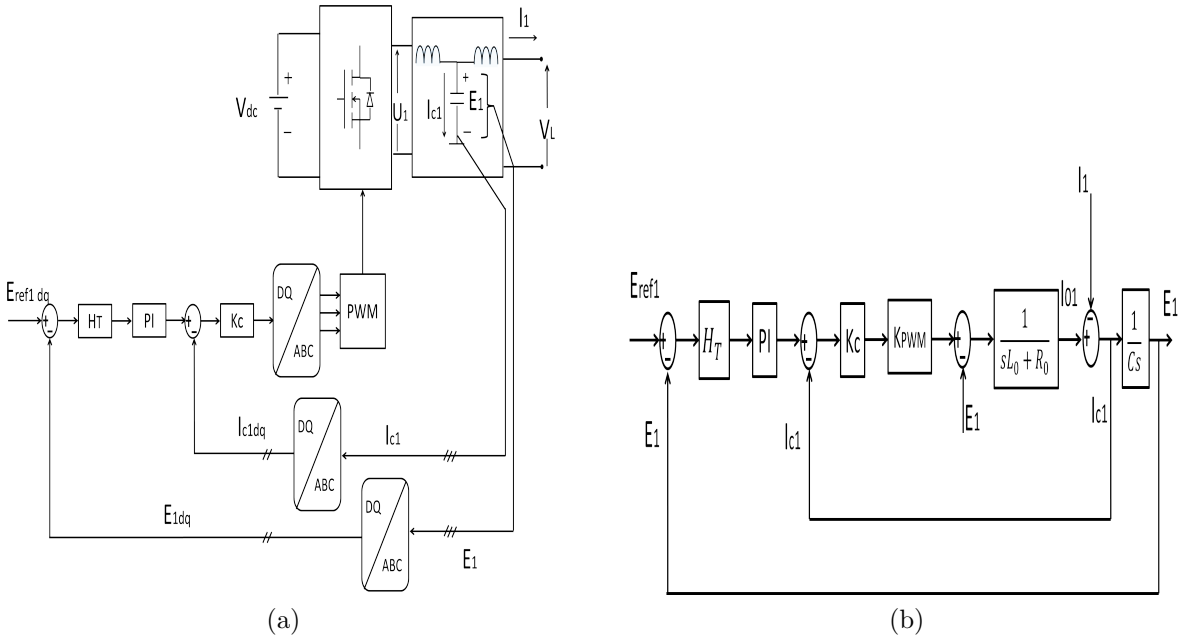


Figure 5-1: (a) Dual loop control of capacitor voltage and current in synchronous frame, (b) control block diagram.

5.2 Proposed autonomous control scheme

Chapter 3 presented the internal multi-loop control of each inverter. This section presents an autonomous control mechanism to generate the reference capacitor voltage of each inverter. The proposed control has the following characteristics:

1. Depends solely on locally-measurable variables.
2. Guarantees a fixed load voltage (V_L in Fig. 5-1a), in terms of amplitude and frequency.
3. Eliminates circulating current between parallel units.
4. Distributes the output currents equally between the parallel UPS modules.

Fig. 5-1a shows the multi-loop controller of inverter 1. The generation of the reference capacitor voltage (E_{ref1dq}) will be discussed in this chapter. The block diagram of the closed-loop controller of the inverter is shown in Fig. 5-1b. To improve the transient response, decoupling terms are applied to the digital control. The inner loop is the capacitor current loop and the outer loop is the capacitor voltage loop. For more information about the multi-loop control refer to Chapter 3.

5.2.1 Thevenin equivalent circuit

Each inverter can be represented in the dq synchronous frame, as shown in Fig. 5-2a [77]. The three phase voltages are assumed to be balanced and the reference frame rotates at the same angular speed of the sinusoidal inputs (ω_0).

The voltages E_{1d} and E_{1q} represent the dq components of the capacitor voltages of inverter 1, V_{Ld} and V_{Lq} represent the dq components of the load voltage. In the synchronous frame, each variable is related to a dc quantity in the steady state, hence, the inductors appear as short circuits. By applying KVL:

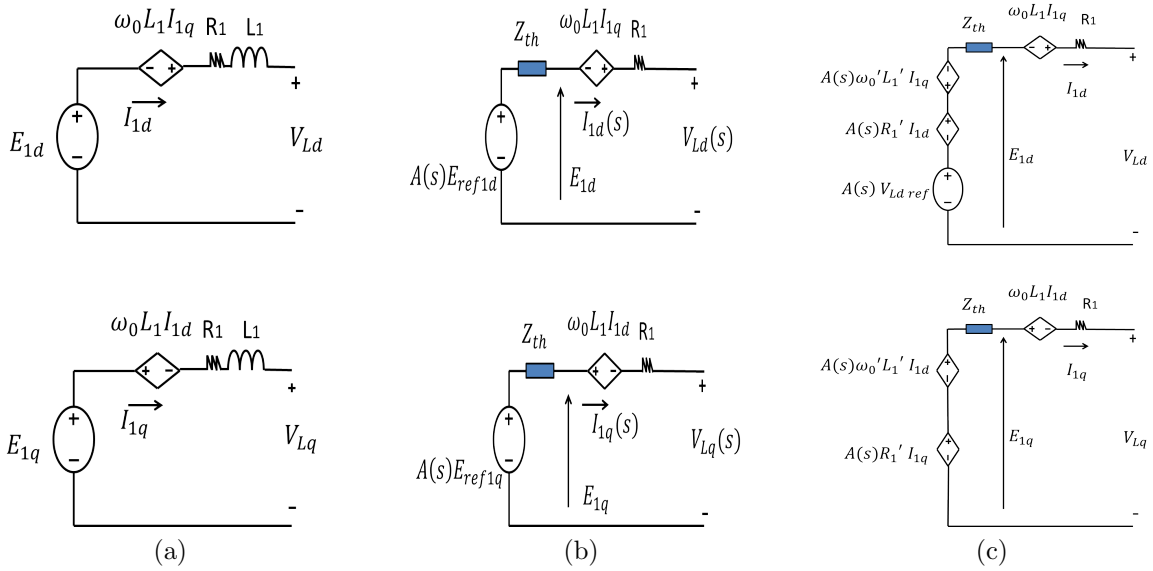


Figure 5-2: (a) Representation of two parallel inverters connected to a load, (b) Thevenin equivalent circuit of inverter 1, (c) Equivalent circuit diagram of inverter 1 with autonomous control.

$$V_{Ld} = E_{1d} - R_1 I_{1d} + \omega_0 L_1 I_{1q}. \tag{5.1}$$

$$V_{Lq} = E_{1q} - R_1 I_{1q} - \omega_0 L_1 I_{1d}. \tag{5.2}$$

Each inverter can be modelled as an equivalent Thevenin circuit in the Laplace domain [78]. Based on the block diagram of one inverter (Fig. 5-1b), and by adding the decoupling terms to improve the transient performace, the closed-loop inverter can be represented equivalently by a voltage source and an equivalent Thevenin series impedance [71]:

$$E_{1dq} = \frac{G_{PI}k_c}{CL_0s^2 + Cs(R_0 + k_c) + G_{PI}k_c + 1} E_{ref1dq} - \frac{sL_0 + R_0}{CL_0s^2 + Cs(R_0 + k_c) + 1} I_{1dq}. \tag{5.3}$$

Equation (5.3) can be re-written as:

$$E_{1dq} = A(s)E_{ref1dq} - Z_{th}(s)I_{1dq} \tag{5.4}$$

where:

$$A(s) = \frac{k_p k_c s + k_i k_c}{CL_0 s^3 + Cs^2(R_0 + k_c) + (k_p k_c + 1)s + k_i k_c} \tag{5.5}$$

$$Z_{th}(s) = \frac{s^2 L_0 + R_0 s}{CL_0 s^3 + Cs^2(R_0 + k_c) + (k_p k_c + 1)s + k_i k_c}. \tag{5.6}$$

Fig. 5-2b shows the representation of (5.4), where $A(s)$ and $Z_{th}(s)$ are as shown in (5.5) and (5.6), respectively, and Z_1 is the impedance of the load-side inductor:

$$\bar{Z}_1 = R_1 + j\omega L_1 \tag{5.7}$$

where ω is the angular frequency ($\omega = 2\pi f$, f=50 Hz).

Ideally, in (5.4), E_1 must track the reference E_{ref1} at the fundamental frequency with unity gain and zero phase, while rejecting any load current influence [61]. Using the same parameters of the capacitor current and capacitor voltage controllers used in Section III (k_c=0.02, k_i=2000, and choosing a proportional gain of k_p=10), the Bode plots of $A(s)$ and $Z_{th}(s)$ are shown in Fig. 5-3. Notice that $A(s)$ has a unity gain and zero phase offset at 50 Hz (314 rad/s). Notice also that $Z_{th}(s)$ is very small at the fundamental frequency.

Substituting the equation of E_{1dq} from (5.4) into (5.1) and (5.2):

$$V_{Ld} = A(s)E_{ref1d} - Z_{th}I_{1d} - R_1 I_{1d} + \omega_0 L_1 I_{1q} \tag{5.8}$$

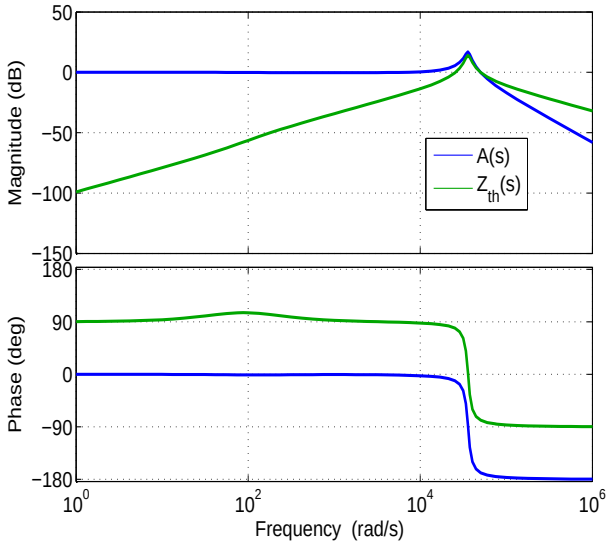


Figure 5-3: Bode plot of closed-loop transfer function $A(s)$ and equivalent Thevenin impendance $Z_{th}(s)$ with controllers parameters chosen as: k_c=0.02, k_i=2000, and k_p=10.

$$V_{Lq} = A(s)E_{ref1d} - Z_{th}I_{1q} - R_1I_{1q} - \omega_0 L_1 I_{1d}. \tag{5.9}$$

Fig. 5-2b shows the representation of (5.8) and (5.9). Under ideal conditions, $A(s)$=1, Z_{th}=0, and hence $E_{1dq} = E_{ref1dq}$.

5.2.2 Autonomous control equation

It follows from (5.8) and (5.9) that the aim of the autonomous controller is to generate the reference capacitor voltage (E_{ref1dq}) such that: a) the load voltage is equal to a predetermined fixed value (V_{Lref}), and b) all parallel inverters will have equal capacitor voltages. The second condition is important to ensure that there is no circulating current between the inverters. The proposed autonomous control scheme relies on varying the capacitor reference voltage of each inverter as a function of its own output current. The following equation describes the operation of the proposed autonomous control scheme for inverter i:

$$\bar{E}_{refi} = \bar{V}_{Lref} + \bar{Z}_i^{'}.\bar{I}_i \tag{5.10}$$

where I_i is the output current of inverter i, $\bar{E}_{refi}$ is its reference capacitor voltage , $\bar{V}_{Lref}$ is the reference load voltage, and $\bar{Z}_i^{'}$ is the compensation impedance of unit i. The compensation impedance is normally equal to the impedance of the output inductor ($\bar{Z}_1$) and can alternatively be written in the form $Z_i^{'} = R_i^{'} + j\omega_0^{'}L_i^{'}$, where $\omega_0^{'}$ is a constant value used in the controller and is equal to the nominal frequency of the system (314 rad/s for 50 Hz frequency).

The reference capacitor voltage for inverter 1 can be represented in the dq synchronous frame based on (5.10) as follows (with $Z_1^{'} = R_1^{'} + j\omega_0^{'}L_1^{'}$):

$$\begin{cases} E_{ref1d} = V_{Lref} + R_1^{'}I_{1d} - \omega_0^{'}L_1^{'}I_{1q} \\ E_{1refq} = \omega_0^{'}L_1^{'}I_{1d} + R_1^{'}I_{1q} \end{cases} \tag{5.11}$$

where $R_1^{'}$ and $L_1^{'}$ are the values used in the controller which have values equal to the resistance and inductance of the load-side inductor.

Substituting the equation of the autonomous control (5.11) into the load voltage equations ((5.8) and (5.9)), the following equations are obtained for inverter 1:

$$\begin{cases} V_{Ld} = A(s)V_{Lref} + A(s)R_1^{'}I_{1d} - A(s)\omega_0^{'}L_1^{'}I_{1q} - Z_{th}I_{1d} - R_1I_{1d} + \omega_0L_1I_q \\ V_{Lq} = A(s)\omega_0^{'}L_1^{'}I_{1d} + A(s)R_1^{'}I_{1q} - Z_{th}I_{1q} - R_1I_{1q} - \omega_0L_1I_d. \end{cases} \tag{5.12}$$

Equation (5.12) can be represented in the equivalent circuit diagram shown in Fig. 5-2c.

In equation (5.12), and as shown in Fig. 5-3, Z_{th} is very small at the fundamental frequency and can be ignored, and $A(s)$ is equal to 1. Consequently, in ther ideal case, the last four terms will cancel each other out in the equation of V_{Ld} in (5.12). On the other hand, V_{lq} will be zero. The dq components in the steady state will therefore be as follows:

$$\begin{cases} V_{Ld} = V_{Lref} \\ V_{Lq} = 0. \end{cases} \tag{5.13}$$

Equation (5.13) shows that the load voltage will be equal to the reference value and has a zero phase (i.e. it is synchronized with the grid voltage). In case of variation in the parameters of the output inductor, the dq components of the load voltage may include some error. However, this error is very small and does not cause any problems. Moreover, it can be compensated by adjusting the controller's parameters in (5.11).

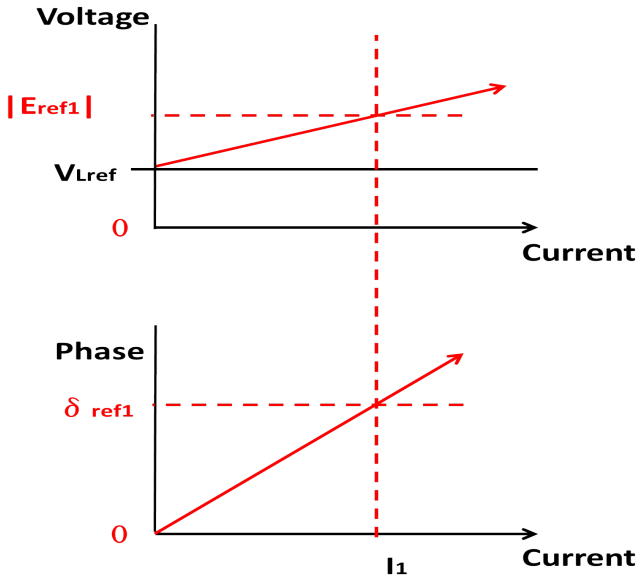


Figure 5-4: The relation between the output current and reference voltage and phase in the proposed autonomous control.

Fig. 5-4 represents the change in the reference capacitor voltage and phase as functions of the output current based on the autonomous control equation (5.10). The change in the current will create a change in the reference voltage and phase, such that the load voltage will remain fixed at V_{Lref} with zero phase angle.

Fig. 5-5 shows the block diagram of n parallel UPS modules connected in parallel to a load. The detailed construction of UPS 1 is shown. Each UPS uses a PLL (phase locked loop) to

generate the reference phase of the grid (θ_{ref1}). The reference phase is used to transform the output current of UPS 1 to the synchronous frame. It is also used to transform the capacitor voltage and capacitor current to the synchronous frame. The dq-components of the output current (I_{1dq}) are used to generate the reference capacitor voltage (E_{ref1dq}), as described in (5.11). The output of the autonomous control block (E_{ref1dq}) is used for the multi-loop control to generate the PWM gate signals as discussed in Section III.

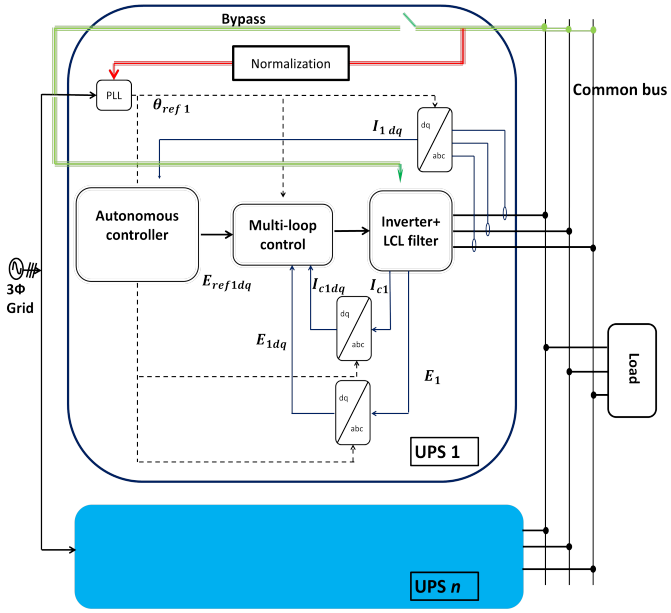


Figure 5-5: Block diagram of n parallel on-line UPS modules with detailed construction of UPS 1 with proposed autonomous control.

In Fig. 5-5 there are two inputs to the PLL: the main utility voltage and the load voltage. Both the utility voltage and the load voltage are normalized to unity. This is done because the amplitude of the input voltage to the PLL appears as a gain term in the forward path [76]. In the normal condition, the reference phase angle (θ_{ref1}) is generated from the utility voltage [74, 75]. However, in case of grid failure, the common bus voltage is used instead. Notice that the autonomous control equation (5.11) synchronizes the load voltage with the utility. In other words, the phase of V_L is equal to the reference phase. Since all parallel UPS units have their clocks synchronized, when the grid fails, the common load bus voltage is used by all parallel

units and the system keeps operating without interruption. When the grid voltage is restored, the UPS units re-synchronize their clocks with the utility [5]. More details about the structure of the PLL and re-synchronization with the grid will be explained in a future publication.

The reason for naming the control method as current-dependent capacitor voltage control can now be explained based on Fig. 5-2c. The reference capacitor voltage is controlled based on the output current of the inverter. The current-dependent voltage source in Fig. 5-2c ($A(s)Z_1^{'}I_1$) compensates the voltage drop on the output-side inductor so that the load voltage exactly equals the reference value.

5.2.3 Effect of line impedance

Depending on the distance between the UPS modules and the load, the impedance of the connecting cables can be resistive or inductive [28, 60]. Since the autonomous control equation is based on controlling the capacitor voltage of the filter, while taking into account the voltage drop on the load-side inductor, the impedance of the line can be lumped together with the impedance of the inductor. The impedance of the load-side inductor (Z_1) and the impedance of the connecting cables (Z_{line}) can be lumped together. The total impedance is the summation of Z_1 and Z_{line}, which is Z_{total}. The autonomous control equation (5.10) is now modified to take into account the impedance of the feeder by modifying the value of $Z_1^{'}$ to be equal to Z_{total}.

Fig. 5-6 demonstrates the effect of the line impedance on the reference capacitor voltage of one inverter. To give a clear picture of the influence of the line impedance, two cases of the impedance of the feeder (Z_{line}) will be analysed: resistive and inductive line. In Fig. 5-6a-c, the impedance of the line is assumed to be pure inductive (R_{line}=0). Fig. 5-6a shows the relation between the output current, the inductance of the line (L_{line}), and the rms value of the reference capacitor voltage ($|E_{ref1}|$). On the other hand, Fig. 5-6b shows the relation between the output current, the inductance of the line, and the phase of the reference capacitor voltage (δ_{ref1}).

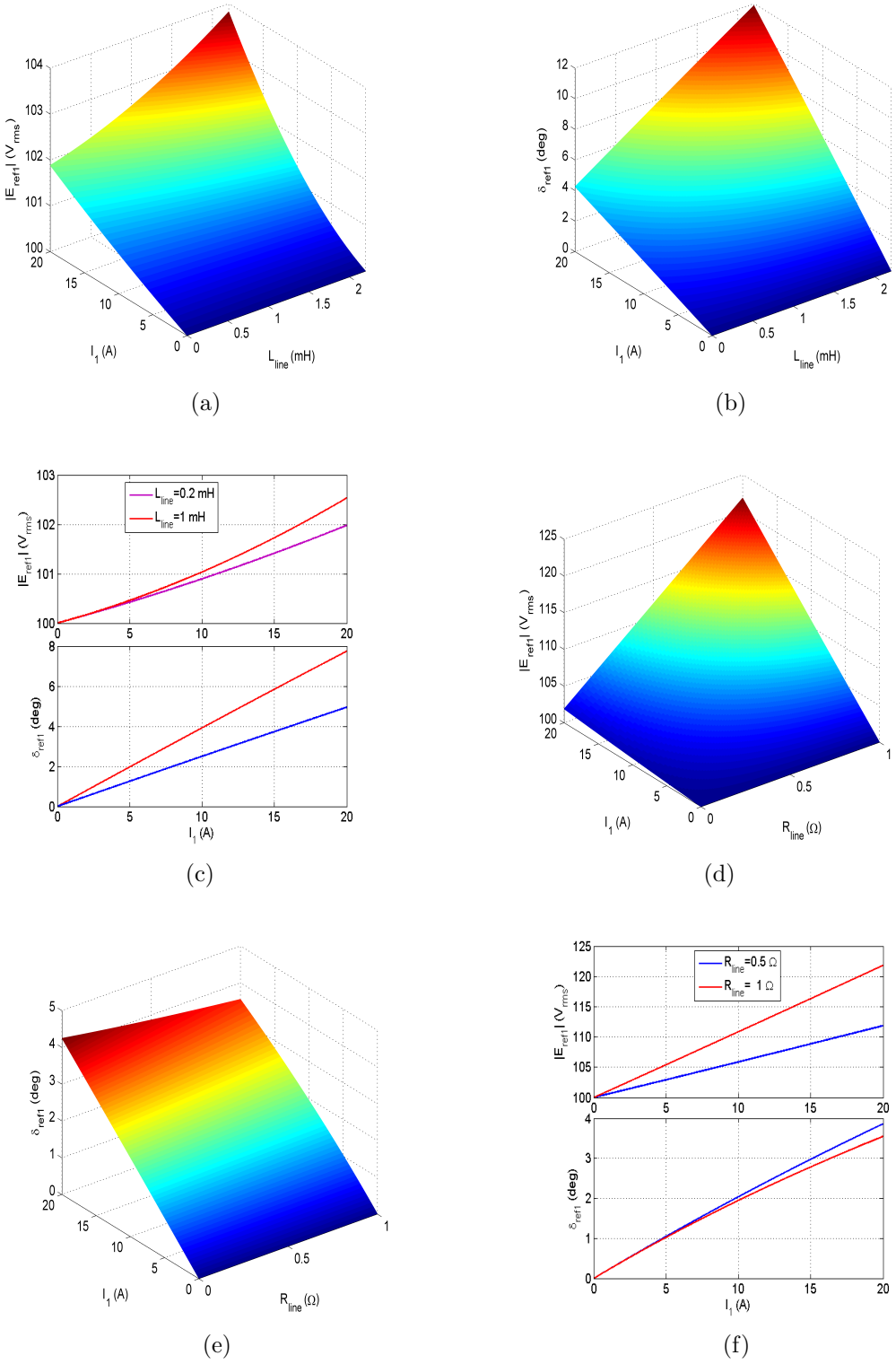


Figure 5-6: Effect of line impedance on the reference capacitor voltage and phase angle, (a-c) the line is pure inductive, (d-f) the line is pure resistive (a) relation between I_1, L_{line} and rms reference voltage , (b) relation between I_1, L_{line} and reference phase angle, (c) reference voltage and phase for two values of line inductance, (d) relation between I_1, R_{line} and rms reference voltage, (e) relation between I_1, R_{line} and reference phase angle, (f) reference voltage and phase for two values of line resistance.

Notice that increasing the inductance of the feeder results in increase in both the magnitude and phase angle of the reference capacitor voltage. Fig. 5-6c shows the relation between the current and the rms voltage and phase of the reference capacitor voltage for two values of line inductance: 0.2 mH and 1 mH. Notice that for the same value of current (the same load), larger line inductance results in larger reference capacitor voltage and phase. Notice also that the inductance of the line has a more pronounced effect on the phase angle than on the voltage.

In Fig. 5-6d-f, the feeder line is assumed to be pure resistive (L_{line}=0). Fig. 5-6d shows the relation between the output current, the resistance of the line (R_{line}), and the rms value of the reference capacitor voltage ($|E_{ref1}|$). On the other hand, Fig. 5-6e shows the output current, the resistance of the line, and the phase of the reference capacitor voltage (δ_{ref1}). Notice that increasing the resistance of the feeder results in increase in the magnitude of the reference capacitor voltage, while it has a negligible effect on the reference phase. Fig. 5-6f shows the relation between the current and the reference rms voltage and phase for two values of line resistance: 0.5 Ω and 1 Ω. Notice that for the same value of current (the same load), larger line resistance results in larger reference capacitor voltage, and a small reduction in the reference phase. Notice also that the resistance of the line does not have a significant effect on the reference phase angle.

In the next section small signal stability analysis of two parallel inverters will be investigated, and the effect of gain parameters on the stability of the system will be analysed.

5.3 stability analysis

The time average model of the system of two parallel inverters in Fig. 5-7 in synchronous dq reference frame is:

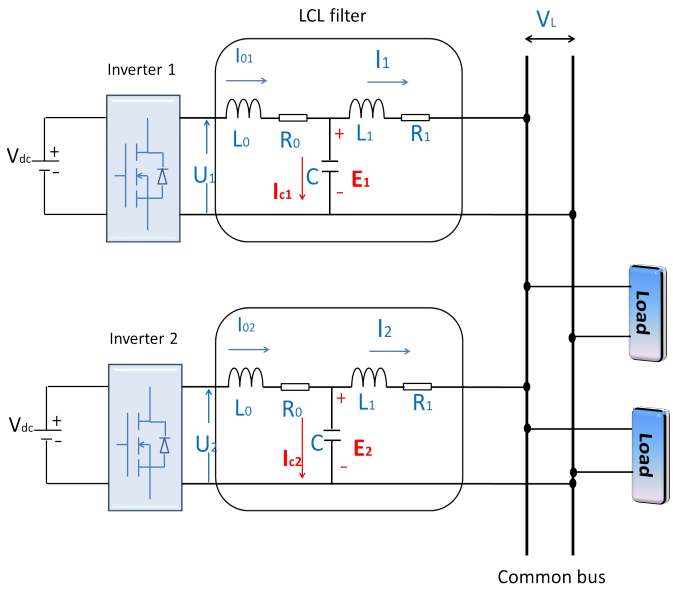


Figure 5-7: Two inverters with LCL filters connected in parallel.

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} I_{0id} \\ I_{0iq} \end{bmatrix} = \dfrac{1}{L_0}\begin{bmatrix} U_{id} - E_{id} \\ U_{iq} - E_{iq} \end{bmatrix} + \begin{bmatrix} -R_0/L_0 & \omega \\ -\omega & -R_0/L_0 \end{bmatrix}\begin{bmatrix} I_{0id} \\ I_{0iq} \end{bmatrix} \\ \dfrac{d}{dt}\begin{bmatrix} E_{id} \\ E_{iq} \end{bmatrix} = \dfrac{1}{C}\begin{bmatrix} I_{0id} - I_{id} \\ I_{0iq} - I_{iq} \end{bmatrix} + \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}\begin{bmatrix} E_{id} \\ E_{iq} \end{bmatrix} \\ \dfrac{d}{dt}\begin{bmatrix} I_{id} \\ I_{iq} \end{bmatrix} = \dfrac{1}{L_1}\begin{bmatrix} E_{id} - V_{Ld} \\ E_{iq} - V_{Lq} \end{bmatrix} + \begin{bmatrix} -R_1/L_1 & \omega \\ -\omega & -R_1/L_1 \end{bmatrix}\begin{bmatrix} I_{id} \\ I_{iq} \end{bmatrix} \end{cases} \tag{5.14}$$

where U_{idq} is the dq-axis components of the PWM outputs of the inverters, $i = 1, 2$ denotes the index of the inverter. The two inverters have the same LCL filter parameters. Other current and voltage variables are as shown in Fig. 5-1a. The PWM output voltage of the inverter, U_{idq}, is represented as:

$$U_{idq} = k_{pwm}\left[k_c k_p e_{idq} + k_c k_i \int e_{idq} - k_c I_c\right] \tag{5.15}$$

where e_{idq} is the voltage error signal ($e_{1dq} = E_{ref1dq} - E_{1dq}$, $e_{2dq} = E_{ref2dq} - E_{2dq}$). E_{irefdq} is as shown in (5.11).

A complete state space model of two parallel inverters operating under the proposed scheme around the equilibrium point can now be derived based on the time average model . Using (5.11), (5.14), and (5.15), and applying small signal perturbations, the state space model in matrix form can be described as:

$$\Delta\dot{X} = A\Delta X + \frac{1}{L_0}\Delta U \tag{5.16}$$

where ΔX is the state vector, $\Delta X = [\Delta i_{01d}\ \Delta i_{01q}\ \Delta E_{1d}\ \Delta E_{1q}\ \Delta i_{1d}\ \Delta i_{1q}\ \int \Delta e_{1d}\ \Delta e_{1q}$ $\Delta i_{02d}\ \Delta i_{02q}\ \Delta E_{2d}\ \Delta E_{2q}\ \Delta i_{2d}\ \Delta i_{2q}\ \int \Delta e_{2d}\ \Delta e_{2q}\ ]^T$, ΔU is the system input, $\Delta U = [\Delta U_{1d}\ \Delta U_{1q}$ $\Delta U_{2d}\ \Delta U_{2q};]^T$, and A is the state matrix.

The system input, ΔU, can be represented in terms of the state variables. Based on (5.11), (5.14), and (5.15), the system input is represented as:

$$\Delta U = B\Delta X. \tag{5.17}$$

Matrices A and B are shown in (5.18) and (5.19).

$$A = \begin{bmatrix} A_{ii} & A_{ij} \\ A_{ij} & A_{ii} \end{bmatrix}, A_{ii} = \begin{bmatrix} \frac{-R_0}{L_0} & \omega & \frac{-1}{L_0} & 0 & 0 & 0 & 0 & 0 \\ -\omega & \frac{-R_0}{L_0} & 0 & \frac{-1}{L_0} & 0 & 0 & 0 & 0 \\ \frac{1}{C} & 0 & 0 & \omega & -\frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & -\omega & 0 & 0 & -\frac{1}{C} & 0 & 0 \\ 0 & 0 & \frac{1}{L_1} & 0 & -\frac{R_1-R_L}{L_1} & \omega & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_1} & -\omega & -\frac{R_1-R_L}{L_1} & 0 & 0 \\ 0 & 0 & -1 & 0 & R_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & \omega L_1 & 0 & 0 & 0 \end{bmatrix},$$

$$A_{ij} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{-R_L}{L_1} & -\frac{-Z_L}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{-Z_L}{L_1} & -\frac{-R_L}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{5.18}$$

$$B = \begin{bmatrix} B_1 & B_2 & 0 & 0 \\ 0 & 0 & B_1 & B_2 \end{bmatrix}^T, \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} -k_c & 0 & -k_c k_p & 0 & k_c(1+R_1 k_p) & 0 & k_c k_i & 0 \\ 0 & -k_c & 0 & -k_c k_p & k_c k_p \omega L_1 & k_c & 0 & k_c k_I \end{bmatrix}. \tag{5.19}$$

The closed-loop system can now be represented as:

$$\Delta \dot{X} = \left(A + \frac{1}{L_0} B \right) \Delta X. \tag{5.20}$$

The stability of the system can be investigated by calculating the eigenvalues of (5.20). Fig. 5-8a shows the poles of the system. All poles are in the left hand plane, which proves that the system is stable. To study the effect of the minor loop gain (k_c) and the voltage loop gain (k_p),

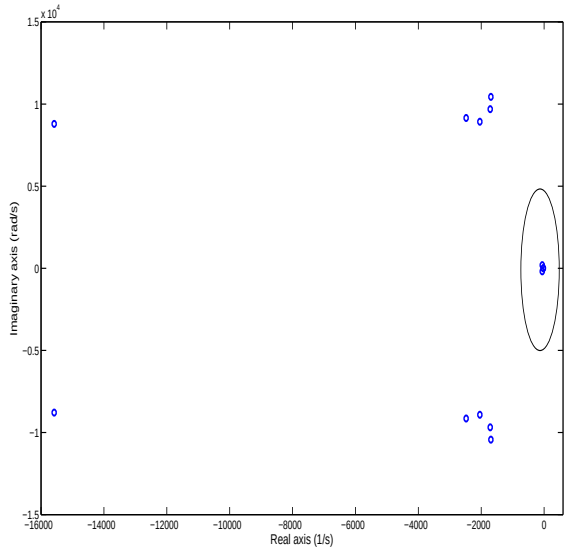
the dominant poles will be studied since they have the largest influence on the system (marked with a circle in Fig. 5-8a). As shown in Fig. 5-8b, increasing k_c moves the poles further to the left which makes the system more stable. On the other hand, low-frequency poles move towards the origin when k_p is increased, which means the stability margin of the system will be decreased and the system becomes slower.

5.4 Autonomous Control Simulation Results

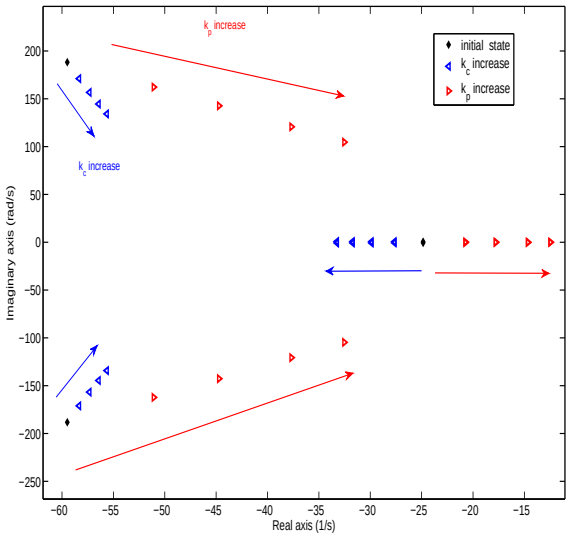
5.4.1 Case 1: Two UPS modules connected to a resistive load

Two UPS units are connected in parallel to a 2-kW load under the proposed autonomous control scheme. The internal block diagram of each unit is as shown in Fig. 5-5. The parameters of the LCL filters are shown in Table 4.1. Fig. 5-9a shows the output currents and their phase. Notice how the currents quickly coalesce to the equilibrium point with equal currents. Since the load is resistive, the phase of the currents in the steady state is equal to the phase of V_L, which is equal to the reference phase of the grid. At t=0.4 s, the load is increased to 4 kW. The currents increase at the same rate and converge to a new equilibrium state at which they maintain proper distribution.

The increase in the output currents of the inverter is reflected as an increase in the reference capacitor voltages of the two inverters. According to (5.11), the d-axis component of the reference capacitor voltage of an inverter (E_{ref1d}) is proportional to the d-component of its output current and has a slope equal to R_1. In case of resistive load, I_{1q}=0. On the other hand, the q-component of the reference capacitor voltage (E_{ref1q}) is also proportional to the d-component of the output current, but has a slope of ωL_1. Generally, R_1 is much smaller than ωL_1, which means that the change in E_{refq} is larger than E_{refd}. For example, for the inductors used in the simulation, $R_1 = 80\ m\Omega$ and $\omega L_1 = 0.38\ \Omega$. Fig. 5-9b shows the dq-components of the output



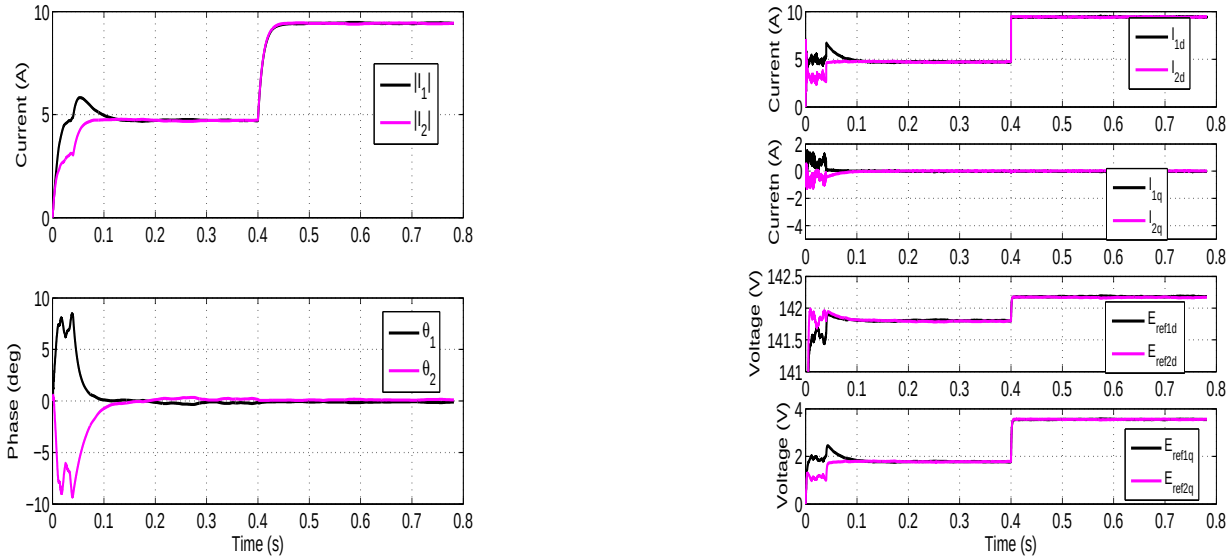
(a)



(b)

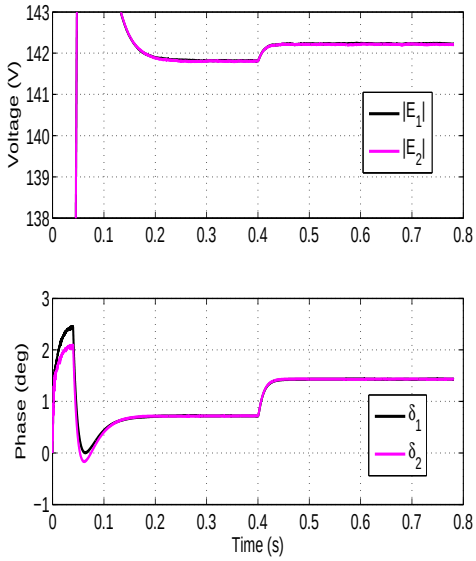
Figure 5-8: (a) Eigenvalues of a system of two parallel UPS units under the proposed autonomous control, (b) effect of increasing k_c and k_p on the poles marked with a circle in Fig. 5-8a.

currents of the two inverters as well as the dq-components of the reference capacitor voltages. Notice that the increase in the load causes increase in the d-components of the currents which is reflected as an increase in the dq-components of the reference capacitor voltages. The change in the d component of the reference voltage due to the load increase is about 0.3 V, while the

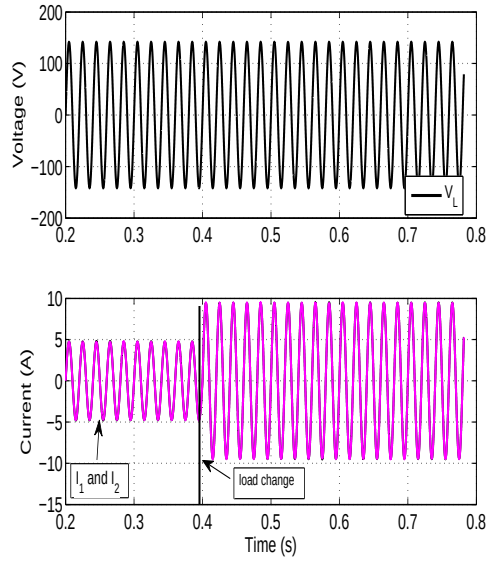


(a)

(b)



(c)



(d)

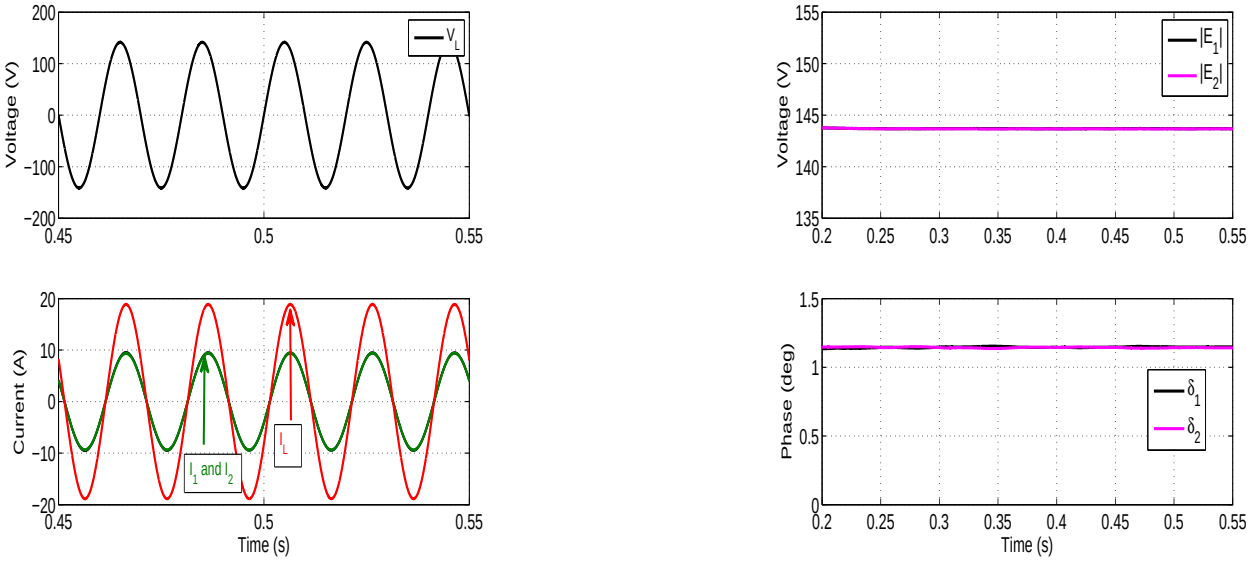
Figure 5-9: Case 1: resistive load 2 kW then increases to 4 kW (a) output currents and phase angles, (b) dq-components of output currents and dq-components of reference capacitor voltages, (c) capacitor voltages and their phase angles, (d) waveforms of load voltage and output currents.

change in the q component is about 1.7 V.

Fig. 5-9c shows the magnitude and phase of E_1 and E_2. The capacitor voltages of the two inverters follow the reference value. The waveform of the load voltage is shown in Fig. 5-9d and equals the reference value. The sudden change in the load does not cause distortion in the load voltage.

5.4.2 Case 2: Reactive load

A 4 kVA reactive load with 0.9 power factor is connected at the output. Fig. 5-10a shows the waveforms of the load voltage, output currents and load current. The load voltage follows the reference value and the output currents of the inverters are equal. The load current equals the summation of I_1 and I_2. Notice that the phase shift between the currents and the load voltage is 25.8°, which corresponds to a 0.9 power factor. Fig. 5-10b shows the magnitude and phase of the capacitor voltages (E_1 and E_2).



(a) (b)

Figure 5-10: Case 2: inductive load 4 kVA, 0.9 power factor (a) waveforms of load voltage, output currents and load current, (b) capacitor voltages and their phase angles.

5.4.3 Case 3: Inductive line impedance

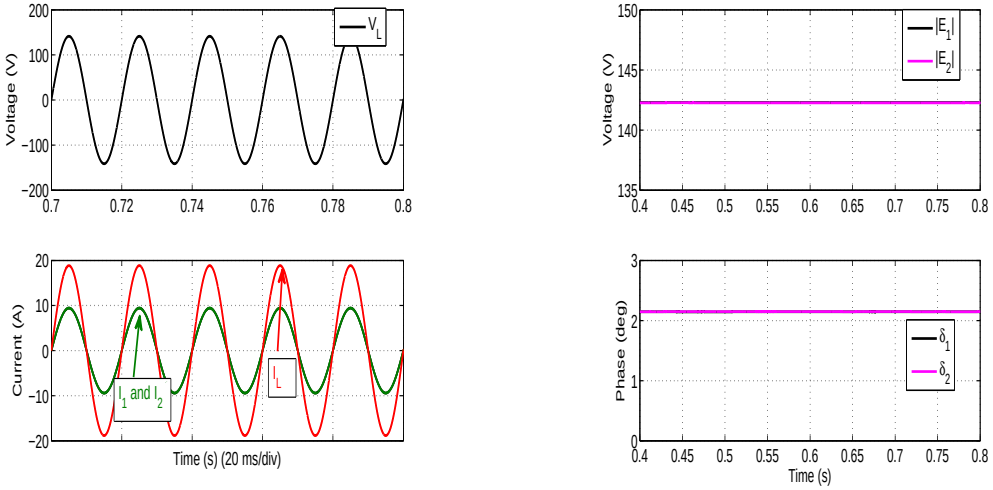
In this part we assume that an inductive line is connected at the output of the inverters to a 4 kW load. The inductance of the line is $L_{line} = 0.6\ mH$. Fig. 5-11 shows the corresponding waveforms for this case. Fig. 5-11a shows the waveforms of the load voltage, output currents and load current. The current distribution is not affected by the inductive impedance of the line as predicted by theory. Moreover, the load voltage equals the reference value. Fig. 5-11b shows the voltage and phase of the capacitors of the inverters. Comparing the voltage magnitude and phase with Fig. 5-9c in which the load is 4 kW in the steady state, we notice that the voltage magnitude is almost the same; however, the phase is different. In Case 1, the phase of the capacitor voltage in the steady state is 1.5° (Fig. 5-9c); in Case 3, on the other hand, the phase is 2.1° (Fig. 5-11b). This result agrees with the theoretical predictions made in Section IV; in Fig. 5-6c, it is shown that the inductance of the feeder has a more significant effect on the phase angle of the capacitor voltage than on the amplitude.

Finally, Fig. 5-11c shows the dq-components of the reference capacitor voltage.

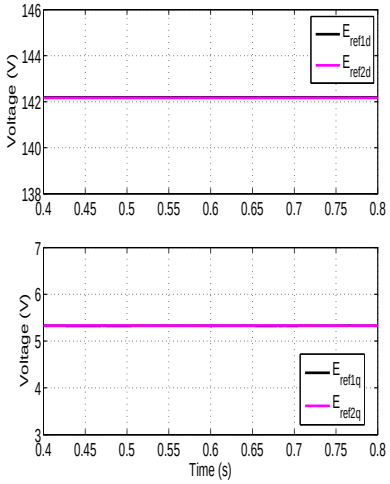
5.4.4 Case 4: Resistive line impedance

In this part we assume that a resistive line is connected at the output of the inverters. The resistance of the line is $R_{line} = 4\ \Omega$, and the load is 4 kW.

Fig. 5-12 shows the corresponding waveforms for this case. Fig. 5-12a shows the waveforms of the load voltage, output currents and load current. The current distribution is not affected by the resistance of the line as predicted by theory. Notice that the waveforms are similar to those in Fig. 5-11a. Fig. 5-12b shows the voltage and phase of the capacitors of the inverters. Comparing the voltage magnitude and phase with Fig. 5-9c in which the load is 4 kW in the steady state, we notice that the change in the magnitude of the capacitor voltage is more significant than the change in the phase. In Case 1, the magnitude of the capacitor voltage in the steady state is



(a) (b)



(c)

Figure 5-11: Case 3: inductive feeder line with inductance $L_{line} = 0.6\ mH$ (a) waveforms of load voltage, output currents and load current, (b) capacitor voltages and their phase angles, (c) dq-components of reference capacitor voltages.

142.2 V (Fig. 5-9c); in Case 3, on the other hand, the voltage is 180 V (Fig. 5-12b). This result agrees with the theoretical predictions made in Section IV; in Fig. 5-6f, the inductance of the feeder has a more significant effect on the magnitude of the capacitor voltage than on the phase angle.

Finally, Fig. 5-12c shows the dq-components of the reference capacitor voltage.

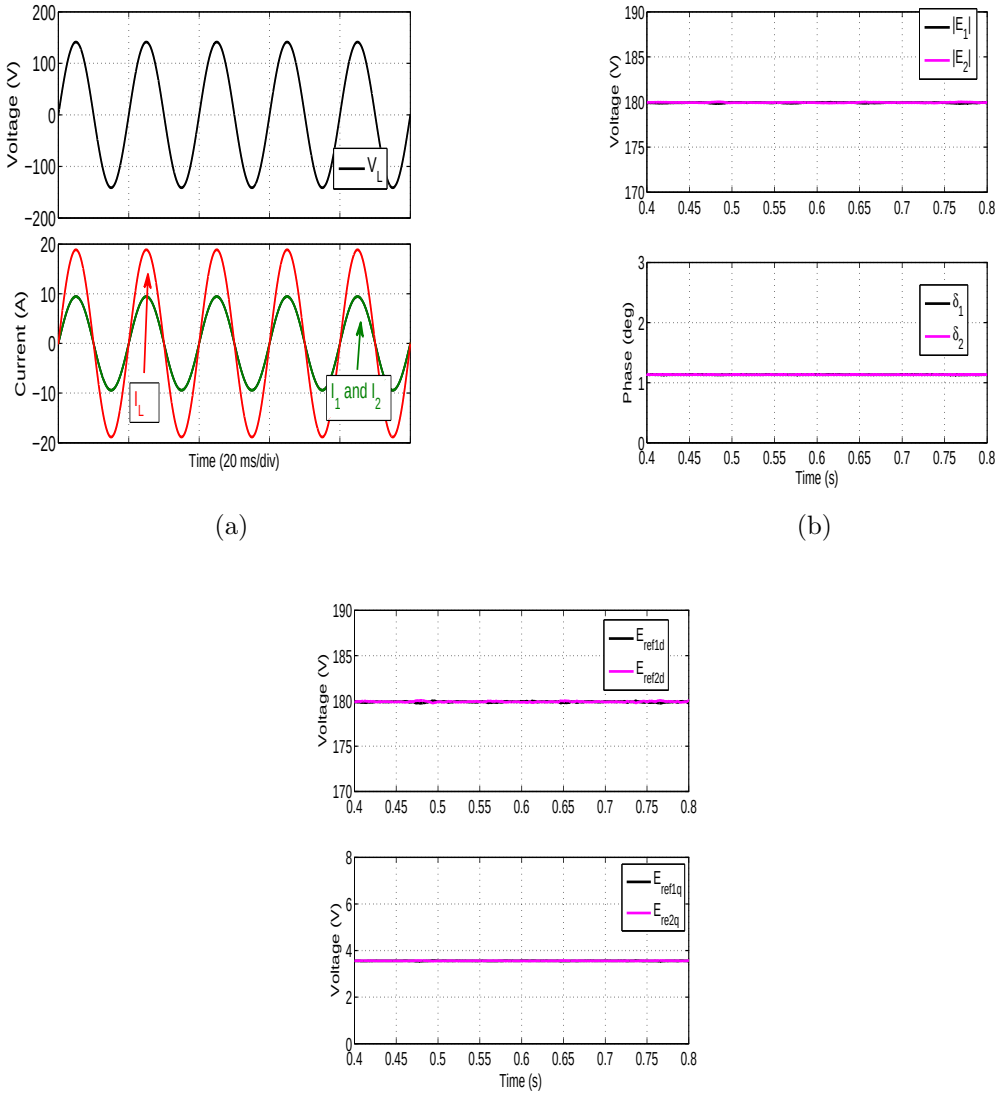


Figure 5-12: Case 4: resistive feeder line with resistance $R_{line} = 4\ \Omega$ (a) waveforms of load voltage, output currents and load current, (b) capacitor voltages and their phase angles, (c) dq-components of reference capacitor voltages.

5.4.5 Case 5: Connection/Disconnection of modules

Connecting additional parallel UPS units to the system while operating, as well as disconnecting units from the system, add tremendous advantages to the control scheme. The system might encounter big changes in the load between the day and night time. Hence, it is important that the control scheme has a feature to connect and disconnect modules without power interruption.

In this section, simulation results of connecting and disconnecting UPS modules while the system is operating will be presented. The waveforms of the output currents and the load voltage are shown to verify the effectiveness of the proposed autonomous control algorithm.

The procedure to connect a new unit to the system (hot swap operation), is summarized in the following steps:

1. The capacitor voltage of the new unit is controlled to be equal to the load voltage (amplitude and phase).

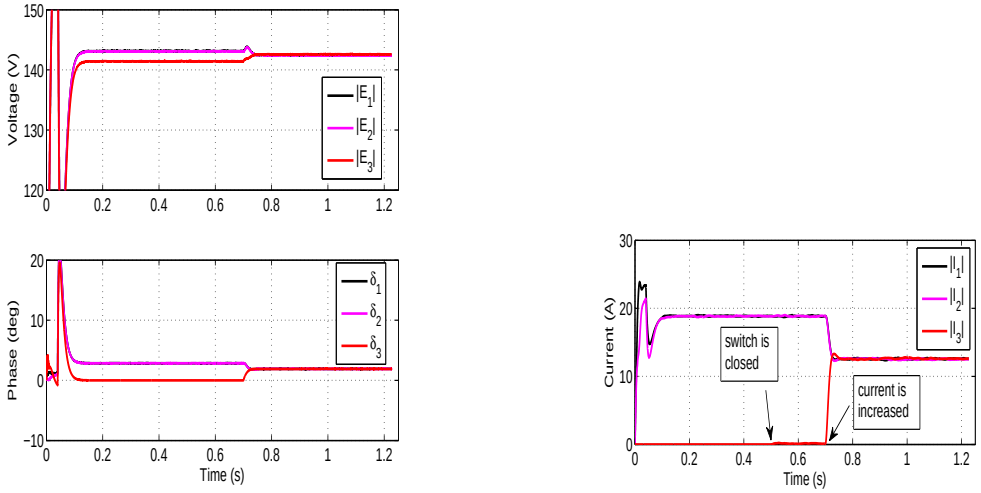
2. The connecting switch is closed. Since the capacitor voltage of the new unit and the load voltage are equal, the output current of this unit is zero.

3. Depending on the load condition, the capacitor voltage is controlled to be equal to a constant value. Once the capacitor voltage is changed, the output currents of the new unit will increase, and simultaneously, the output currents of the other units will decrease.

4. In the steady state, the controller of the new unit switches to autonomous control algorithm.

To investigate the hot-swap operation, a load of 8 kW is assumed, and two UPS modules are connected in parallel to supply power to the load. It is desired to add a new UPS unit to the system. Following the procedure described above, the simulation results are shown in Fig. 5-13.

Disconnecting units from the system can be done easily in the proposed control scheme. Any unit can be disconnected at any time without any interruption of the operation. To investigate this case, the same system of three parallel units described in this subsection is considered again, in which the load is 10 kW. UPS 3 is disconnected by opening the switch. Once the switch is opened, the output currents of the other units increase to compensate for the increase of equivalent power. Fig. 5-14 shows the simulation results for this case.



(a) (b)

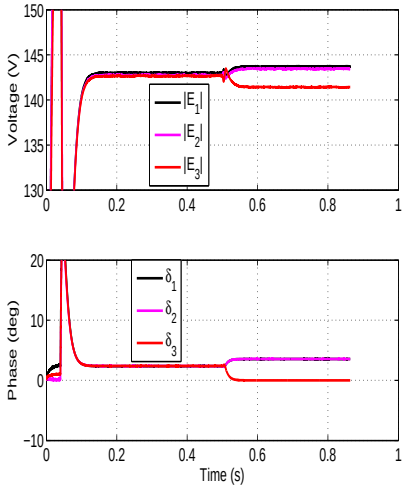
Figure 5-13: Case 5: connection of a new UPS unit into a system of two operating UPS modules (a) capacitor voltages and phase angles, (b) output currents.

In Fig. 5-14a the capacitors voltages of the three units are shown. At t= 0.5 s UPS 3 is disconnected. Notice that the output voltage of UPS 3 drops to the reference load voltage since the output current is zero in the steady state. The capacitors can then be discharged to zero by dissipating the stored energy into parallel resistors. The output currents are shown in Fig. 5-14b. The load voltage is shown in Fig. 5-14c. Notice that disconnecting the unit does not cause disturbance in the load voltage amplitude or phase.

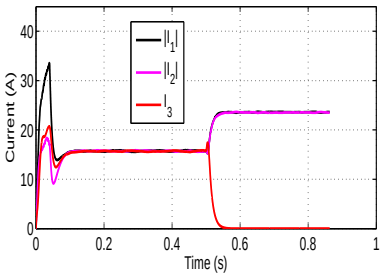
5.4.6 Procedure for UPS Maintenance

In this section the procedure for UPS maintenance is explained. In the case of malfunction of some UPS units, the load is connected to the utility voltage though a bypass switch. Fig. 5-15 shows two parallel UPS units connected to a load. The utility voltage is connected to a bus through an inductor. The voltage of this bus is V_s. The bypass switch, when closed, connected the utility to the load bus directly.

Procedure to disconnect the units:



(a)



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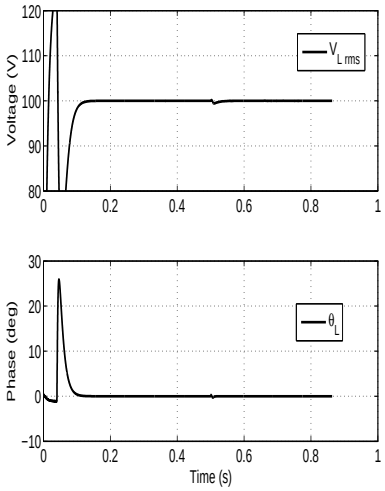


(c)

Figure 5-14: Case 5: Disconnecting a UPS module from a system of three modules, UPS 3 is disconnected at t=0.5 s (a) capacitor voltages and phase angles, (b) output currents, (c) load voltage and phase.

1. UPSs synchronize the supply voltage V_s with the load voltage V_L. In the normal operating condition, V_L is fixed at a specific value (for example 100 Vrms). However, during the procedure of maintenance, V_L is controlled to be equal to the grid voltage (V_s). In Fig. 5-16a, at t=0.3 s the load voltage is synchronized with V_s. The phase angles of the utility voltage and the load voltage are shown in Fig. 5-16b.

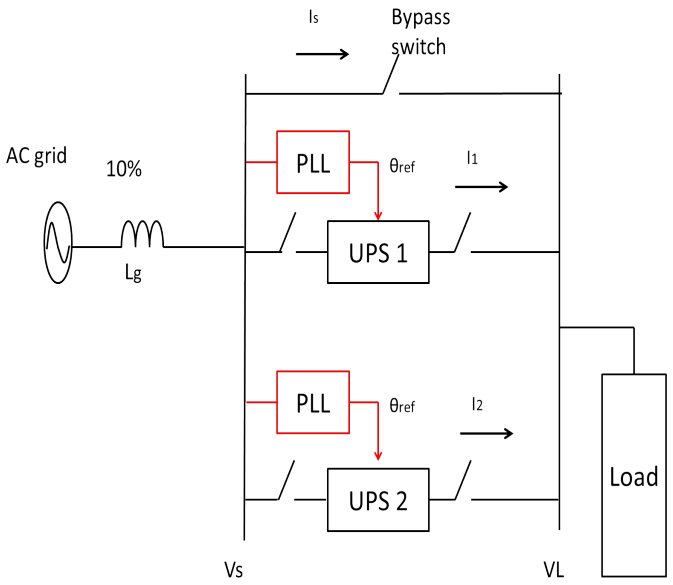


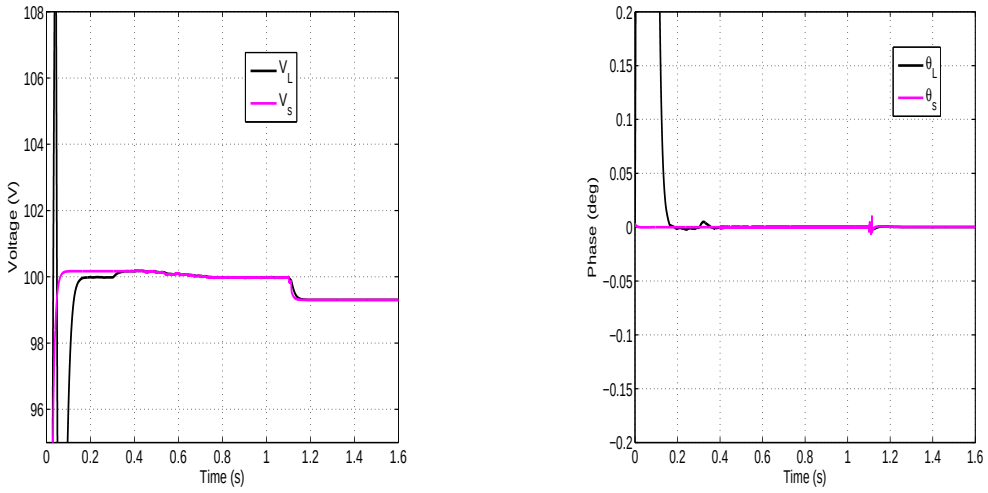
Figure 5-15: Block diagram of two parallel UPS units with bypass switch from the grid to the load.

2. The bypass switch is closed to connect the loads to the AC supply. When the bypass switch is closed at t=0.4 s, current will flow from the AC supply to the load (I_s). Hence, the output currents of the UPSs will decrease, as shown in Fig. 5-17. Notice that I_1 and I_2 remain equal after the bypass switch is closed. The amount of supply current (I_s) depends on the load condition, the voltage of the AC supply before the inductor or the transformer (V_g), and the inductor L_g.

3. UPSs are disconnected from the system. At t=1.1 s the UPSs are disconnected from the system. Now the AC supply provides the total current to the load.

4. The UPSs are disconnected now from the system and maintenance can be performed after discharging the capacitors of the filters.

After the maintenance operation is finished and the UPS modules are ready to be reconnected to the system, certain procedures must be followed to avoid interruption and disturbance in the load voltage. The following steps summarize the procedure to reconnect UPS units to the



(a) (b)

Figure 5-16: Procedure of disconnecting UPS modules for maintenance. Load voltage and phase are synchronized with the grid at t=0.3 s, the bypass switch is closed at t=0.4 s, and the UPSs are disconnected at t=1.1 s (a) load voltage and utility voltage, (b) load phase and utility phase.

system:

1. The UPSs are connected to the power source and energized. The batteries are charged.

2. UPSs synchronize their output voltages with the grid voltage. Using the PLL and voltage sensors, each UPS extracts the phase and voltage level of the grid voltage (V_s) and synchronizes its capacitor voltage with the grid.

3. The UPSs are connected to the load bus sequentially, by closing their switches. Here, the procedure to connect a UPS to the system is similar to that explained in the previous section. First, the capacitor voltage of the UPS is controlled to be equal to the load voltage (which is equal to V_s). Next, the switch is closed. At this stage the output current of the UPS is zero. Then, the UPS is controlled to supply a constant current by increasing the capacitor voltage and phase.

   The connection of the other UPSs follow the same procedure.

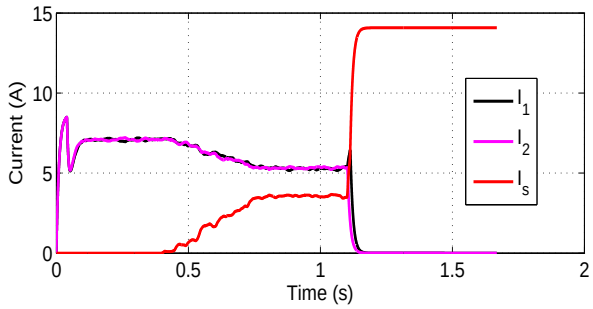


Figure 5-17: Procedure of disconnecting UPS modules for maintenance. The bypass switch is closed at t=0.4 s, and the UPSs are disconnected at t=1.1 s.

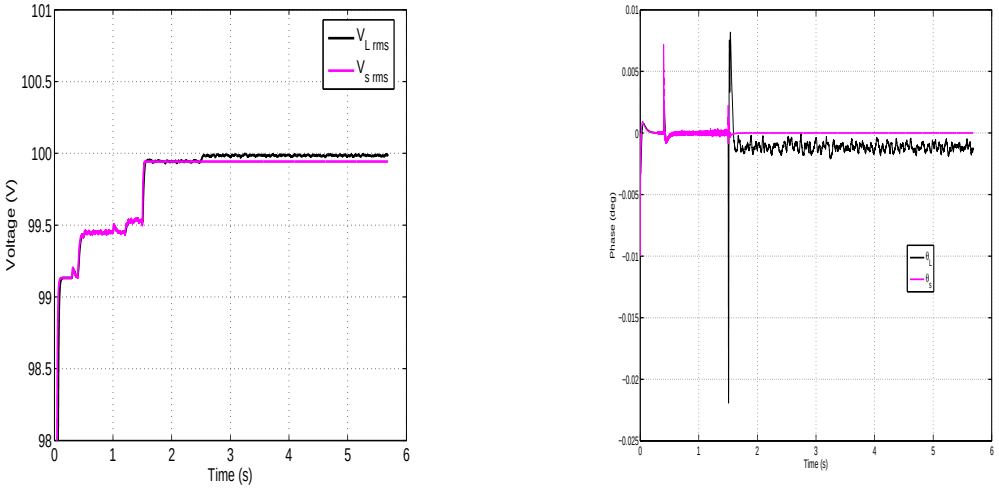
In Fig. 5-18a and Fig. 5-18b, the load voltage and grid voltage and phase angles are shown. Fig. 5-19 shows the output currents of the UPS units and the utility current. UPS 1 is connected at t=0.3 s. At t=0.4 s it starts supplying a constant output current. At t=1 s, the switch of UPS 2 is closed. At t=1.1 s it starts supplying a constant current.

4. At this stage, all UPSs are connected and are supplying a constant current. The UPSs then switch to autonomous mode.

   In Fig.5-19, the two parallel UPS units swithc to autonomous mode at t=1.5 s. At the same time, the bypass switch is opened.

5. The bypass switch is opened and the grid is disconnected from the system.

6. Finally, the load voltage is controlled at a fixed value (V_{Lref}), as shown in Fig. 5-18a, at t=2.5 s the load voltage is controlled as 100 Vrms.



(a) (b)

Figure 5-18: Procedure for connecting UPS modules. UPS 1 is connected at t=0.3 s and starts supplying constant current at t=0.4 s. At t= 1 s UPS 2 is connected (a) load voltage and utility voltage, (b) load phase and utlity phase.

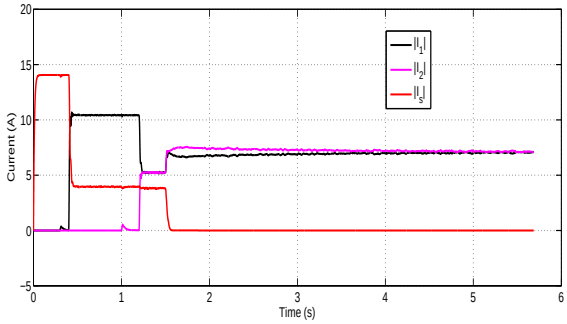


Figure 5-19: Procedure for connecting UPS modules. UPS 1 is connected at t=0.3 s and starts supplying constant current at t=0.4 s. At t= 1 s UPS 2 is connected. Output currents and utility current

5.4.7 Nonlinear Load

With the rapid growth of technology and advanced equipment, the complexity of the power systems is increasing. Many of the loads connected are nonlinear and generate harmonics. The IEEE 519-1992 standard imposes a limit on the total harmonic distortion (THD) of the output voltage of less than 5%. Hence, for a control scheme of parallel inverters to be reliable, nonlinear load conditions must be taken into account. Active load sharing control methods are superior to the droop method in handling the harmonics generated by nonlinear loads. One of the weak points of the droop method is its inability to distribute the harmonic currents equally between the parallel inverters.

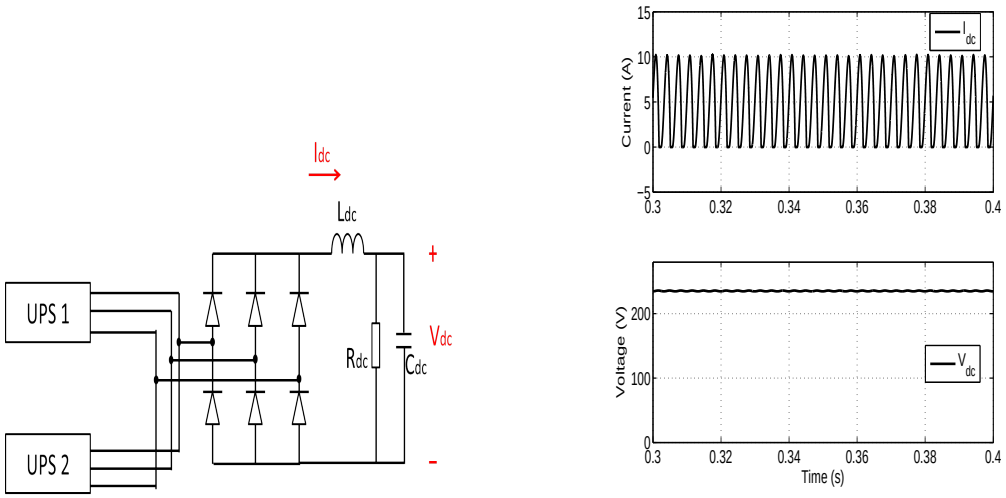
This section discusses nonlinear loads connected to a system of parallel inverters which are controlled using the proposed autonomous control scheme.

A three phase rectifier is connected at the output of two parallel UPS modules using the proposed autonomous control scheme. The resistance of the dc load is 50Ω. A dc capacitor of 4600μF is connected in parallel to the load to smooth the output voltage of the rectifier.

The circuit diagram of two UPS modules connected in parallel to a three phase rectifier is shown in Fig. 5-20a.

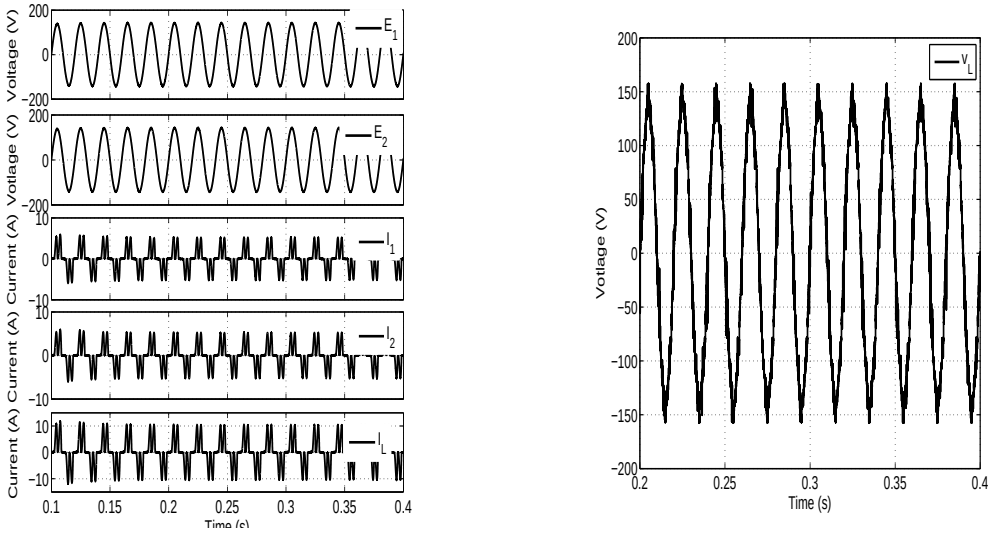
An inductor is added in series at the dc side of the rectifier (L_{dc}). This inductor transforms the output current from discontinuous mode to continuous mode. In the first part of the simulation, the inductor is removed from the output side. The results of the output dc voltage and current are shown in Fig. 5-20b. The dc current is in the discontinuous mode (the current decreases to zero for some period of time). The discontinuous current increases the harmonics in the input side of the rectifier and causes distortion in the load voltage. The dc voltage is also shown in Fig. 5-20b. The dc voltage is smooth due to the capacitor added in parallel to the load.

The waveforms of the UPS units are shown in Fig. 5-21. The control scheme maintains equal



(a) (b)

Figure 5-20: Autonomous control under nonlinear load (a) circuit diagram of two UPS units connected to rectifier load, (b) output dc voltage and dc current.



(a) (b)

Figure 5-21: waveforms under autonomous control under nonlinear load (a) from top to bottom: capacitor voltage of UPS 1, capacitor voltage of UPS 2, Output current of UPS 1, output current of UPS 2, load current, (b) load voltage.

current distribution and the harmonics are shared between the two inverters. The load voltage is shown in Fig. 5-21b. The THD of the load voltage is 4.66%, which complies with the IEEE 519-1992 standard of 5%.

5.5 Robustness Against Parameters Variation

In order to share the load power accurately between parallel inverters, all parallel units should have the same output impedance. This condition is derived based on equation (5.10), which is the proposed autonomous control equation. Since it is decided that all inverters must have the same reference capacitor voltage, a necessary condition to eliminate the circulating current, and since the reference load voltage is fixed and known for all units (V_{Lref}), then, for n parallel inverters the following equation is derived:

$$Z_1 I_1 = Z_2 I_2 = \cdots = Z_n I_n. \tag{5.21}$$

For parallel units with different power ratings, the output impedances should be inversely proportional to the power ratings of the inverters, as follows:

$$\frac{I_1}{I_2} = \frac{Z_2}{Z_1}. \tag{5.22}$$

Equation (5.22) shows that the output impedance of the inverter has a significant effect on the proportion of output currents. Moreover, the value of the impedance in the controller ($\bar{Z}_i'$ in (5.10)) should theoretically match the actual value of the impedance of the output inductor ($\bar{Z}_1$).

In practical systems, it is difficult to guarantee that parallel inverters have exactly the same output inductors. Moreover, these parameters may change while the system is operating. Hence, it is important to investigate the the robustness of the proposed control and to ensure the stability of the system in case of variation in the parameters of the system. Fig. 5-22 shows the output currents of two parallel inverters with 10% change in the inductance of inverter 2 (L_2). It is evident that the variation of the inductance of one inverter has a significant effect on the system. In particular, there is large error in the phase of the output currents of the

inverters.

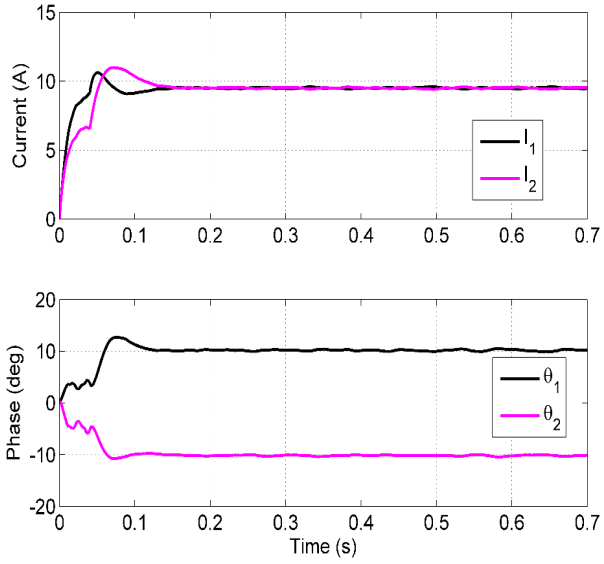


Figure 5-22: Output currents of two inverters under the proposed control with 10% change in the inductance of inverter 2.

The sensitivity of the proposed control scheme to the variation in the output impedance of the inverters can be overcome by adding a virtual impedance in series with the inverter. The proper design of the virtual impedance can solve the problem of output impedance imbalance and reduce the sensitivity of the output inductors, as discussed in Chapter 3.

The virtual impedance is achieved by dropping the reference voltage as a function of the output current of the inverter. In the case of the system discussed in this dissertation, the reference capacitor voltage is dropped:

$$E^*_{ref1} = E_{ref1} - Z_{v1}(s)I_1 \tag{5.23}$$

where Z_v is the virtual impedance of inverter 1.

The block diagram of inverter 1 with a resistive virtual impedance (R_{v1}) is shown in Fig. 5-23a. Notice that the output current of the inverter is multiplied by a constant value equal to the virtual resistance (R_{v1}) and subtracted from the reference voltage. The equivalent circuit of the

inverters is shown in Fig. 5-23b with R_{v1} and R_{v2} in series with the two inverters, respectively.

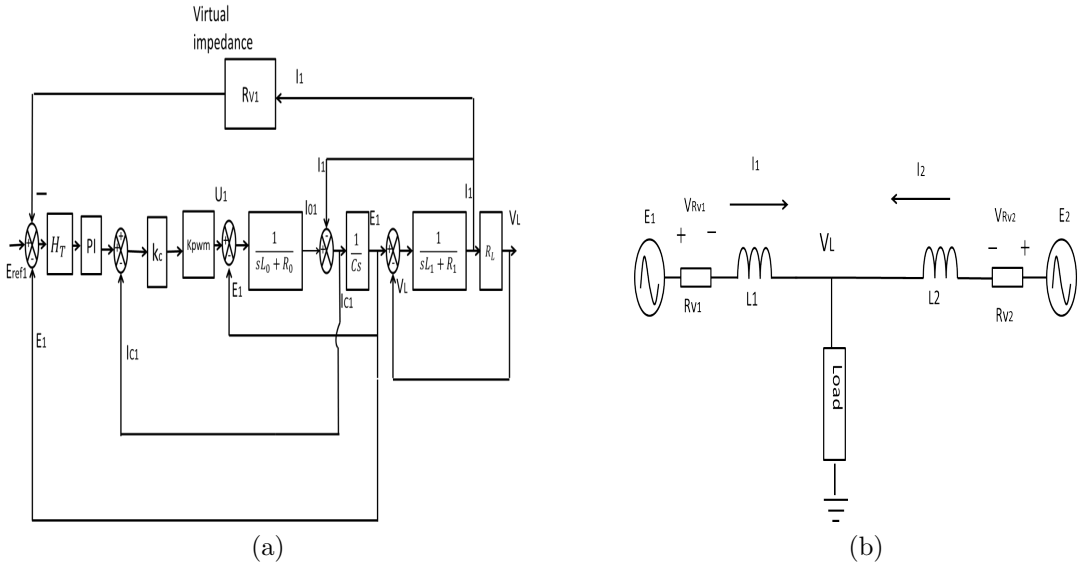


Figure 5-23: Virtual impedance implementation (a) block diagram of one inverter with a resistive virtual impedance, (b) equivalent circuit with virtual resistance.

The implementation of the virtual impedance concept into the controller is an easy task that can be realized by adding a few lines in the program of the controller. Yet, the benefits gained are numerous: enhanced performance, reduction in circulating current, better power quality, increased stability, and less sensitivity to the values of the physical components and controller parameters [66, 67, 64].

The current distribution of the two parallel inverters with a resistive virtual impedance will be investigated. Different values of virtual resistances are incorporated into the controller to show the effect on the system. The same system of two inverters with 10% change in L_2 is assumed. The output currents and load voltage are shown in Fig. 5-24a and Fig. 5-24b, respectively.

In Fig. 5-24a, the virtual resistance is increased from 0.6Ω to 2Ω to 4Ω. The effect of increasing the virtual resistance is reduction in the difference in the phase shift between the output currents of the inverters. This result can be explained when the impedances of the output inductors are compared with the virtual resistance. For an inductor L_1 =1.2 mH, the

equivalent impedance at $50Hz$ is 0.3768Ω. If R_v is zero, a 10% change in the impedance of one inverter has a significant effect on the distribution of the output currents. However, when the virtual resistance is increased to 4Ω, the virtual resistance becomes dominant since the impedance of the inductor is only about 9.4% of the virtual resistance, and therefore a 10% variation does not have as much effect.

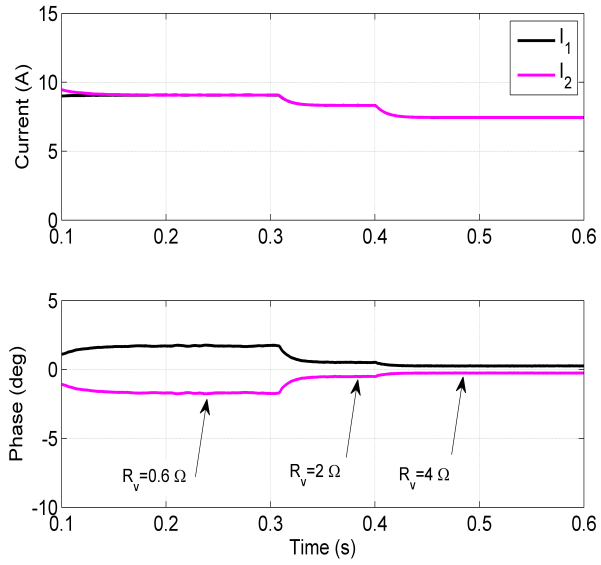
The effect of increasing the virtual resistance on the load voltage can be observed in Fig. 5-24b, where the load voltage decreases with the increase of the virtual resistance. This is an intuitive and expected result that adding a virtual resistance causes a voltage drop (V_{Rv1} in Fig. 5-23b), and adding an inductive virtual impedance causes phase delay [66]. Certain measures can be taken to solve this problem.

In this research, we deal with the problem of voltage drop on the virtual impedance by an adaptive controller that changes the reference load voltage to compensate for the voltage drop V_{Rv1}. Re-writing equation (5.10):

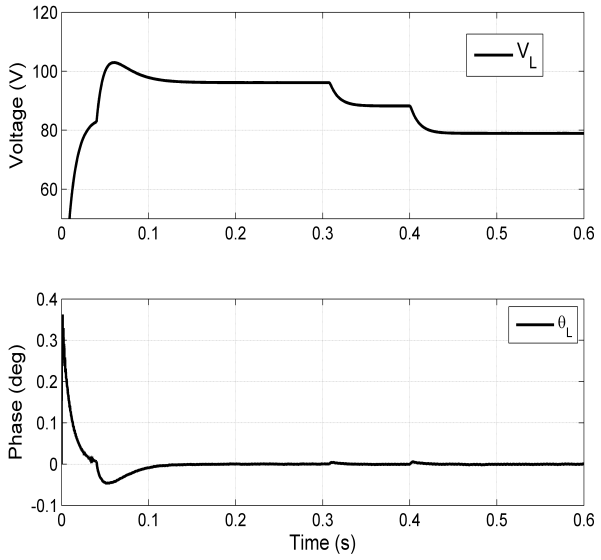
$$\bar{E}_{ref1} = \bar{V}_{Lrefnew} + \bar{Z}_1' \bar{I}_1 \tag{5.24}$$

where $\bar{V}_{Lrefnew}$ is the new reference voltage generated at the controller by adding the voltage drop on the virtual resistance V_{Rv1} to the reference load voltage V_{Lref}. The voltage drop on the virtual resistance is not an instantaneous value; a sample-and-hold block is used to keep it at a constant value and changes according to the output current variation.

After implementing the virtual impedance with voltage drop compensation, the results of output currents and load voltage are shown in Fig. 5-25. A virtual impedance of 5Ω is activated at t=0.2 s, and the phase error is eliminated. The load is increased at t=0.4 s and the proper current distribution is maintained. The load voltage is shown in Fig. 5-25b. The load voltage follows the reference and the voltage drop on the virtual resistance is compensated.



(a)

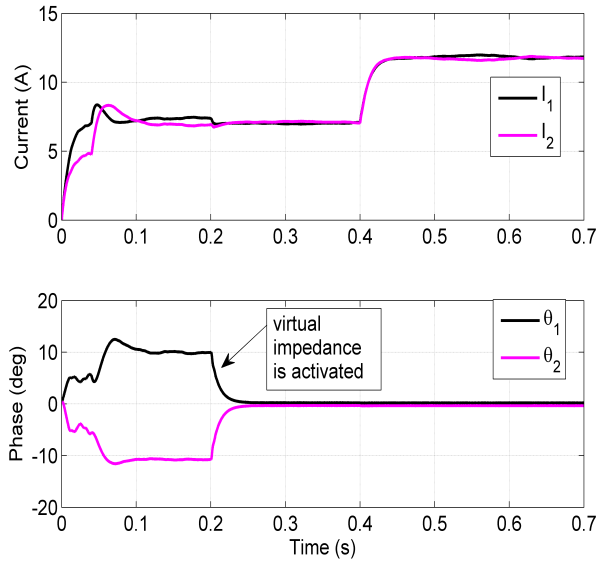


(b)

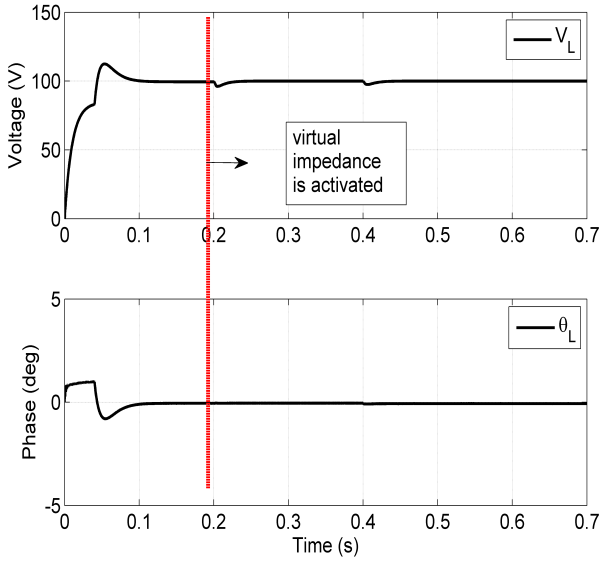
Figure 5-24: Output currents and load voltage for two inverters with 10% variation in the inductance of L_2 for different values of virtual resistance (a) output currents, (b) load voltage.

5.6 Comparison with Droop Control

This section provides a case study of parallel inverters connected to a load and controlled using the droop control scheme and the proposed control scheme (CCVC). The differences in the



(a)



(b)

Figure 5-25: Output currents and load voltage for two inverters with 10% variation in the inductance of L_2 with 5Ω virtual resistance and voltage drop compensation (a) output currents, (b) load voltage.

dynamic performance, load voltage, and circulating current is investigated.

We assume two parallel inverters and that the power rating of inverter 2 is twice that of inverter 1. The output inductors are chosen so that their impedances are inversely proportional

to the power ratings of the inverters ($X_1 = 2X_2$), where $X_1 = 0.1 + j\omega L_1$, $X_2 = 0.08 + j\omega L_2$, L_1 =2.4 mH, and L_2 =1.2 mH. The block diagram of the system is shown in Fig. 5-26.

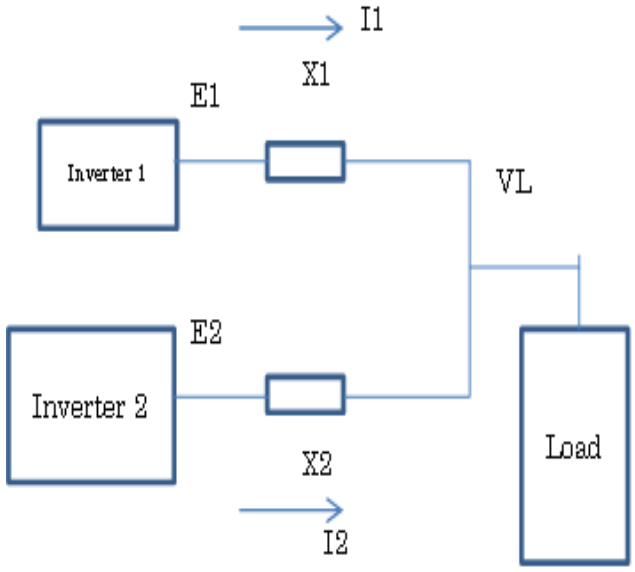


Figure 5-26: Block diagram of two inverters with inverter 2 having twice the capacity of inverter 1.

As discussed in Chapter 2, the two equations that govern the traditional droop control are as follows:

$$\omega = \omega_0 - k_p P \tag{5.25}$$

$$V = V_0 - k_q Q \tag{5.26}$$

where ω_0 is the reference radian frequency, V_0 is the reference voltage, k_p and k_q are the active power and reactive power slopes, respectively, and P and Q are the active and reactive power.

The slopes k_p and k_q for the two inverters are chosen taking into consideration the power ratios of the inverters, as follows: $k_{p2} = 4 \times 10^{-4}$rad/s.W, $k_{p1} = 2k_{p2}$, $k_{q2} = 0.007$V/VAr,

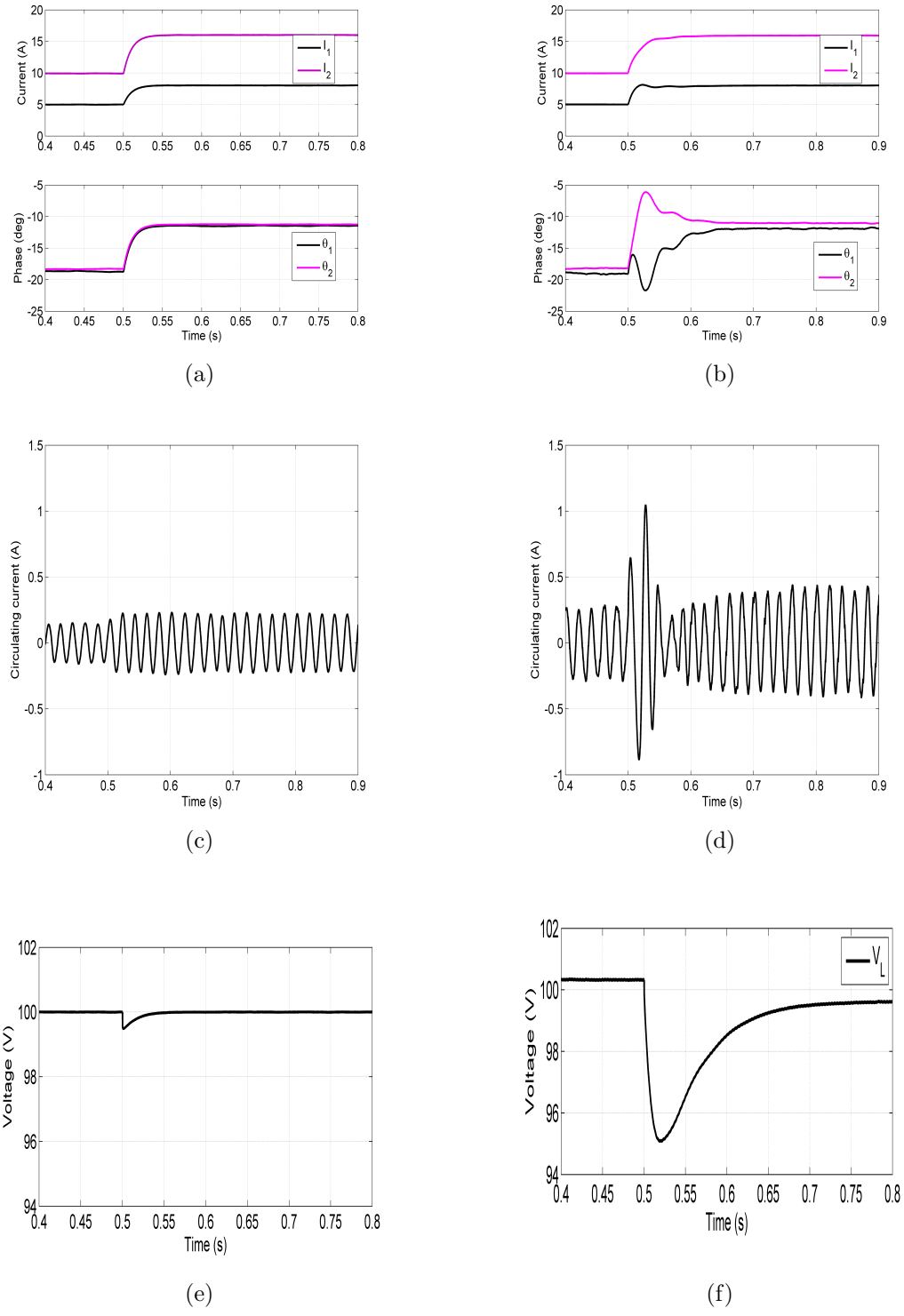


Figure 5-27: Comparison between the Droop control and CCVC (a) output currents for CCVC, (b) output currents for Droop, (c) circulating current for CCVC, (d) circulating current for Droop, (e) load voltage for CCVC (f) load voltage for Droop.

$k_{q1} = 2k_{q2}$.

The comparison results are shown in Fig. 5-27. The output currents and phase angles are shown in Fig. 5-27a and Fig. 5-27b. The proposed control exhibits a better dynamic response in the transient state. The circulating currents from Inverter 1 to Inverter 2 are shown in Fig. 5-27c and Fig. 5-27d. The proposed control results in 50% reduction in the circulating current. Finally, the load voltage is shown in Fig. 5-27e and Fig. 5-27f. There are two merits in using the CCVC compared to the Droop: First, the load undershoot in case of load change in the proposed control is negligible, while in the case of Droop is significant. Second, the level of load voltage remain constant in the proposed control, contrary to the Droop in which the load voltage changes according to the Droop equation (the same observation is correct for the frequency of the system).

Fig. 5-27a and Fig. 5-27b show significant difference between the two control schemes in the transient response. Especially the phase response of the output currents for the Droop control has relatively larger settling time. The transient response can be improved by increasing the gain of the voltage droop equation (k_q in (5.26). However, increasing the accuracy of the droop control, as discussed in many publications in the literature, comes at the expense of increasing the deviation of the load voltage from the reference value [4, 5, 14, 72]. In Fig. 5-28 the gain of the voltage droop equation is increase (from 0.007 to 0.02 V/VAr). The transient response is improved, but since k_q is increased by more than one order of magnitude, the voltage deviation will increase.

5.7 Unbalanced Load Condition

In this paper we use synchronous reference frame PLL (SRF-PLL), which is widely used in power electronics and power systems applications. In this technique, the loop filter is a PI controller and the open loop transfer function has two poles at the origin (hence it is called a type-II

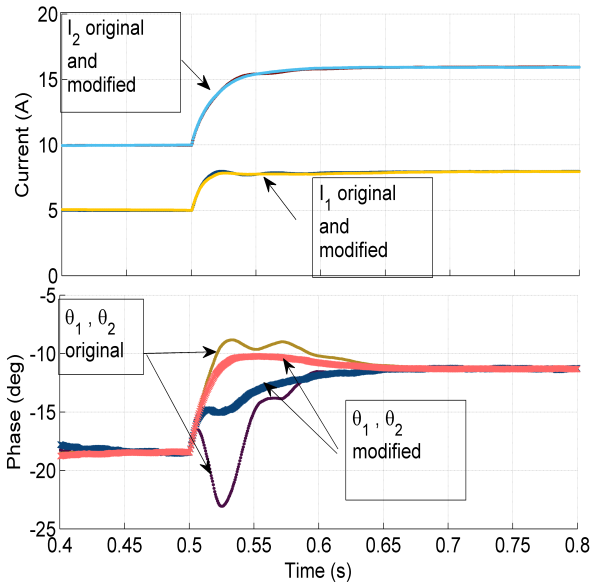


Figure 5-28: Output currents of Droop control after increasing the gain of voltage droop equation (k_1).

PLL). By designing the PLL to have a high bandwidth, SRF-PLL can achieve fast and accurate estimation of the frequency and phase of the input signal under ideal conditions. However, under distorted input conditions its performance is degraded. The disturbance rejection can be improved by reducing the bandwidth of the PLL at the expense of reduced detection speed [45]. Fig. 5-29 shows the frequency of the PLL for an unbalanced load with 92% unbalance factor. Notice that reducing the bandwidth of the PLL reduces the fluctuation in the frequency. However, and as will be shown, this small fluctuation does not have effect on the proposed control. Moreover, since this is a problem related to the PLL, regardless of what kind of control is used, the distorted input to the PLL will produce the same response.

While the solution of reducing the bandwidth is acceptable for some applications, for other applications it may not be acceptable since the dynamic speed of the PLL is reduced, such as low-voltage ride-through of distributed generators [45]. Some of the suggested solutions to achieve accurate phase estimation without compromising the dynamic response of the PLL are adding additional filtering stages within the control loop, or at the input of the PLL. Examples of

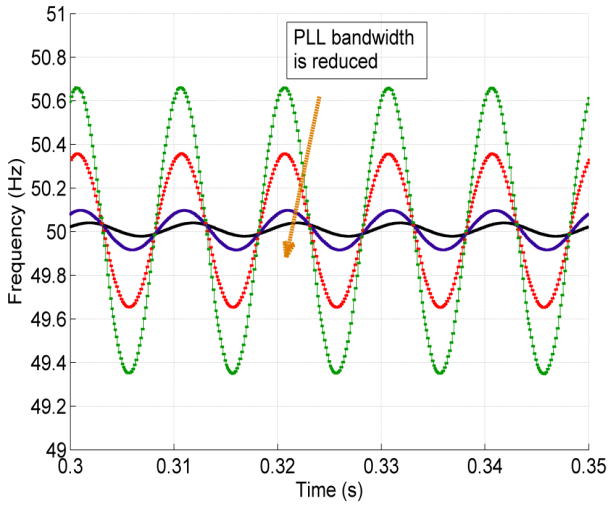


Figure 5-29: Frequency of PLL for unbalanced load with 92% unbalance factor for different PLL bandwidth.

such available solutions are: decoupled double synchronous reference frame PLL (DDSRF-PLL), multireference frame-based PLL (MRF-PLL), and multiple complex-coefficient-filter-based PLL (MCCF-PLL). Hence, for unbalanced load and nonlinear load conditions, it is better to use an advanced type of PLL.

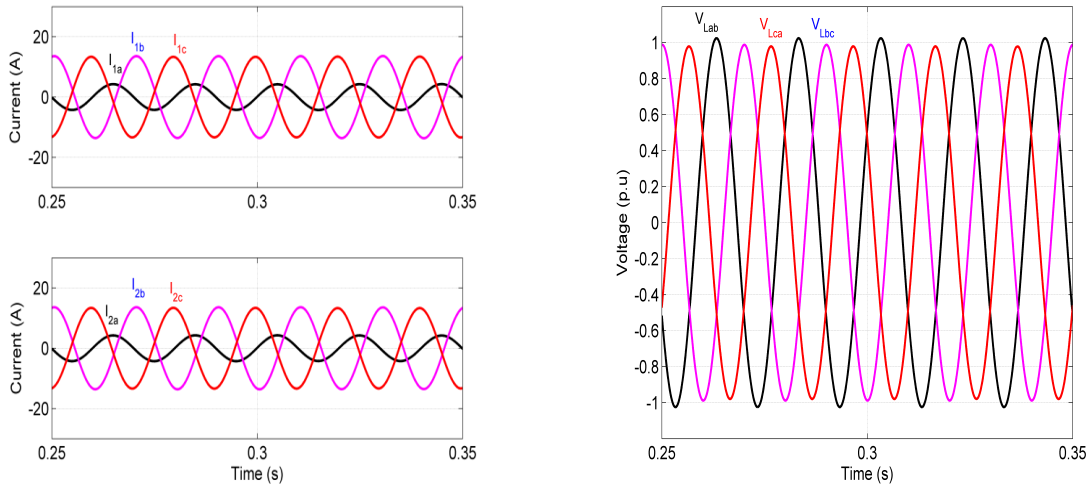
To test the performance of the proposed control under unbalanced load condition, the following load condition is considered: Phase A=500 W (25%), phase B = phase C=2 kW (100%). The results of output currents, load voltage, and PLL output frequency and phase are shown in Fig. 5-30a. The load unbalance factor is calculated as:

$$K_I = \frac{I_{max} - I_{min}}{I_{avg}}. \tag{5.27}$$

From Fig. 5-30a:

I_{1a}=4 A, I_{1b}=13.8 A, I_{1c}=13.7 A.

At the steady state, maximum current is 13.8 A, minimum current is 4 A, and average current is 10.56 A. The unbalance factor in this case is 92.8%.



(a) (b)

Figure 5-30: (a) Output currents, (b) load line-to-line voltages for unbalanced load condition.

The voltage unbalance factor, according to the NEMA (National Equipment Manufacturer's Association) standard, is:

$$K_V = \frac{V_{LLmax} - V_{LLavg}}{V_{LLavg}} \tag{5.28}$$

where V_{LLmax} is the maximum line-to-line voltage, and V_{LLavg} is the average line-to-line voltage.

From Fig. 5-30b: V_{ab}=1.02 p.u , V_{bc}=0.99 p.u, V_{ca}=0.985 p.u. According to ANSI C84.I and NEMA MG-I standards, electric supply systems should be designed and operated to limit the maximum voltage unbalance to 3%. Maximum line to line voltage= 1.025 p.u, average line to line voltage=0.9983 pu. K_V=2.17%, which is within the standard. Hence, the unbalanced condition has no big effect on the system.

5.8 Summary

Detailed analysis of a new autonomous control scheme was presented in this chapter. The simulation results validate the theoretical predictions of the proposed control. The proposed control relies on using the output current of each inverter to control the capacitor voltage and phase angle to indirectly control the load voltage. In the next chapter, experimental verification of the autonomous control method, as well as the communication-based control method (Chapter 4 will be presented.

Chapter 6

Hardware Implementation

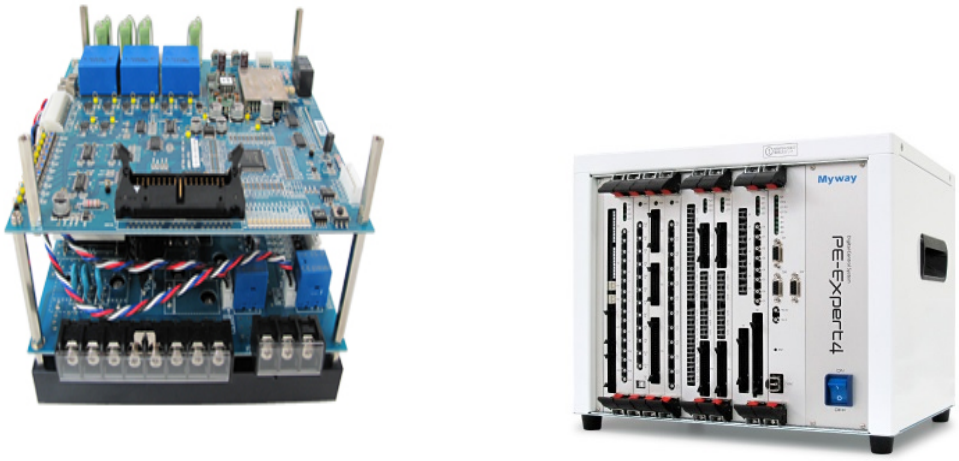
This chapter presents experimental verification of the two proposed methods in Chapters 4 and Chapter 5. The goal is to verify that the results obtained in the simulation and the theoretical predictions can be tested on a real system operating under different load conditions. Two inverters are used in the experiment with output LCL filters.

6.1 Experimental Setup

6.1.1 Inverter unit

To verify the validity of the proposed control methods, two 5 kVA, three phase inverters are used in the experiment. The inverter unit is shown in Fig. 6-1a. The specifications of the inverter are shown in Table 6.1. The inverter unit can be connected directly to the three phase grid and a built-in AC/DC rectifier converts the voltage to dc, or a separate dc source can be used as input.

There are built-in voltage and currents sensors as shown in Table 6.1. Two unit us equipped with two voltage sensors that can be used to measure two phase or line voltages, depending on the connection. The third quantity can be calculated mathematically. The two current sensors are used to measure the u and w phase output currents of the inverter, and the third quantity



(a) (b)

Figure 6-1: (a) 5 kVA inverter unit used in the experiments, (b) digital controller platform.

can be calculated.

6.1.2 Digital controller platform

Fig. 6-1b shows the PE-Expert 4 digital platform used for the control. The DSP used is TMS320C6657. In addition to the DSP board, two extension boards are used (one for each inverter unit). The extension board includes 8 AD converters, 6 optical gate signal connectors, digital input/output port, and up/down counter port. The specifications of the extension PEV board are shown in Table 6.2.

6.1.3 Voltage and current sensors

As mentioned earlier, there are two voltage sensors and two current sensors in the inverter unit. The voltage sensors are LEM LV25-P 500V/5V. The current sensors are LEM HX25-P 25A/4V. The circuit diagrams for the voltage and current sensors are shown in Fig. 6-2.

There are three voltage sensors in each inverter unit. The first one is at the dc input side of the inverter. The two other sensors are for monitoring the three phase output voltages. The

Table 6.1: Specifications of one inverter unit used in the experiment.

Parameter	Specification	Remarks
Rated capacity	5 kVA	
Rated current	14.4 A	
Rated voltage	230 V	
Overload capacity	120% for 1 minute	
Switching frequency	20 kHz	
Cooling method	forced air	
Dead time	at least 3 μs	
Insulation resistance	100 MΩ	
DC voltage sensor	$\pm$500 V to $\pm$ 5 V	
DC current sensor	$\pm$31.25 A to $\pm$5 V	
AC voltage sensors	$\pm$500 V to $\pm$ 5 V	two voltage sensors (u and w phases)
AC current sensors	$\pm$31.25 A to $\pm$5 V	two current sensors (u and w phases)
Control circuit power	DC24 V input	used for the control circuit (1.5 A)
Weight	2 kg	

Table 6.2: Specifications of the digital controller platform.

Parameter	Specification
3 Phase PWM	7 channels (6 gate channels and 1 brake arm)
PWM resolution	14 bits
Dead time	0-20 μs
Carrier frequency	1-500 kHz
ADC	14 bit, 8 channels simultaneous sampling
PWM channels connector	Optical connector
Digital I/O	32 channels

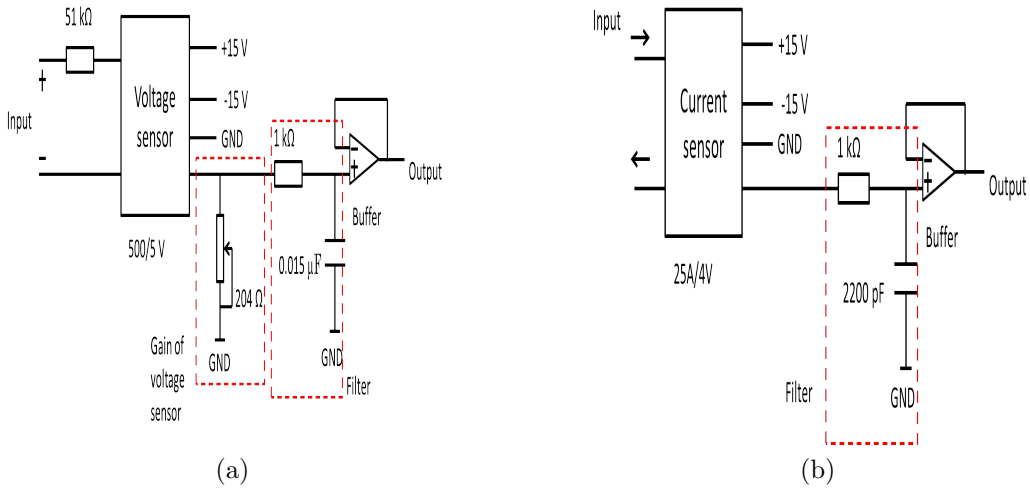


Figure 6-2: (a) Circuit diagram of voltage sensor, (b) Circuit diagram of current sensor.

voltage sensor has 5 inputs: two inputs for the voltage, two inputs for external ±15 V power supply, and one input for the ground. At the output of the voltage sensor there is a variable resistor to adjust the gain of the sensor. Normally, the initial setting value is 5 V for 500 V input voltage. The signal is then passed through a low pass filter for noise attenuation. Then, the signal is sent to the output through a buffer. The output signal is sent to a connector which is connected to the AD converter of the extension board. The detected signal is also used in the protection circuit to disconnect the power from the inverter in case the voltage exceeds a certain value.

The current sensor circuit is shown in Fig. 6-2b. The current passes through the hall effect sensor. the output signal passes through a low pass filter and a buffer before it is sent to the connector and the ADC converter in the extension board. There are three current sensors: one input dc current sensor, and two output U and W phase current sensors. The current sensor signal is also used in the protection circuit for over current detection.

The signals from the sensors are connected to a control board, the control board is connected to the AD converter in the extension board. The control board includes eight ports. Six of the ports are connected to the voltage and current sensors (1 dc voltage sensor, 2 output voltage

sensors, 1 dc current sensor, and 2 output current sensors). The last two ports are connected to external analogue sensors and can be used to detect external signals and connected to the AD converter. The external analogue connectors accept voltage levels in the range ±5 V. In the experimental setup, the two external analogue connectors are used to measure the U and W capacitor currents of the LCL filters. External current sensors are used to detect the current signals and convert them to voltage signals before sending them to the AD converter.

6.1.4 Three phase rectifier and IGBT switches

Additional circuits were built to test the system under nonlinear load conditions and step load variations. IGBT (insulated-gate bipolar transistor) switches are used, with each package containing 2 IGBT switches. The IGBT module is 2MBI400VD-060-50 from Fuji Electric. The specifications of the unit are shown in Table 6.3. The gates of the IGBTs are driven by a gate drive optocoupler ACPL-337J.

Table 6.3: Specifications of one IGBT module.

Items	Conditions	Characteristics
Collector-Emitter voltage	maximum value	600 V
Gate-Emitter voltage	maximum value	±20 V
Collector current	maximum value	400 A
Internal gate resistance		2.3Ω
Reverse recovery time	forward current=400 A	0.2μs
Gate-Emitter threshold voltage	V_{CE}=20 V, I_C=400 mA	6.7 V

Each IGBT module includes two IGBTs. The emitter of the upper IGBT is connected with the collector of the lower IGBT (C2E1). Three IGBT modules are required for the experiment. Depending on what kind of experiment, there are two configurations as shown in Fig. 6-3. For a three phase rectifier configuration, the circuit diagram is shown in Fig. 6-3a. The IGBTs are switched off by applying -15 V (logic 0) to the gate-emitter junction, and the parallel free-wheeling diodes are used to form a three phase passive rectifier. The three phase input lines are

connected to the terminals C2E1 of each IGBT module, and the dc voltage is obtained at the output between the terminals C1 and E2.

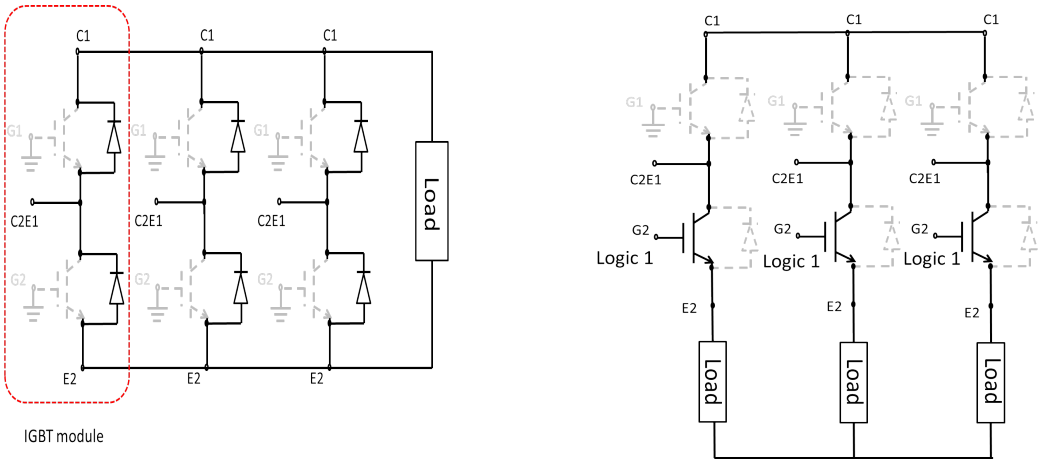


Figure 6-3: (a) Circuit configuration of a passive rectifier, (b) 3 phase IGBT switch.

The circuit is modified so that it can function as a three phase switching device to connect/disconnect a three phase load, as shown in the configuration in Fig. 6-3b. The upper IGBTs are switched off by applying -15 V voltage to the gate-emitter junctions. The three phase input is connected the same as in the rectifier circuit (to terminals C2E1). The three phase load is connected in series with the lower IGBTs in Y configuration. When a +15 V signal is applied to the gate G2, the IGBTs are turned on and the load is connected to the three phase voltage. When a -15 V signal is applied to the gate G2, the IGBTs are turned off and the load is disconnected.

6.1.5 LCL Filter

An LCL filter is connected at the output of each inverter unit. Two different types of inductors are used in the filter. The inverter-side inductor is L_0 and the output side inductor is L_1. The specifications of each inductor are shown in Table 6.4.

The capacitors used in the filters are GENTEQ Gem III 97F8040 film general purpose AC

Table 6.4: Specifications of the inductors used in the LCL filters.

Specification	L_0	L_1
Inductance	600 μH±10%	1200 μH±10%
Rated current	15 Arms	15 Arms
Saturation current	42 Adc (50% decrease in L_0)	30 Adc (30% decrease in L_1)
Withstand voltage	2.4 kVac for 1 sec	2.4 kVac for 1 sec
Insulation resistance	500 Vdc 100 MΩ	500 Vdc 100 MΩ
DC resistance	55.6 mΩ	39.6 mΩ
Core	dust core	silicon steel core
Maximum temperature	155°C	155°C
Power loss	13.6 W	8.9 W

Capacitor with quick connect blades termination, unpainted aluminum case and terne plate steel cover. The specifications of the filter capacitors are shown in Table 6.5.

Table 6.5: Specifications of the capacitor used in the LCL filter.

Specification	Value
Capacitance	40 μF±6%
Leakage current	30 μA maximum
Operating temperature	-40°C to 70°C
Case material/finish	Unpainted Aluminum case, Ternplate steel cover
Equivalent series resistance	0.0190 Ω

6.1.6 Structure of one inverter unit

Fig. 6-4 shows the structure of one inverter with output LCL filter and the DSP. The gate signals are sent to the inverter via a 7 channel optical cable (6 channels for gate signals and one channel for brake arm at the dc side).

The feedback signals from the inverter are sent to the DSP via an 8 channel coaxial SMB cable. The measured signals are the U and W inverter-side currents (i_0), the U and W output currents (i_1), the U ans W capacitor phase voltages (E_1), and the U and W capacitor currents (i_c). The experimental setup of the two inverters and the LCL filters are shown in Fig. 6-12.

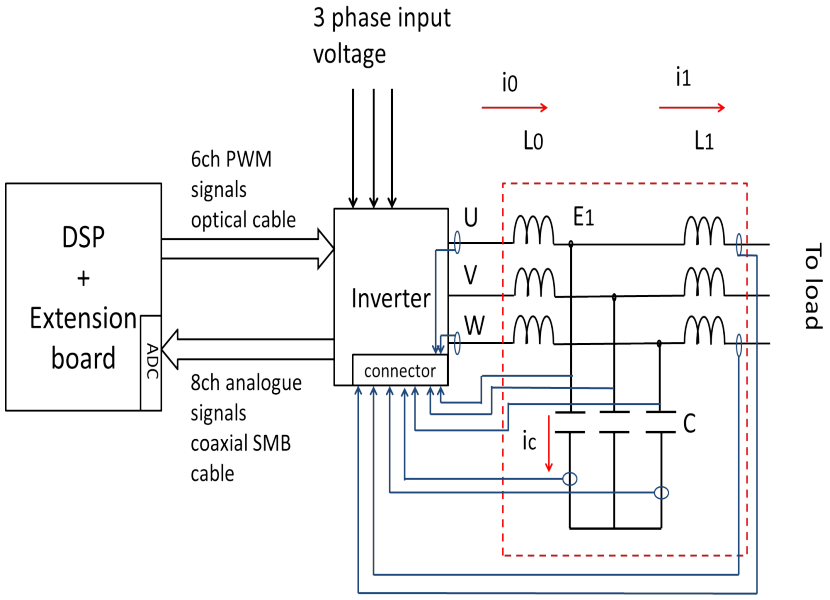


Figure 6-4: Circuit diagram of DSP, three phase inverter, and output LCL filter.

6.2 Communication-based equal load sharing

This section shows the experimental results of two parallel inverters controlled using the proposed communication-based control scheme. The output currents of the two inverters are used in the control unit to calculate the reference current. The reference capacitor voltage is then calculated.

The reference phase voltage is chosen as 100 Vrms, which is the reference load voltage. Fig. 6-6 shows the three phase capacitor voltages and output currents for the two inverters. The load is 400 W resistive.

The effectiveness of the control scheme in distributing the load equally between the inverters can be checked by comparing the output currents of the two inverters. The single phase capacitor voltage and current of the two inverters are shown in Fig. 6-7. Notice that the capacitor voltages of the two inverters are equal in amplitude and have the same phase.

Fig. 6-8 shows the dq-components of the reference capacitor voltage for the two units. The reference dq-components of the capacitor voltage of the two units are calculated using (4.4)

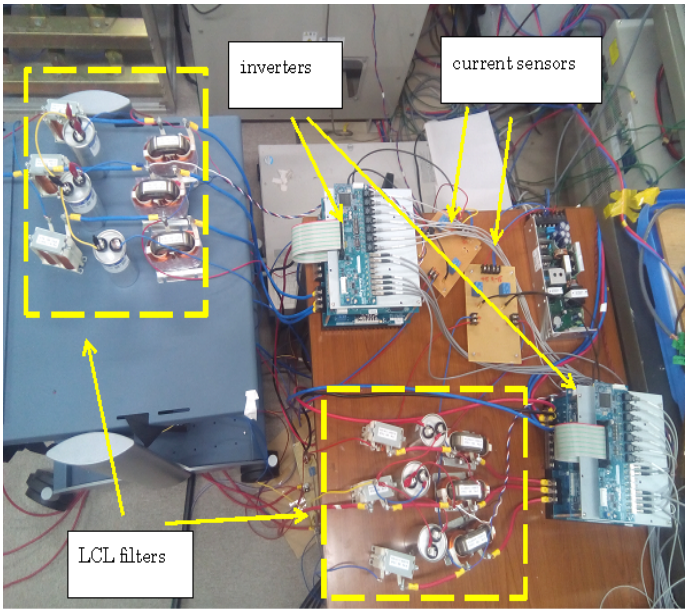
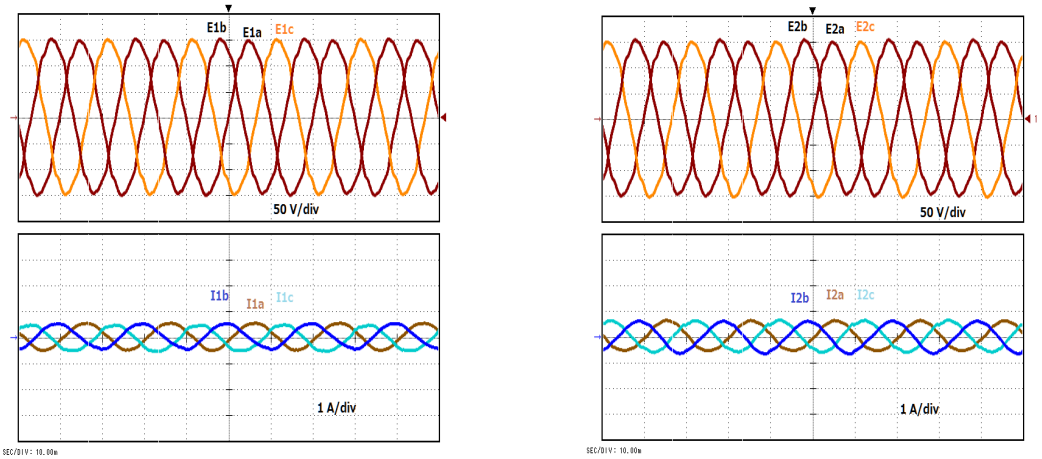


Figure 6-5: Experimental setup of two inverters, filters, and current sensors.



(a) (b)

Figure 6-6: Waveforms of three phase capacitors voltages and output currents for two parallel inverters controlled using communication-based control.

and (4.5). For a 400 W load, at 100 V_{rms} phase voltage, the load current is 1.9 A (peak). Accordingly, the reference current for unit 1 is equal to the load current divided by two (1.45 A). Using (4.4) and (4.5), and using the parameters of the filters, the dq components of the reference capacitor voltage are: E_{ref1d} =141.47 V, and E_{ref1q} = 0.546 V. As shown in Fig. 6-8, the reference dq-components of the capacitor voltage (E_{ref1d} and E_{ref1q}) equal the calculated

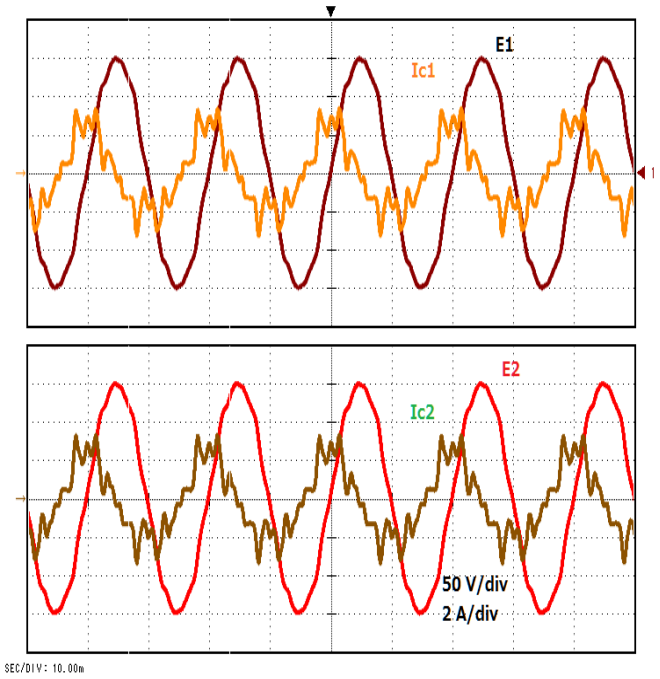


Figure 6-7: Single phase capacitors voltages and capacitors currents for two inverters.

values.

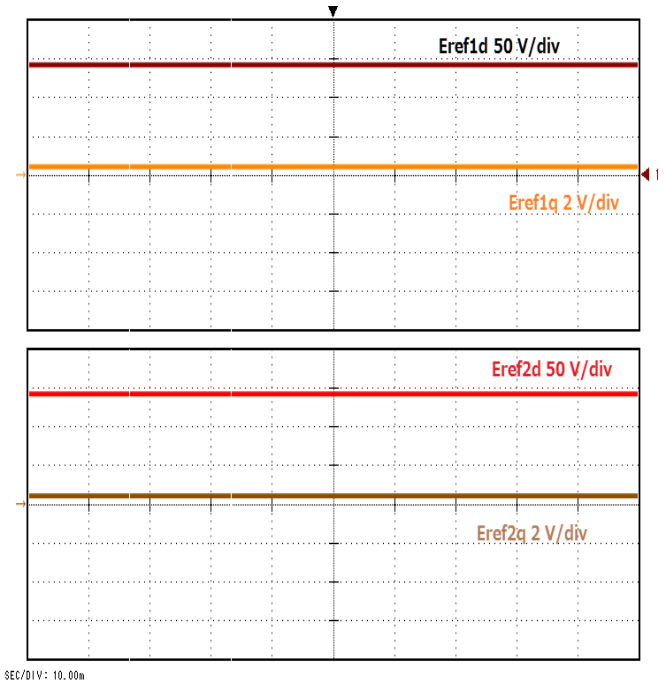


Figure 6-8: DQ reference capacitors voltages of the two inverters.

The output currents of the two inverters, as well as the load current, are shown in Fig. 6-9.

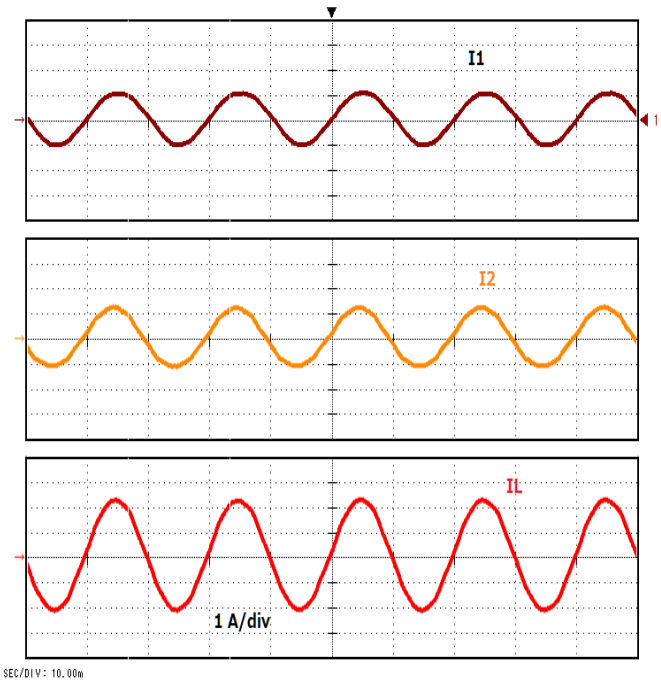


Figure 6-9: Output currents and load current.

Notice that the load current is shared equally between the two inverters. Notice also that the two currents are equal and have the same phase. The phase-to-ground load voltage is shown in Fig. 6-10. As shown in the figure, the voltage equals the reference value, which is 100 V_{rms} or 141.42 V_p.

Next, the effect of applying a step load on the performance of the system is demonstrated. The reference capacitors voltages and output currents of the two units are shown in Fig. 6-11a. The load is increased from 400 W to 1 kW as shown in the figure. When the step load is applied to the output, an abrupt increase in the output current is detected by the UPSs. Consequently, the reference capacitor voltage is updated. The reference voltage is then used to control the capacitor voltage of the inverter. At the steady state, the system reaches a new equilibrium point at which the output currents of the two inverters are equal. The load current is shown in Fig. 6-11.

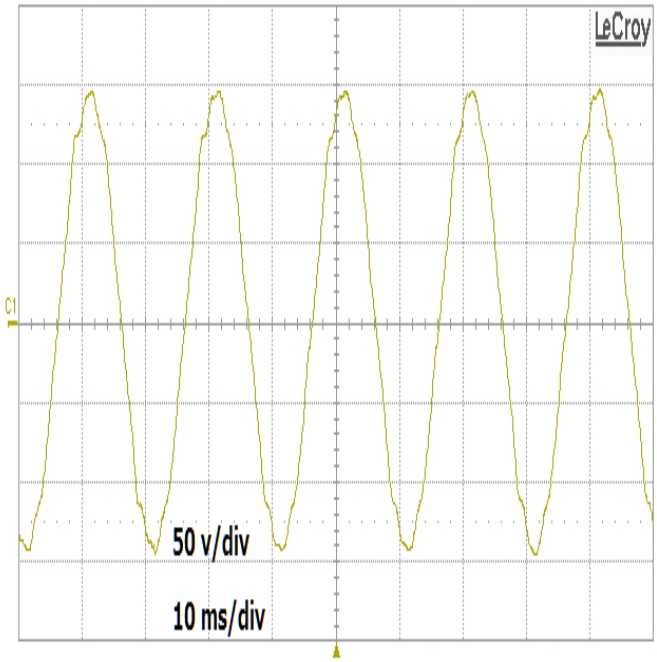
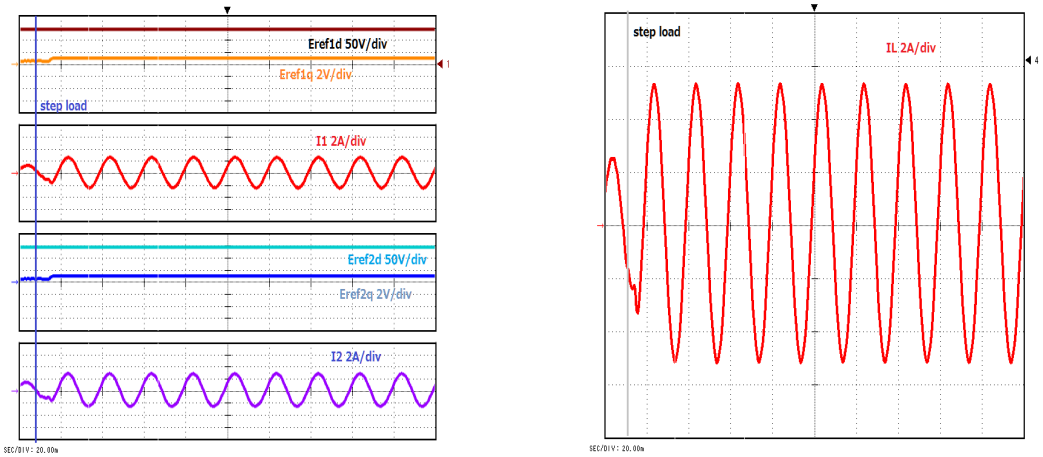


Figure 6-10: Load voltage-resistive load.



(a) (b)

Figure 6-11: Communication-based control-step load (a) dq reference capacitors voltages and output currents, (b) load current.

6.3 Autonomous control

This system shows the results of the proposed autonomous control scheme for the same system of two parallel inverters, without exchanging information between the UPS units.

6.3.1 Resistive load

A 1 kW load is connected at the output of the inverters. Fig. 6-12a shows the output currents of the two parallel inverters. The inverters are intentionally operated such that they supply unequal output currents at the beginning. The system switches to the proposed autonomous control as shown in the figure and the output currents become equal. Fig. 6-12b shows the capacitor voltage and capacitor current of the two inverters. Notice that E_1 and E_2 are equal and are in-phase. The switching harmonics in the current pass through the capacitor of the filter as shown in the figure.

Based on equation (5.11), the reference dq-components of the capacitor voltage can be calculated. For a resistive load, $I_{1q} = 0$ in (5.11). For a 1 kW load, the load current is 4.7 A_{peak}. Accordingly, the reference current for unit 1 is 2.35 A. Using (5.11), and using the parameters in Table 3.1, the dq components of the reference capacitor voltage are: E_{ref1d} =141.51 V, and E_{ref1q} = 0.89 V. The calculated values of the dq reference capacitor voltage for the two parallel inverters are confirmed experimentally as shown in Fig. 6-12c. From the dq values, the magnitude and phase angle of the reference capacitor voltages are calculated as: $|E_{ref1}|$= $|E_{ref2}|$=141.4658 V, and $\delta_{ref1} = \delta_{ref2} = 0.36°$. The magnitudes and phase angles are shown in Fig. 6-12d.

The output currents I_1 and I_2 are shown in Fig. 6-12e. Notice that the load current is shared equally between the two inverters. The load current is also shown, which is equal to the summation of the output currents of the two inverters.

Finally, the load voltage is shown in Fig. 6-12f. As shown in the figure, the load voltage equals the reference value which is 100 V_{rms} (141.2 V_{peak}).

6.3.2 No load condition

In this case the two inverters are connected in parallel with no load at the output. Fig. 6-13a shows the capacitor voltages of the two inverters, the inverter-side currents (I_{01} and I_{02}), and the output currents. Notice that the capacitor voltages of the two inverters remain equal under the proposed autonomous control scheme even under no-load condition. Notice also that the only currents following in the inverters are the capacitor currents, while the output currents are very small. Fig. 6-13b shows the load voltage which follows the reference value.

6.3.3 Step load condition

The two parallel inverters are connected to a load. To verify the dynamic stability of the proposed method, a step-load change of 60% is considered. The results are shown in Fig. 6-13c and Fig. 6-13d. The experimental results show that the output currents increase while maintaining equal distribution without any significant effect on the load voltage.

6.3.4 Nonlinear load condition

Two parallel inverters are connected to a rectifier load. A 4600 μF capacitor is connected at the output of the rectifier. The results are shown in Fig. 6-13e and Fig. 6-13f. Notice that the load harmonics are shared equally between the two inverters. The total harmonic distortion in the load voltage is 3.66%, which is within the standard of IEEE 519-1992 of 5%.

6.4 Summary

Experimental verification of the proposed control was presented in this chapter using a system of two parallel inverters connected to a load. The inputs of the inverters are connected to the three phase grid, and a three phase rectifier is used to convert the three phase voltage to dc

voltage. The experimental results are in good agreement with the simulation. Different kinds of load conditions were considered, such as no-load, step load, and non-linear load.

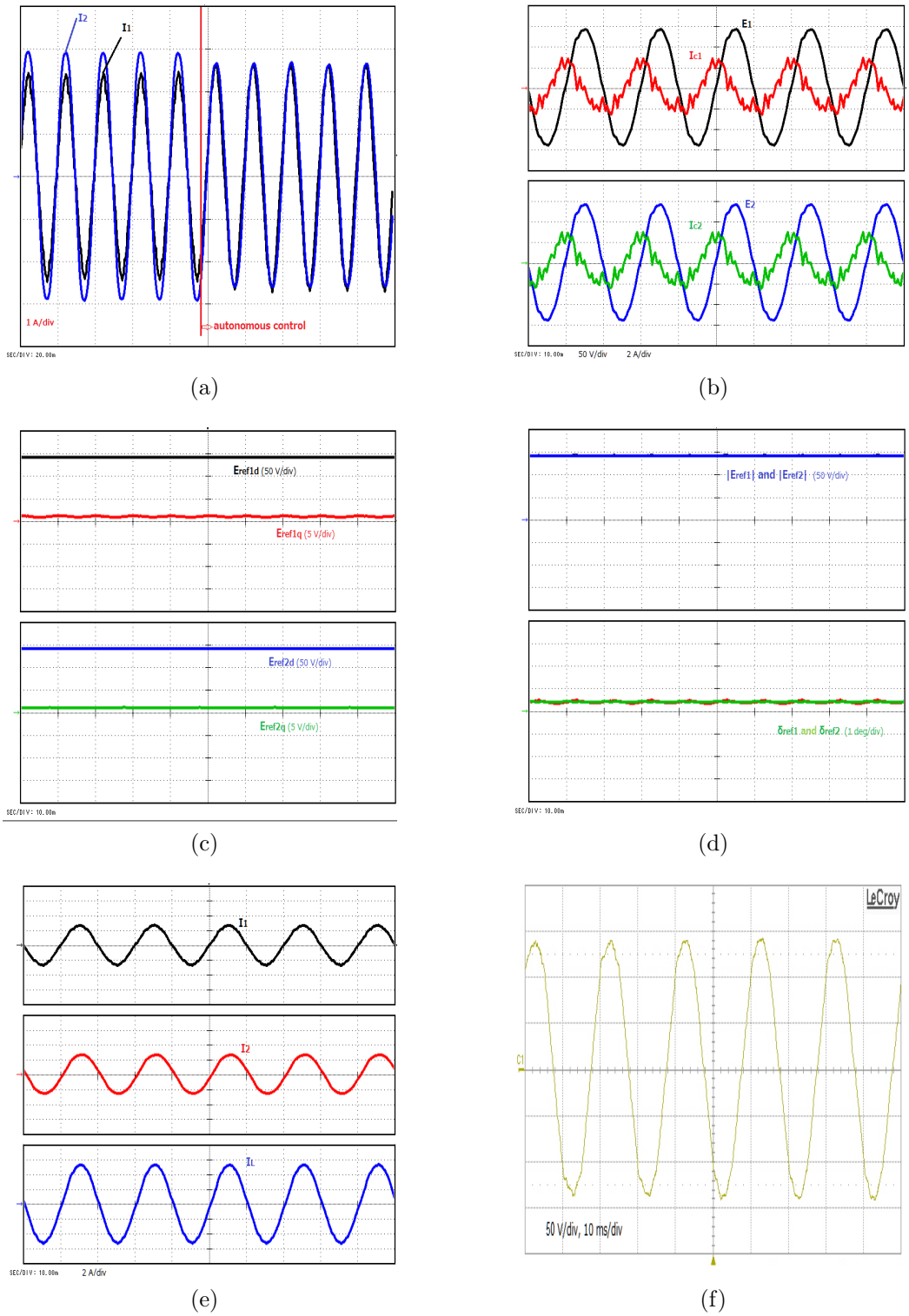
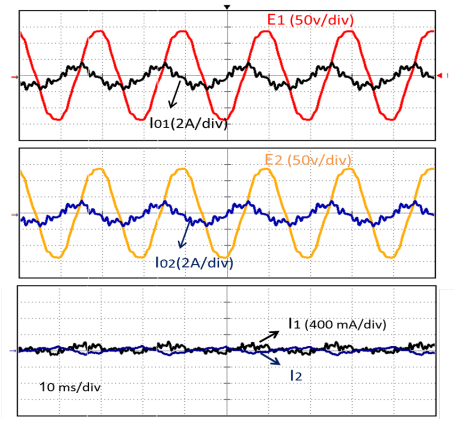
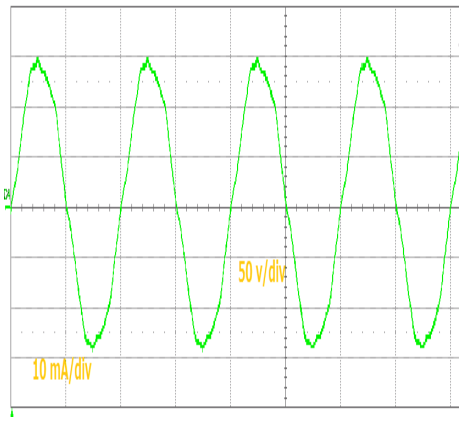


Figure 6-12: Experimental results of two parallel inverters (a) output currents I_1 and I_2 showing transition period to autonomous control, (b) capacitor voltage and capacitor current of both inverters, (c) dq-components of the reference capacitor voltages of the two units, (d) magnitude and phase angle of reference capacitor voltages, (e) output currents I_1 and I_2, and load current I_L in the steady state using the autonomous control scheme, (f) load voltage V_L.



(a)



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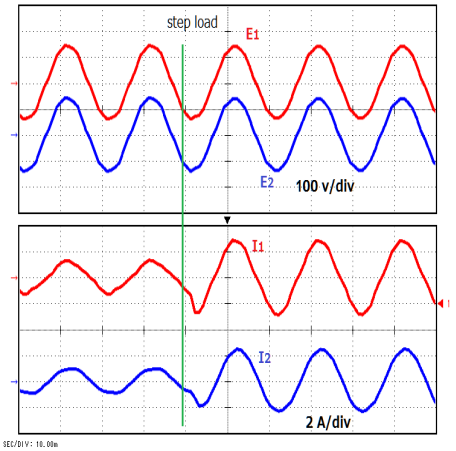
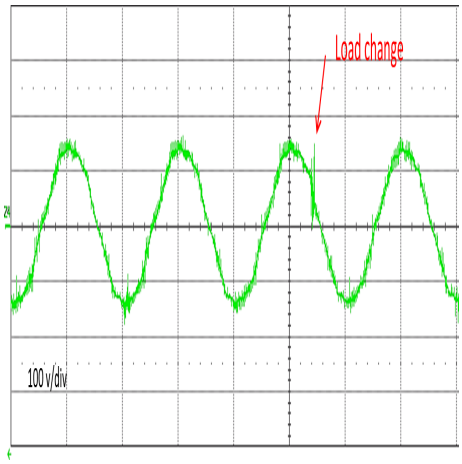
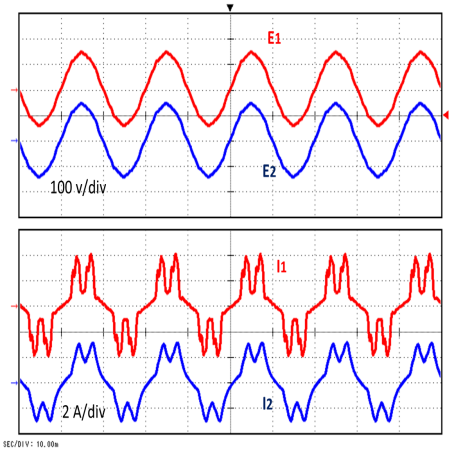


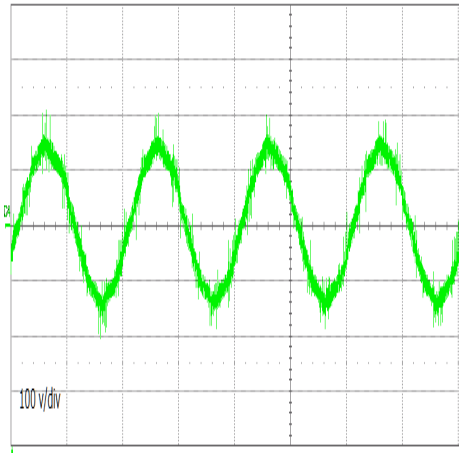
(c)



(d)



(e)



(f)

Figure 6-13: Experimental results of two parallel inverters (a) voltages and currents waveforms for no-load condition, (b) load voltage for no-load condition, (c) waveforms for step-load condition, (d) load voltage for step-load condition, load is increased by 60%, (e) waveforms for non-linear load condition, and (f) load voltage for non-linear load condition.

Chapter 7

Summary and Conclusions

7.1 Summary

Uninterruptible power supply systems have existed for many decades to provide stable and reliable power networks. However, with the advancement in technology and power electronic devices, combined with the environmental challenges facing the world, such as climate change and the sustainability of energy sources, it has become necessary to re-structure the already existing power systems. Much of the research in energy sector in the present is focused on the integration of new components into the grid in what is called distributed generation (DG). The process of adaptation of the emerging technology into the existing installations can be expedited by the clustering of a large system into smaller ones. Distributed generation is especially effective when different kinds of energy sources are available (such as solar and wind energy).

Numerous papers that discuss different control techniques of parallel inverters are available in the literature. Nevertheless, parallelism of inverters is still a challenging problem. Mainly due to the lack of a universal control scheme that can be used for all applications. Instead, most of the research is focused on the investigation of control techniques that are suitable for particular applications, but not for others.

In our attempts to overcome some of the drawbacks of the available control techniques for

DG systems, we have proposed a new, robust, autonomous control scheme in this dissertation. This presentation started with an overview of the fundamentals of uninterruptible power supply systems and control strategies. The basic structure and types of UPS systems (*i.e.,* on-line, off-line, and line-interactive UPS systems) are discussed in Chapter 2. In the same chapter, the theoretical and practical issues concerning the parallelism of inverters and DG systems are presented. The most available control techniques (*viz.,* active load sharing and Droop control), are briefly discussed for the sake of comparison with the proposed technique later on.

The fundamentals of three phase inverters and the small-signal model in the dq synchronous frame, along with the structure and types of PLL configurations are discussed in Chapter 3. The inverter model is used for stability analysis of multi-loop control and resonance damping of the output filter.

Next, the main contributions in this work are presented in Chapter 4 and Chapter 5. We present two new control techniques:

- Communication-based control scheme (Chapter 4): this control scheme relies on communication between parallel inverters and can achieve excellent load current distribution.

- Autonomous control scheme (CCVC) (Chapter 5): this technique can be used to control parallel inverters without communication between the units. Compared to the traditional droop method, the proposed method is fast and has high accuracy in achieving current distribution. Moreover, unlike the Droop control, the load voltage and frequency are constant.

The proposed autonomous control scheme is called current-dependant capacitor voltage control (CCVC) scheme. Compared to the traditional droop control, the new method can achieve autonomous control of parallel inverter with no voltage or frequency deviations. The proposed method also exhibits superior transient state performance and fast response to load variations

compared to the droop method (*cf.* Chapter 5).

A comparison between active load sharing (ALS), Droop method and the proposed autonomous control method (CCVC) is presented in Table 7.1. The proposed method encompasses the advantages of the ALS and Droop methods in terms of precision, constant voltage and frequency regulation, and does not require any communication links or signal injection.

Table 7.1: Comparison between Active Load Sharing, Droop, and proposed autonomous control methods.

Control Method	Advantages	Disadvantages
ALS	• Excellent voltage regulation. • Precise current sharing. • No voltage or frequency deviation.	• Requires communication links • Low reliability and not flexible.
Droop	• No communication links. • High reliability, expandability, and flexibility. • Voltage and frequency regulation can be improved.*	• Poor voltage and frequency regulation. • Slow dynamic response. • Poor harmonics sharing.
CCVC	• No communication links required. • Precise current sharing. • No voltage and frequency deviation. • Easy to implement.	• For unbalanced or nonlinear load, advanced PLL may be required.

* As has been discussed in Chapter 2, recent improvements on the droop method have been done. However, these improvements come at the expense of adding additional communication networks, signal injection, or cost.

Finally, experimental results are presented in Chapter 6 to verify the validity of the proposed methods. Different load conditions are tested, including no-load, step-load, and non-linear load conditions. The experimental results confirm that the proposed methods are practical and effective.

7.2 Recommendations for Future Research

The work presented in this dissertation provides detailed analysis of a new approach for autonomous control of parallel inverters. Although the discussion provided here provides a com-

prehensive presentation to implement the proposed algorithm on a system of parallel UPS modules, the following points are identified as potential areas for future work:

- Complex Microgrid configurations: The present study has been confined to bus-connected load systems. That is, there is a point of common coupling (PCC) in the system to which all inverters and loads are connected. However, in some configurations the DGs and loads are arbitrarily interconnected (*e.g.,* the looped and mesh networks). In this case, the control becomes more challenging.

- Unbalanced loads and fault conditions: Only balanced load condition is considered in this study. The effect of unbalanced loads and different types of faults on the system can be considered in the future.

- Control in the $\alpha - \beta$ stationary frame: In this work, we have implemented the controller in the dq synchronous frame. All voltage and current signals are transformed to dc signals, and a PI controller is used. Transformation to the synchronous frame requires a common reference voltage and a PLL to extract the reference phase angle. Control in the stationary frame, on the other hand, does not involve transformation and might offer some advantages. A different kind of controller is required in this case, such as a proportional resonant (PR) controller.

- Control of single phase inverters: In the case of single phase inverters, a virtual secondary circuit that is perpendicular to the single-phase circuit can be used to transform the voltage and current quantities to the dq synchronous frame.

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