Extremely Energy-Efficient Integrated Circuits Using Adiabatic Superconductor Logic

断熱型超伝導論理回路を用いた超低電力集積回路の研究

A dissertation presented

by

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Abstract

Complementary metal-oxide-semiconductor (CMOS) circuit technology has sustained the exponential growth of computing power for more than 20 years. However, it has been estimated that the power consumption of a next-generation supercomputer will exceed the power supplied from a single power plant. This indicates the need to dramatically improve the energy efficiency of logic devices to achieve future high-end computers.

As an extremely energy-efficient logic, we proposed and have been investigating adiabatic quantum-flux-parametron (AQFP) devices. Due to adiabatic switching operations, its bit energy (energy dissipation per bit) can go below $I_c\Phi_0$, where I_c is a critical current of a Josephson junction and Φ_0 is a single-flux-quantum (SFQ). $I_c\Phi_0$ corresponds to the energy dissipated at every 2π phase transition in conventional non-adiabatic superconductor logics.

We have two objectives in this study. One is to reveal physical energy bounds on computation through investigation of the energy efficiency of AQFP logic. The other is to develop fundamental circuits necessary for energy-efficient computing systems using AQFP logic.

First, we numerically and experimentally demonstrated the sub-$I_c\Phi_0$ bit-energy operations of AQFP gates to show that AQFP gates operate in adiabatic modes. We investigated the dependence of energy dissipation and operation margins on circuit parameters. After optimizing the parameters, we calculated the bit energy and the bit error rate at 4.2 K to verify the sub-$I_c\Phi_0$ bit-energy operations at a finite temperature. Additionally, we measured the bit energy of an AQFP gate using a superconductor resonator-based method.

Secondly, we numerically demonstrated the sub-k_BT bit-energy operations, where k_B is the Boltzmann constant and T is temperature, to show that AQFP gates can operate beyond thermodynamic energy bounds. We investigated the dependence of energy dissipation on operation frequencies and damping conditions of Josephson junctions. By using underdamped junctions, we confirmed the sub-k_BT bit-energy operations at a finite temperature thorough circuit simulation. This result indicates that there is no minimum energy dissipation required for the operations of AQFP gates unless the entropy of the system decreases, which corresponds to the Landauer's argument

on the minimum energy dissipation for computation. Also, we discussed quantum-mechanical energy bounds and experimentally demonstrated AQFP gates with underdamped junctions.

Additionally, we investigated reversible computing using AQFP logic with underdamped junctions, in order to deal with an important but unresolved question: "Is reversible computing achievable by using practical devices?" We built a purely reversible gate by using AQFP gates, which we designated as the reversible quantum-flux-parametron (RQFP) gate. We calculated its energy dissipation and confirmed that there is no minimum energy dissipation for reversible logic operations using RQFP gates. To the best of our knowledge, these are the first calculation results that show no minimum energy dissipation in reversible computing that use practical circuit structures. Moreover, our experimental results have demonstrated the logical and physical reversibility of the RQFP gate. We believe that this is the first demonstration that shows both logical and physical reversibility using practical devices.

Finally, we proposed a novel energy-efficient latch for AQFP logic, which we designated as the quantum-flux-latch (QFL). Latches are necessary circuitries in large computing systems but had been missing in AQFP logic. We discussed its energy efficiency through simulation and experimentally demonstrated correct operations of the QFL and a 1-bit shift register using QFLs. Also, we proposed high-speed test circuits using QFLs and experimentally demonstrated logic operations of AQFP circuits at high speed.

We strongly believe that our results showed the extremely high energy efficiency of AQFP logic. These results will move the AQFP logic to practical usage as extremely energy-efficient integrated circuits.

Acknowledgment

I'd like to express huge thanks to everyone who supported me through my PhD studies at Yokohama National University.

First, I'd like to thank my advisor, Prof. Nobuyuki Yoshikawa for his grateful advice and support in both research and my life. His open and kind attitude always welcomed discussions with me, and eventually accelerated my research progress. One of the most impressive words from him was "Don't think about the future too much. Do what you can do now". These generous words relieved me from anxiety and stress during my PhD studies. I'm sure that, if I hadn't met him, I could not spend such a fruitful time during my precious 20s.

Also, I'd like to thank Prof. Yuki Yamanashi (Yokohama National University) for his valuable advice in research. Especially, he helped me improve my writing and presentation skills. His great passion for science and technology has driven my interest to be a researcher.

I have investigated novel energy-efficient latches for AQFP logic under the tutelage of Prof. Theodore Van Duzer at University of California, Berkeley for one month since November 2012. I'd like to appreciate Prof. Theodore Van Duzer for giving me such a great opportunity to do research at Berkeley, Dr. Stephen R. Whitely and Dr. Lizhen Zheng for useful discussions. Special thanks go to Dr. Thomas Ortlepp (now at CiS Research Institute, Germany). He has taught me lots of skills to design superconducting circuits and also has given me so many ideas to achieve latches.

One of the most important tools to carry out my PhD studies was the 3D inductance extractor, InductEx, which was invented and developed by Prof. Coenrad Fourie (Stellenbosch University, South Africa). The nature of AQFP logic needs 3D inductance extraction for good layout design. I'd like to appreciate Prof. Coenrad Fourie for improving the InductEx and kindly responding to my questions.

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Finally, I'd like to express my deepest gratitude to my family for their care and love. I feel their support always pushes me towards a better direction.

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Contents

Chapter 1

Introduction

In this chapter, we briefly describe the motivation and objectives of our research, following a brief introduction to research background. First, we show that the minimum energy bound for computation is determined by the thermodynamic connection between information and energy. We also describe how far complementary metal-oxide-semiconductor (CMOS) technology is from the bound. Then we introduce adiabatic quantum-flux-parametron (AQFP) as an extremely energy-efficient logic, which is an adiabatic superconducting device. We show its operation principle and circuit characteristics. Following these description about energy limitation in computation, we define the purpose of our research on energy-efficient integrated circuits using AQFP logic. Additionally, we introduce the overviews of general superconductor logics and reversible computing.

1.1 Background

Recent supercomputers achieve the computing power of more than 10 PFLOPS with power consumption in excess of 10 MW. Figure 1.1 shows the energy efficiency of the 1st-ranked computers in recent TOP500 [TOP500]. It is clear that power consumption increases as computing power increases, eventually reaching around 200 MW for 1 EFLOPS [Geist10, Ball12, Service12, 村上 13]. This power costs more than $200 million per year and is difficult to supply safely, which indicates that each supercomputer needs a power plant in the near future. Hence, energy efficiency is now the most important metric of advancement in modern computer design [Borkar11]. Many post-CMOS devices are under research to obtain higher energy efficiency [ITRS], however, most of them could obtain slightly higher efficiency. This is because they are non-adiabatic devices, and their minimum energy dissipation is thermodynamically determined, as will be described later. It is true that none of post-CMOS deices in ITRS ERD have demonstrated switching energy lower than that of CMOS ($= 1.00 \times 10^{-16}$ J).

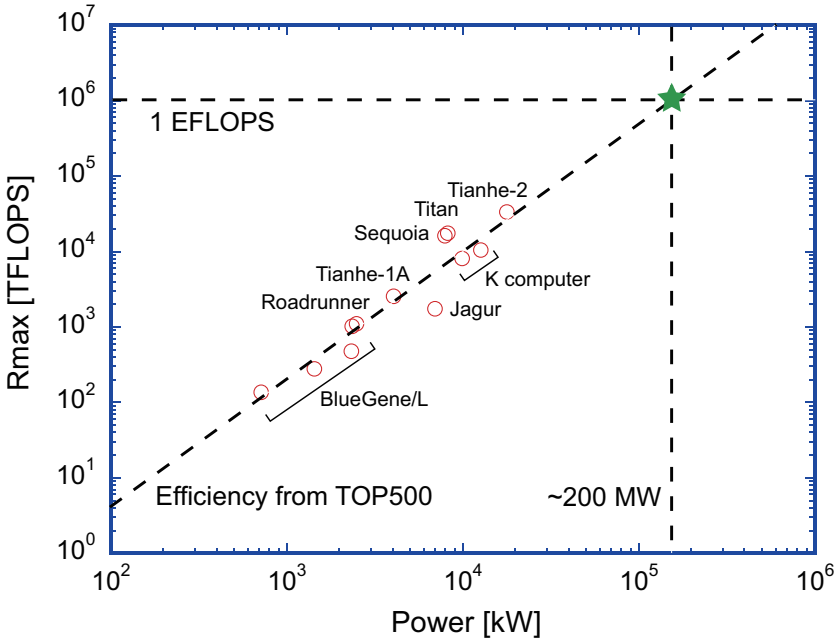


Figure 1.1: The 1st-ranked computers in recent TOP500.

Therefore, an extremely energy-efficient logic device based on a totally new switching operation principle is needed to achieve future high-end computers.

1.2 Motivation

1.2.1 Connection between information and energy

What is the minimum energy dissipation for computation? This is a very fundamental and important question in pursuing higher energy efficiency in computation. The answer has been already predicted by Rolf Landauer in his paper in 1961 [Landauer61]. He argued that there is no minimum energy limitation for computing if there is no reduction in entropy, which is well known as the Landauer's principle. Here we explain the principle by taking AND as an example. AND generates a 1-bit output from 2-bit inputs. During this logic operation, 1-bit information is erased and entropy of $k_B \ln 2$ is reduced, where k_B is the Boltzmann constant. Thereby, heat of more than $k_B T \ln 2$ must be generated in order not to violate the second law of thermodynamics, where T is temperature. Also, the reduction in entropy is linked to logical reversibility [Bennett73]. The gate is considered to be logically reversible, if its inputs are uniquely determined from its outputs. In irreversible logic operations, such as AND, OR, and XOR, the information of inputs are erased and the entropy reduces. The Landauer's

principle imposes the Landauer bound of $k_B T \ln 2$ as the minimum energy dissipation on these irreversible logic operations.

From the physical point of view, the Landauer bound corresponds to the minimum energy dissipation in irreversible or non-adiabatic switching operations. Figure 1.2 shows the time sequence of potential energy during a non-adiabatic switching operation. Note that most of logic devices, including CMOS and conventional superconductor logics, switch non-adiabatically in this manner. A bi-stable device (= 1-bit memory) has double-well potential energy as shown in Fig. 1.2a, where each well corresponds to the logic states of "0" and "1", respectively. The two distinguishable states are separated by the energy barrier, E_b. For conventional superconductor logics, E_b corresponds to $I_c \Phi_0$, where I_c is a critical current of Josephson junctions and Φ_0 is a single-flux-quantum (SFQ). When the device is supplied with sufficiently large energy (Fig. 1.2b), the potential varies from bi-stable to mono-stable, resulting in sudden and irreversible state transition (jump on the potential). During this physically irreversible sequence, the energy corresponding to E_b is dissipated as heat. The bit error rate (BER) of a non-adiabatic device, Π, where the error is caused by thermal noise, is determined as [Zhirnov03]: $\Pi = \exp(-E_b/k_B T)$. The BER reaches 0.5 for $E_b = k_B T \ln 2$, which results in an indistinguishable state. Therefore, the minimum energy dissipation for a non-adiabatic switching operation corresponds to the Landauer bound. This is because the non-adiabatic switching operation is physically, as well as logically, irreversible. More detailed discussions between logical and physical reversibility were reported in [Likharev82].

After long discussions and numerical analyses of this energy bound [Shizume95, Dillenschneider09, Sagawa09], some very recent experimental demonstrations that confirmed its validity have been reported [Berut12, Orlov12]. (Also, some important experiments regarding the connection of information and energy have been reported [Toyabe10].) These results indicate that the Landauer bound limits the minimum energy dissipation in modern CMOS-based computers [Keyes81, Lloyd00, Meindl00, Zhirnov03, Boechler10], which perform irreversible logic operations.

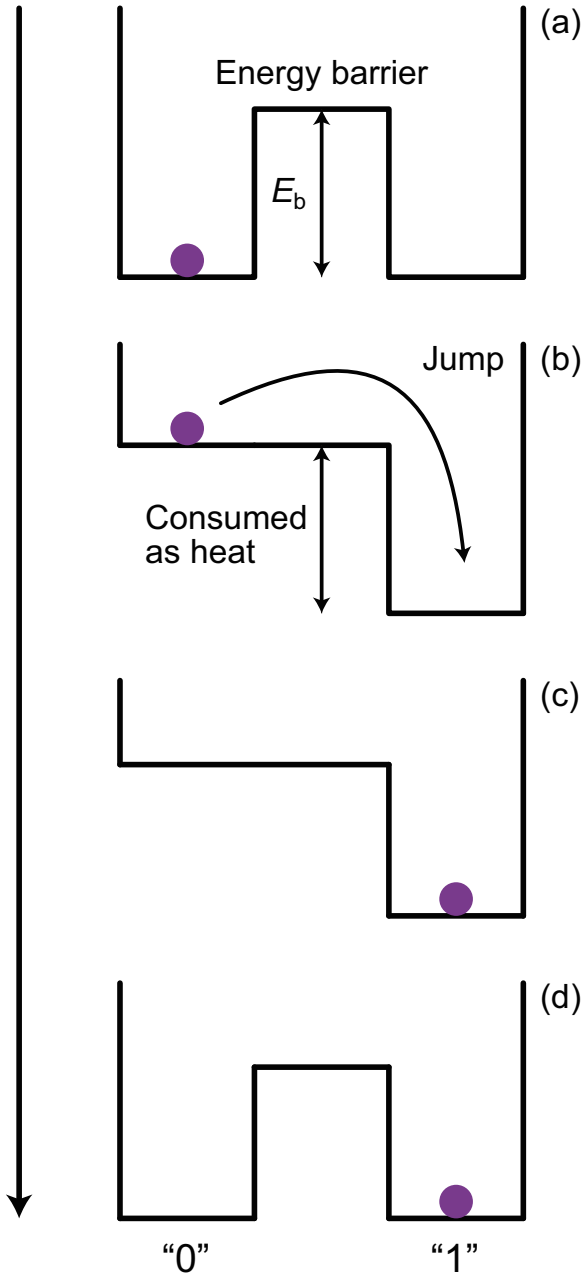


Figure 1.2: Time sequence of potential energy during a non-adiabatic switching operation.

1.2.2 Practical limits of non-adiabatic devices: CMOS and conventional superconductor logics

Whether the device is made of semiconductors or superconductors, the minimum energy bound of non-adiabatic devices is thermodynamically determined, because the switching energy almost corresponds to its energy barrier, E_b. In principle, the minimum switching energy of these devices corresponds to the Landauer bound of $k_BT\ln 2$. However, in practical usage, it must be much larger than k_BT in order to suppress the error caused by thermal noise: $\sim 10^6 k_BT$ for CMOS [Mukhopadhyay06] and $\sim 10^3 k_BT$ for conventional superconductor logics [Likharev91]. The difference between CMOS and superconductor logics mainly arises from the fact that in CMOS all the interconnects must be charged and discharged every time the gates switch, while in superconductor logics the passive transmission line (PTL) [Hashimoto03] networks achieve charge-free data movement. Also, static power consumption could significantly increase the minimum energy dissipation of these devices.

1.2.3 Adiabatic quantum-flux-parametron logic as an extremely energy-efficient device

In order to achieve lower energy bound, the adiabatic switching operation was proposed as a new switching principle [Keyes70]. Figure 1.3 shows the time sequence of the adiabatic switching. An adiabatic switching operation starts with a mono-stable state (Fig. 1.3a), which corresponds to an initial or null state. By applying a small gradient on this potential, the state gradually changes from the center to a lower position (Fig. 1.3b). Finally, the state reaches one of the two distinguishable states (Figs. 1.3c and d). Note that this process is physically reversible. According to this new principle, an adiabatic device can switch without irreversible state transition, which enables switching energy smaller than E_b. More important, in principle sub-k_BT bit energy (energy dissipation per bit) is achievable. In case the device is not logically reversible, the heat of more than the Landauer bound is generated to compensate the entropy [Likharev82], even in adiabatic logic.

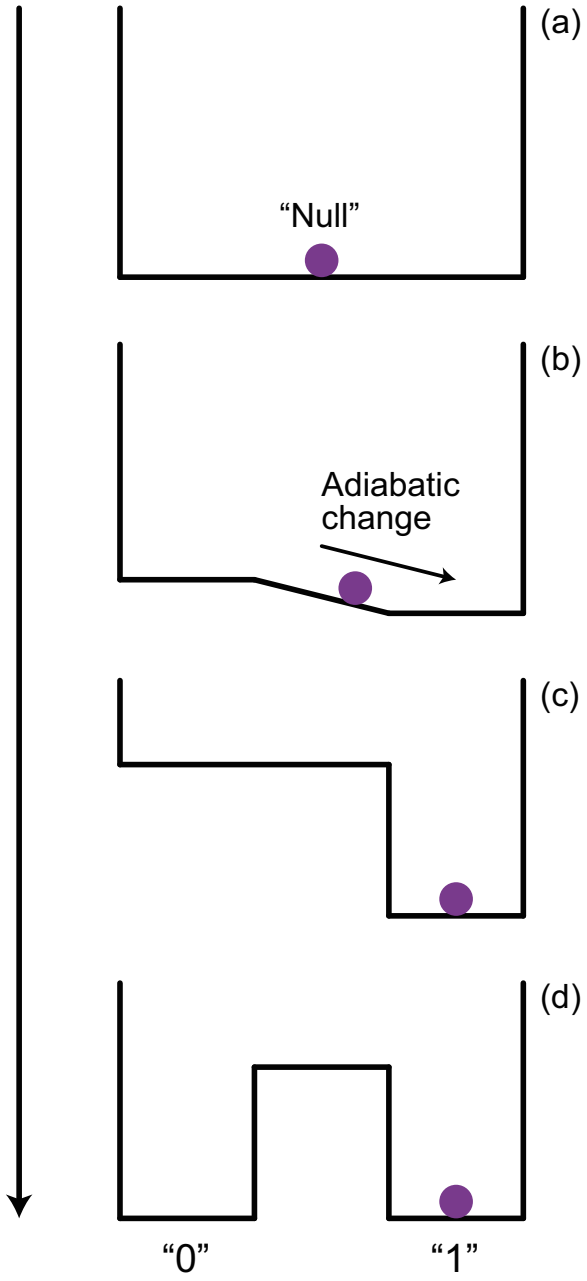


Figure 1.3: Time sequence of potential energy during an adiabatic switching operation.

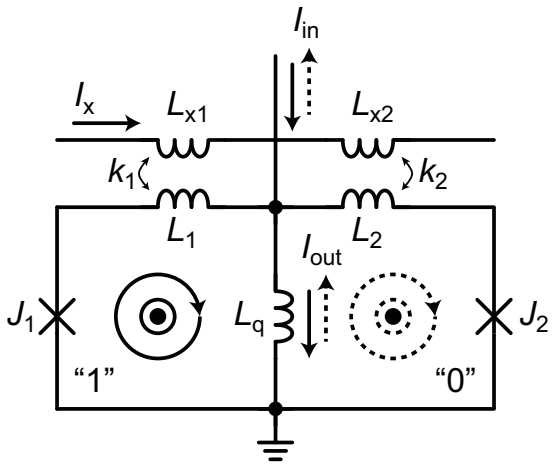


Figure 1.4: Circuit schematic of an AQFP gate.

Several adiabatic devices have been proposed so far, which include CMOS-based adiabatic circuits [Teichmann11], the parametric quantron [Likharev77], and the negative-inductance superconducting-quantum-interference-device (nSQUID) [Semenov03]. However, none of them have achieved sub-k_BT bit energy operations, and they are not practical for usage in a large-scale computing system.

As an extremely energy-efficient device, we herein propose the AQFP logic. Figure 1.4 shows the circuit schematic of an AQFP gate, which is composed of two rf-SQUIDs (see App. A) sharing an inductance, L_q. AQFP gates are based on quantum-flux-parametron (QFP) gates, which were invented by Eiichi Goto [Hosoya91, Hioe91]. In AQFP logic, the gates are designed to be in a fully adiabatic mode. The basic concept and fundamental experiments have been reported in [小澤 11, Takeuchi13a]. Detailed discussion on the relationship between circuit parameters and operation modes haven been reported in [Takeuchi13b], which will be also described in Chap. 2. By using an ac excitation current, I_x, the potential energy of an AQFP gate varies adiabatically from single-well to double-well during a switching event as shown in Fig. 1.3, where the gradient of the potential corresponds to the input current, I_{in}. Additionally, there is no static power consumption due to the ac biasing. As a result, the AQFP logic can achieve sub-k_BT bit energy, unless the entropy decreases.

Moreover, AQFP gates are highly robust against circuit parameter variations. One reason is that the current gain of an AQFP gate is very large because the state of the gate can gradually move with even a very small gradient (= small I_{in}). The other is that all the gates are clocked by the externally applied ac excitation current, I_x, which enables jitter-free logic operations. Thereby, extremely energy-efficient integrated circuits with high robustness can be realized by using AQFP logic.

1.3 Objective and outline

We have two objectives in this study. One is to reveal physical energy bounds on computation through investigation of the energy efficiency of AQFP logic. The other is to develop fundamental circuits necessary for energy-efficient computing systems using AQFP logic. The research outline of this study is shown in Fig. 1.5, below is the agenda.

1. Demonstration of sub-$I_c\Phi_0$ bit energy operations (in Chap. 2) - One of the most important advantages in an adiabatic device is that its switching energy can be much smaller than the energy barrier. We demonstrate it through both numerical analyses and experimental demonstrations, and we clearly show that AQFP gates operate in adiabatic modes.

2. Demonstration of sub-k_BT bit energy operations (in Chap. 3) - According to the Landauer's principle, there is no minimum thermodynamic energy bound for adiabatic switching operations in case the entropy does not reduce. We demonstrate it through numerical analyses, and we clearly show that AQFP gates can operate beyond the Landauer bound.

3. Building purely reversible logic gates using AQFP gates (in Chap. 4) - Reversible computing has never been demonstrated using practical devices, which remains an important but unsolved question in computer science. We build the purely reversible logic gate using AQFP gates, and we clearly show that there is no minimum energy bound for logic operations using purely reversible devices.

4. Proposal and design of novel energy-efficient latches (in Chap. 5) - In AQFO logic, latches are missing fundamental circuits. We propose a novel latch and discuss its energy efficiency. The development of AQFP logic circuits is under investigation by my colleague, Kenta Inoue [Inoue13, 井上 14].

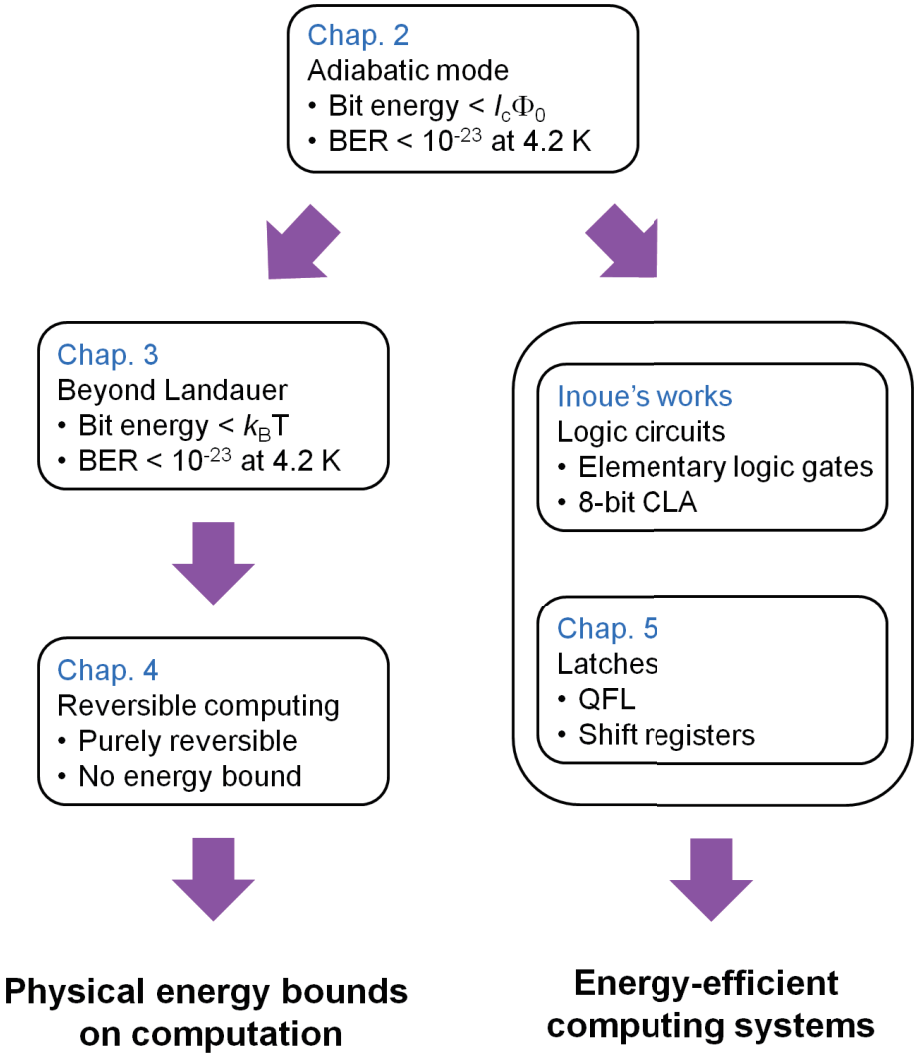


Figure 1.5: Research outline.

1.4 Superconductor logic

1.4.1 Historical overview

The history of superconducting digital electronics have been reported in [Van Duzer08, 早川 09, Likharev12, Fujimaki12]. There are also good textbooks which introduce the fundamental circuit properties and principles of them [Van Duzer98, Kadin99].

Superconductor logics have been being studied as promising post-semiconductor devices since late 1960s. The first superconductor logic was the voltage-state logic, where the logic is represented by the voltages across Josephson junctions. The project of IBM to develop the Josephson computer using voltage-state logic attracted significant attention, until it terminated in 1983. The reason for this termination was because of the intrinsic limitations in speed and power in voltage-state logic. The maximum operation frequency was $\sim$ GHz due to punchthrough, and its power consumption was $\sim 10 \cdot \mu$W/gate.

In late 1980s, a new superconductor logic, the rapid single-flux-quantum (RSFQ) logic [Mukhanov87, Likharev91] was proposed by the Russian research group. In RSFQ, the logic state is represented by the presence or the absence of an SFQ in a SQUID loop (see App. A). While in voltage-state logic Josephson junctions must be underdamped to sustain the voltage state, the critically damped junctions are used in RSFQ, which enables data propagation along with extremely narrow SFQ pulses of $\sim$ ps width (see App. C and D). The experimental demonstration of a 770 GHz frequency divider was reported in [Chen98, Chen99]. No other devices have achieved such an extremely fast operation frequency. Also, its power consumption is only $\sim$ nW/gate, which is much smaller than that of the voltage-state logic. After intense research projects mainly in the US and Japan since late 1990s, vast amounts of RSFQ digital circuits have been reported: the optical-electrical-SFQ hybrid switching system [Yorozu01], the FLUX microprocessors [Dorojevets01, Bunyk03], the CORE microprocessors [Tanaka04, Fujimaki08], superconductor analog-to-digital converters [Mukhanov04].

1.4.2 Advancement of energy efficiency

Although many digital RSFQ circuits have been successfully demonstrated, it is still difficult to justify the development of practical computers using superconductor logics, because of the continuous improvement of energy efficiency in CMOS logic. The practical minimum bit energy in CMOS logic is $\sim 10^6 k_B T \sim 10^{-15}$ J at 300K. That of RSFQ is, in principle, $\sim 10^3 k_B T \sim 10^{-19}$ J at 4.2K. However, by adding static power consumption, it increases to $\sim 10^{-18}$ J. Finally, it reaches $\sim 10^{-15}$ J by adding power consumption of a cryocooler (1000 W/W) [Radebaugh09].

In order to achieve extremely high energy efficiency in comparison with CMOS

logic, some new energy-efficient superconductor logics were proposed and are under drastic investigations. Thanks to the new US government project, Cryogenic Computing Complexity (C3) project [C3], much more attention is attracted to this field [Holmes13]. Below we introduce several energy-efficient superconductor logics, after pointing out the problems on power consumption in RSFQ.

Power consumption in RSFQ logic The nature of superconductors, zero resistance, is well suitable for energy-efficient logic devices. This is because in CMOS logic power consumption and operation frequencies are limited by *RC* time constants. The main problem of RSFQ logic is that its static power consumption is much larger than dynamic power consumption. Figure 1.6 shows the schematic of Josephson-transmission-lines (JTLs) in RSFQ logic, where an SFQ propagates by use of 2π phase transition of each junction. The dynamic power consumption, P_d, arises from switching energy of Josephson junctions, E_{sw}, which are represented as below, respectively:

$$\begin{aligned} E_{sw} &= \int IV\mathrm{d}t \sim I_c \frac{\Phi_0}{2\pi} \int_0^{2\pi} \mathrm{d}\theta \\ &= I_c \Phi_0, \end{aligned} \tag{1.1}$$

$$P_d = E_{sw} f = I_c \Phi_0 f, \tag{1.2}$$

where I_c is a critical current, f is an operation frequency. In order to suppress the error caused by thermal noise, I_c is often designed to be larger than $100\,\mu$A, resulting in the average I_c of $\sim 200\,\mu$A. Therefore, $E_{sw} \sim 0.4\,\mathrm{aJ} \sim 7000 k_B T$, $P_d \sim 20\,\mathrm{nW}$ for an operation frequency of 50 GHz. In contrast, the static power consumption arises from the bias resistance, R_b, which is necessary to provide bias currents, I_b, to each junction stably. In order to suppress the pulse interactions, bias voltage, V_b, must be much larger than that of SFQ pulses [Tanaka12]. If we assume that $V_b \sim R_b I_b$, $I_b \sim 0.8 I_c$, and an activity factor, $\alpha = 0.5$, the static power consumption, P_s, and the bit energy, E_{bit}, are given as below:

$$P_s = R_b I_b^2 \sim 0.8 I_c V_b, \tag{1.3}$$

$$\begin{aligned} E_{bit} &= \alpha E_{sw} + P_s / f \\ &\sim 0.5 I_c \Phi_0 + 0.8 I_c V_b / f. \end{aligned} \tag{1.4}$$

As a result, $E_{bit} \sim 8.2\,\mathrm{aJ} \sim 1.4 \times 10^5 k_B T$ at 4.2 K and $P_d + P_s \sim 420\,\mathrm{nW}$, where it is clear that static power consumption dominates in the total power consumption ($P_s/P_d \sim 20$). This means that in RSFQ logic the nature of superconductors is not fully utilized, because of the resistor networks for stable bias currents.

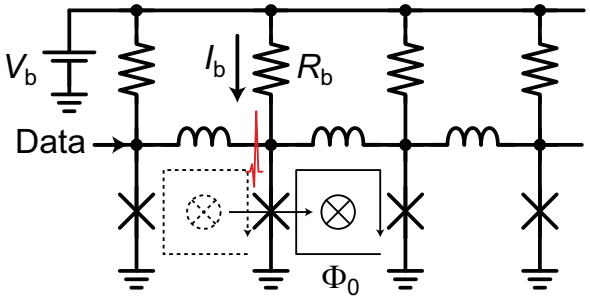


Figure 1.6: Circuit schematic of RSFQ JTLs.

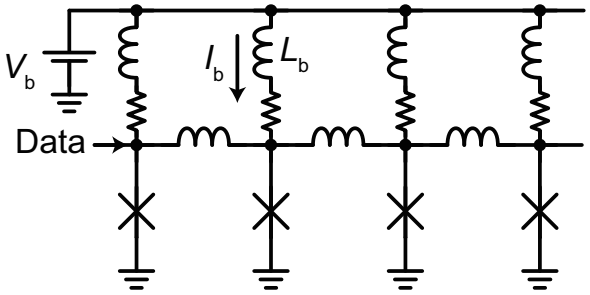


Figure 1.7: Circuit schematic of *LR*-biased RSFQ logic.

***LR*-biased RSFQ logic** A straightforward way to reduce power consumption in RSFQ logic is to reduce R_b. However, as R_b reduces, I_b changes significantly while switching and local redistribution of bias currents occurs, which results in a larger pulse interaction. In order to reduce the interaction, in *LR*-biased RSFQ logic (Fig. 1.7), large inductances, L_b, are inserted between bias resistances and power buses, where large *LR* time constants keep the bias currents while switching. Several numerical and experimental demonstrations on this approach have been reported [Yoshikawa99, Yamanashi07, Ortlepp11]. However, no demonstration of large-scale circuits using *LR*-biased RSFQ logic has been reported yet. This is because L_b requires large circuit area, and *LR*-biasing cannot prevent the redistribution of bias currents.

ERSFQ/eSFQ logic Another approach to reduce the interaction is to utilize the periodic 2π phase transition of Josephson junctions. First, this approach was adopted in the Polonsky's dual-rail scheme [Polonsky99]. However, the hardware overheads were too high for practical usage.

In energy-efficient RSFQ (ERSFQ and eSFQ) logics [Mukhanov11, Kirichenko11, Volkmann13a], the specific nodes in circuits experience 2π phase transition at every clock cycle, which prevents the redistribution of bias currents. In Fig. 1.8, the nodes

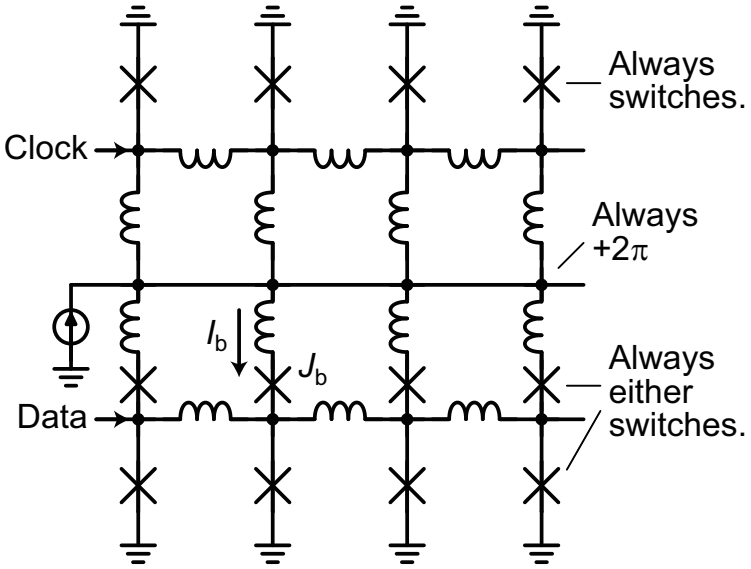


Figure 1.8: Circuit schematic of ERSFQ logic.

in the power buss experience 2π phase transition at every clock cycle. The bit energy of ERSFQ and eSFQ are $2I_c\Phi_0$ and $1.1I_c\Phi_0$ [Mukhanov11], respectively. Moreover, in principle, it is possible to achieve zero static power consumption by disabling clock signals. The experimental demonstration of eSFQ 184-bit shift registers was reported in [Volkmann13b]. Additionally, the investigation to utilize ERSFQ logic in asynchronous ALUs was reported in [Ayala13].

RQL In reciprocal-quantum-logic (RQL) [Herr11], flux biases are provided through transformers as shown in Fig. 1.9, which enables zero static power consumption. The transformers physically separate bias networks and logic circuits, therefore the redistribution of bias currents does not occur. Also, serial biasing using transformers is suitable to achieve large-scale circuits, whereas in RSFQ logic a large amount of bias currents, which are provided in parallel to each gate, could prevent correct operations [Terai03, Ehara13]. In RQL, data is encoded using pairs of an SFQ ($+\Phi_0$) and its reciprocal one ($-\Phi_0$), which prevents SFQs from accumulating in the bias inductance in the transformer, L_b. Additionally, four-phase ac bias currents are used to prevent jitter accumulation and timing variation [Terai04, Fung13]. In order to distribute the high-frequency ac bias currents, superconducting microwave power dividers were developed [Oberg11]. From measurement results, the bit energy was estimated to be $0.33I_c\Phi_0$ at 6 GHz, which indicates that RQL gates operate in partially adiabatic modes thanks to the ac biasing. An 8-bit carry look-ahead adder with 510 nW at 6.2 GHz was successfully demonstrated [Herr13], where superconductor distributed

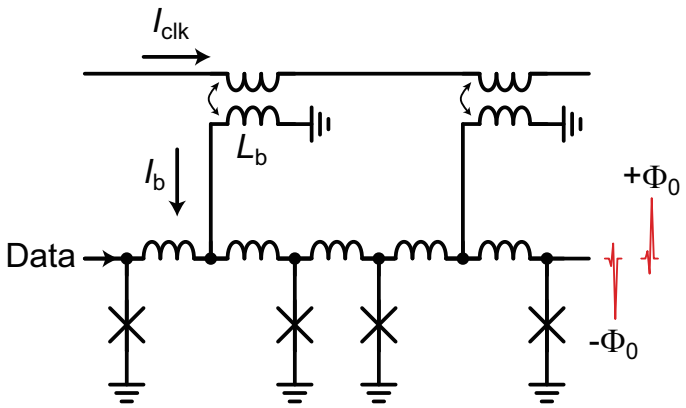


Figure 1.9: Circuit schematic of RQL.

amplifiers [Herr10] were used for the high-speed test.

LV-RSFQ logic The low-voltage RSFQ (LVRSFQ) logic utilizes extremely low bias voltages. While constant bias currents give the constant torque to the phase between a junction (constant-current mode) in conventional superconductor logics, the low bias voltage rotates the phase at constant speed (constant-voltage mode) in LV-RSFQ. The experimental demonstration of LV-RSFQ 8-bit shift registers with 4.0 aJ/bit at 18 GHz using $V_b = 0.1\,\mathrm{mV}$ has been reported [Tanaka12]. As another approach to reduce the power consumption, miniaturization of I_c is also under investigation [Tanaka13].

AQFP logic As described earlier, the AQFP logic is based on the QFP logic. From late 80s to early 90s, lots of research results on QFP-based computers were reported. These include a memory cell [Harada87], A/D converters [Shimizu89, Harada92], shift registers [Casas91, Casas92, Hosoya95], a race arbiter [Lee91], minimum energy bounds [Goto91], noise analyses [Ko92, Ruby93], margin analyses [Hosoya93], and a bit-slice ALU [Hioe95]. In AQFP logic, QFP gates are designed to operate in adiabatic modes in order to reduce energy dissipation.

Here we clearly show the advantages and disadvantages of the AQFP logic in comparison with other energy-efficient logics. The most important point in AQFP is that it is strongly focused on reducing the intrinsic energy dissipation for switching, whereas other logics focus on reducing the static power consumption. Below are the advantages:

- Extremely small bit energy - The switching energy of an AQFP gate can be much smaller than $I_c\Phi_0$, while that of other logics is $\sim I_c\Phi_0$. Additionally, the static power consumption is zero.

- Large current gain - Even a very small input current can push the potential towards one of the logic states.
- Zero timing jitter - All the AQFP gates are clocked by the externally applied ac excitation currents.
- High robustness - AQFP gates are highly robust against global parameter variations, because of the large current gain and zero timing jitter.
- Serial biasing - Excitation currents are serially provided to each gate, therefore the amount of applied currents does not increase if the number of gates increases.
- Reduction in critical currents - Critical currents of the junctions can be significantly reduced while keeping bit error rates very low, which enables a further reduction in energy dissipation. This is because junctions are not critically biased unlike conventional superconductor logics.

Below are the disadvantages:

- Large latency - Each AQFP gate can conduct only one logic operation in one clock cycle.
- Difficulty to hold data - All gates are reset at every clock cycle because of the ac excitation. However, this can be solved by introducing novel latches, as will be described in Chap. 5.

1.5 Reversible computing

In order to go beyond the Landauer bound, Edward Fredkin established the theory of reversible computing [Fredkin82], where the entropy of information is conserved during computation to prevent the heat generation resulting from the entropy reduction. He introduced the Fredkin Gate as a 3-in/3-out reversible logic gate, which serves like a 2×2 switch with an additional control signal. A Fredkin gate is logically reversible because its inputs are uniquely determined from its outputs, thereby conserving the entropy during computation. The history and recent progresses on reversible computing have been reported in [Leff02, Cockshott12, 森田 12].

As part of the effort to achieve practical reversible logic gates, several physical models and devices have been proposed. These include the coupled-potential-well model [Keyes70], the billiard ball model [Fredkin82], the parametric quantron, and the nSQUID. Although an experimental demonstration of nSQUID shift registers has been reported [Ren11], no reversible logic operations have been experimentally demonstrated to date. Thus, discussions on reversible computing remain theoretical, and the

question as to whether reversible computing is achievable using practical logic devices has yet to be resolved.

One of the problems is that an extremely energy-efficient logic device is first necessary, because the energy dissipated by the erasure of information is of the order of k_BT. The bit energy of conventional logic devices, including CMOS and energy-efficient superconductor logics, is at least larger than $\sim 1,000 k_BT$, which is too large to permit their use as reversible logic gates. In contrast, the AQFP logic is a good candidate for use as a building block of reversible logic gates because its bit energy can go below k_BT due to adiabatic switching operations.

Chapter 2

Sub-$I_c\Phi_0$ bit-energy operation

The most important advantage of AQFP gates is that their switching energy can be much smaller than the energy barrier of the system, or $I_c\Phi_0$. In this chapter, we focus on demonstrating the sub-$I_c\Phi_0$ bit-energy operation of AQFP gates through both simulation and measurement. First, we investigate the impacts of circuit parameters on energy dissipation and bias margins, and we optimize them. Through circuit simulation, we show that the bit energy of the optimized AQFP gate is much smaller than $I_c\Phi_0$. We calculate the bit error rate of the gate to confirm if the gate can operate with such a small bit energy at finite temperature. Finally, we measure the bit energy of the gate using a superconducting resonator-based method [Oates91, Chin92, Wallraff04, Lupascu07] and experimentally show the sub-$I_c\Phi_0$ bit-energy operation. The results obtained in this chapter have been reported in [Takeuchi13b, Takeuchi13c].

2.1 Adiabatic switching operation

Figure 2.1 shows the circuit schematic of an AQFP gate, which is composed of two superconducting loops with Josephson junctions, J_1 and J_2, the phase differences of which are ϕ_1 and ϕ_2, respectively, and inductances, L_1, L_2, and L_q. In the figure, I_{in} is an input current, and I_{out} is an output current. In addition, I_x is an excitation current or an ac bias current. The operation principle of an AQFP gate is based on that of a QFP gate. Here, I_x is applied to L_{x1} and L_{x2}, which are magnetically coupled with L_1 and L_2, respectively by the coupling coefficients k_1 and k_2. The parameters of an AQFP gate are often symmetric; $L_1 = L_2 = L$, $L_{x1} = L_{x2} = L_x$, and $k_1 = k_2 = k$. The excitation flux, $k(LL_x)^{1/2}I_x = MI_x$, is applied to each loop, and the direction of I_{in} decides in which loop an SFQ is stored, where the circuit state is "0" when an SFQ is stored in the left loop and is "1" when an SFQ is stored in the right loop. We can determine the circuit state based on the direction of I_{out}.

We use a trapezoidal or sine profile for I_x to change the circuit potential slowly or

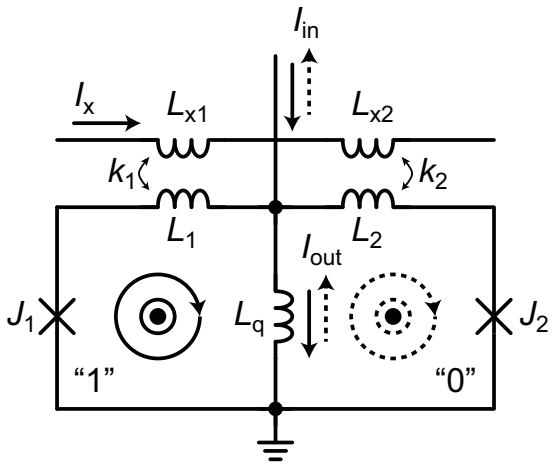


Figure 2.1: Circuit schematic of an AQFP gate.

adiabatically. The potential of a QFP gate, U_{qfp}, is given as follows [Ko92]:

$$U_{qfp} = E_j \left[\frac{(\phi_x - \phi_-)^2}{\beta_L} + \frac{(\phi_{in} - \phi_+)^2}{\beta_L + 2\beta_q} - 2\cos\phi_- \cos\phi_+ \right], \tag{2.1}$$

where $E_j = I_c\Phi_0/2\pi$ is Josephson energy, $\phi_x = 2\pi M I_x/\Phi_0$, $\phi_{in} = 2\pi L_q I_{in}/\Phi_0$, $\phi_- = (\phi_1 - \phi_2)/2$, $\phi_+ = (\phi_1 + \phi_2)/2$, $\beta_L = 2\pi L I_c/\Phi_0$, and $\beta_q = 2\pi L_q I_c/\Phi_0$. Figure 2.2 shows the adiabatic potential change while switching from "0" to "1" using Eq. (2.1) with $\beta_L = 0.2$, $\beta_q = 1.6$, and $|I_{in}/I_c| = 0.3$. We assumed that $\phi_- = \phi_x$, which is a natural restriction to minimize U_{qfp} because the denominator of the first term of Eq. (2.1) is often much smaller than that of the second term of Eq. (2.1). When I_x returns to zero, the circuit state returns to the "initial" state with a single-well potential. Moreover, if I_x is activated again, the circuit is excited to "0" or "1" with a double-well potential. In the mechanical analogy for the gate, the particle is in the potential minimum in Fig. 2.2 during the change of the circuit state. Therefore, the particle has little kinetic energy while switching, which is dissipated as heat by the friction on the potential surface. As the rise/fall time of excitation currents increases, the potential moves more slowly and the kinetic energy decreases. Thus, the gate dissipates even less energy. This is why the AQFP gate can decrease its bit energy to less than $I_c\Phi_0$.

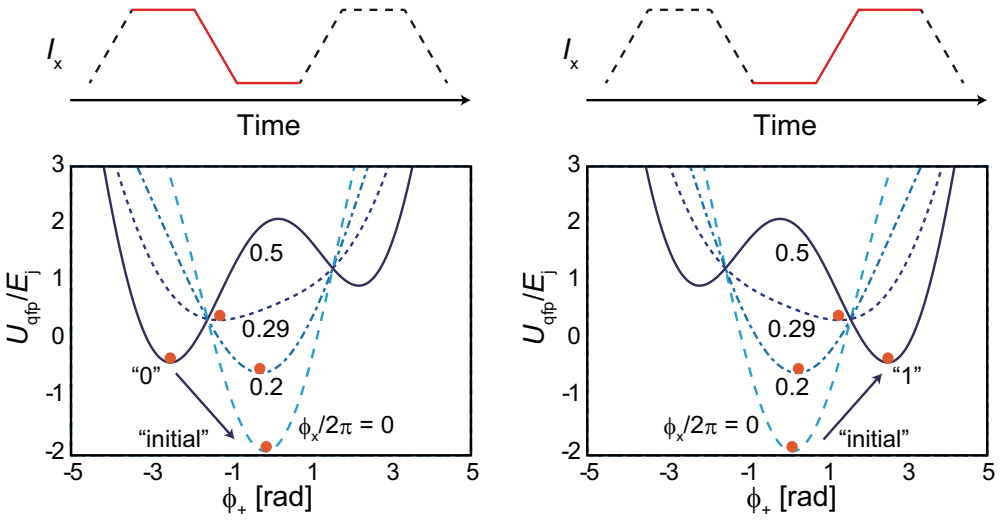


Figure 2.2: Potential change while switching from "0" to "1" with $\beta_L = 0.2$, $\beta_q = 1.6$, and $|I_{in}| = 0.1I_c$.

2.2 Optimization of circuit parameters

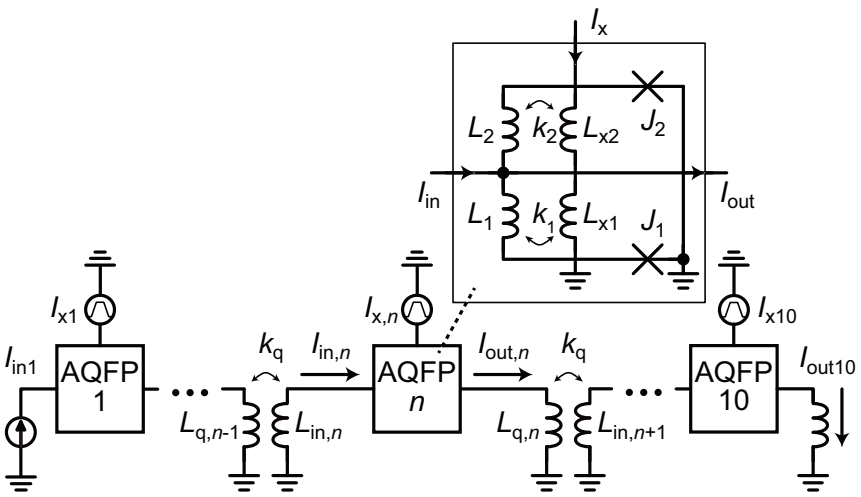
2.2.1 Impacts of β_L and β_q

We optimize β_L and β_q in terms of dynamic energy dissipation and operation margins, because β_L and β_q define how the potential changes during a switching event. However, we need to decide in which system we evaluate an AQFP gate for the optimization, because AQFP gates have energy interactions. Figure 2.3a is the schematic diagram that we used to investigate energy interactions. Ten AQFP gates with the same circuit parameters are connected in series, where the input inductance of the n-th gate, $L_{in,n}$, is magnetically coupled with the output inductance of the $(n-1)$-th gate, $L_{q,n-1}$, by the coupling coefficient, k_q. When the excitation current, $I_{x,n}$, is activated, the gate is excited to "0" or "1" generating an output current, $I_{out,n}$. We activated each excitation current in turn and calculated the bit energy per switching event of each gate by integrating excitation currents and voltages over time using the Josephson-circuit simulator, JSIM [Fang89].

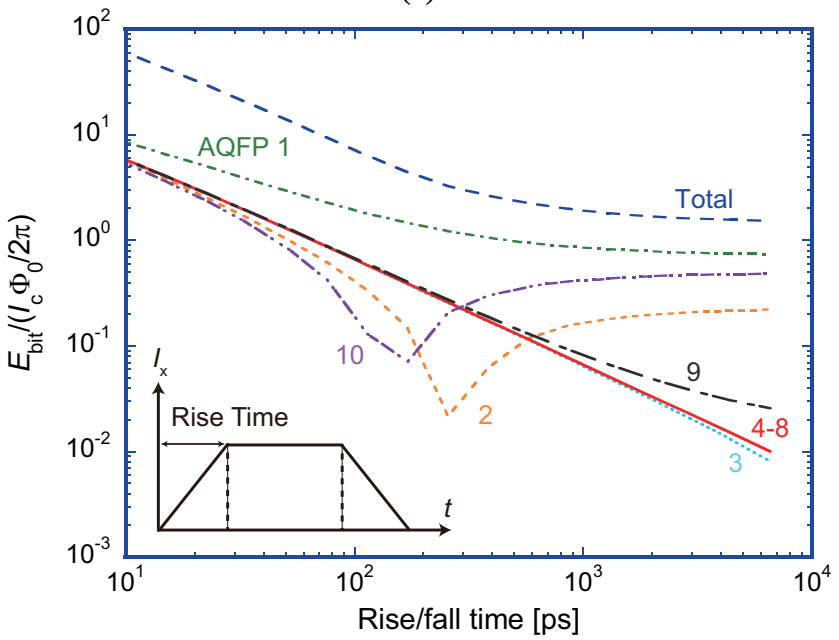
Figure 2.3b shows the simulation results for the bit energy, E_{bit}, of each AQFP gate with $L_{in,n} = L_{q,n}$, $\beta_L = 0.1$, $\beta_q = 1.6$, $k_q = 0.3$, $I_{in1} = 0.1I_c$, and $\phi_x/2\pi = 0.5$. We assumed the use of the Nb Josephson process, the ISTEC standard process (STP2) [Nagasawa95] and assumed the density of critical currents to be 2.5 kA/cm^2. All the junctions in the AQFP gates were critically damped by using shunt resistors so that their McCumber parameter [McCumber68, Stewart68], β_c, becomes 0.89 for high-speed operations (see App. C), which is a typical value for our RSFQ design

using STP2. As mentioned earlier, E_{bit} is supposed to decrease as the rise/fall time of I_x increases. However, the bit energy of the first, second, and tenth gates behave differently because the balance between the energy supplied by the previous gate and that applied to the next gate is complicated near the edge of cascaded AQFP gates. Therefore, several gates are required before and after the gate for which the parameters are optimized. The figure shows that the bit energy of the fourth through eighth gates of ten AQFP gates connected in series behave in the same manner, which means that the supplied and applied energy are balanced in these gates. Moreover, at least three gates are necessary before the optimized gate, and at least two gates are necessary after the optimized gate. Therefore, in this chapter, we decided to use six AQFP gates, which have the same circuit parameters and are connected in series, and we evaluated the fourth gate for calculating bit energy, bias margins, and BERs, as will be described later herein.

Figure 2.4a shows the bit energy as a function of β_L and β_q with $L_{in,n} = L_{q,n}$, $k_q = 0.3$, $I_{in1} = 0.1I_c$, and a rise/fall time of 100 ps. The figure indicates that both β_L and β_q should be decreased in terms of energy dissipation. Figure 2.4b shows the bias margin for the excitation current as a function of β_L and β_q, where a bias of 0% corresponds to $\phi_x/2\pi = 0.5$. This indicates that β_L should be decreased, whereas β_q should be increased, in terms of operation margins. Therefore, β_L should decrease with respect to both energy dissipation and operation margins, whereas β_q exhibits a tradeoff relationship between energy dissipation and operation margins. Here, we define the minimum β_L to be 0.2 based on the restriction of practical layout, and the operation margin should be wider than ±25% so that the gates have robustness against circuit parameter dispersions. As a result, we set the optimized (β_L, β_q) to (0.2, 1.6) with $E_{bit} = 0.12I_c\Phi_0$ and a bias margin of ±26% for a rise/fall time of 100 ps.

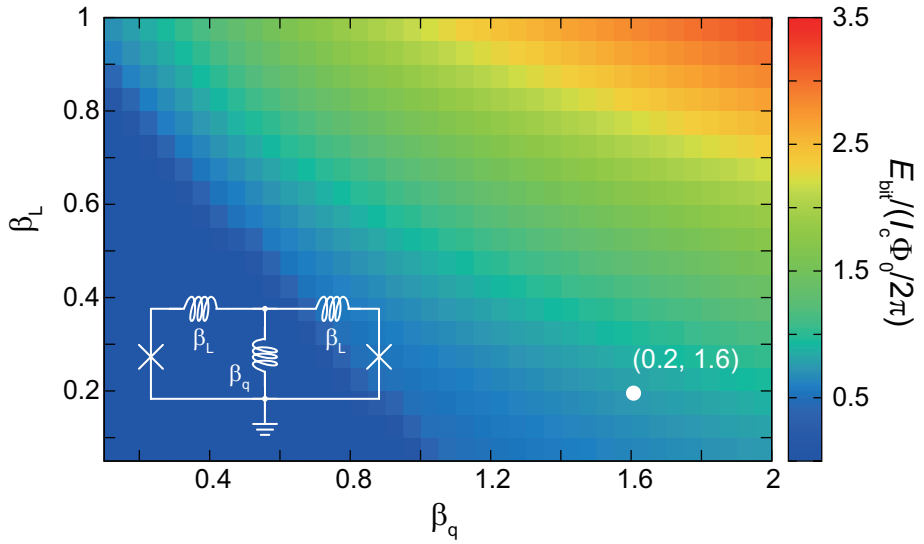


(a)

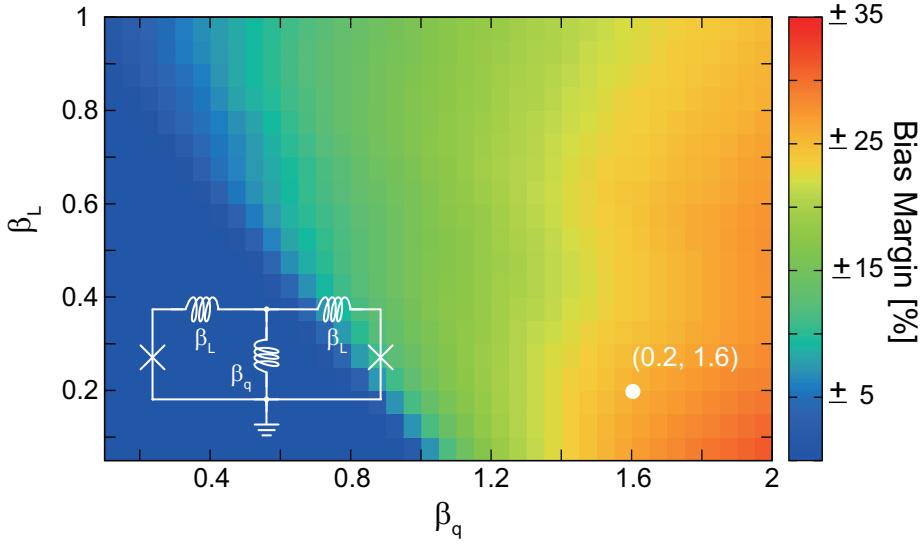


(b)

Figure 2.3: Energy interactions between AQFP gates. (a) Schematic diagram for evaluating interactions. Ten AQFP gates with the same parameters are connected in series. (b) Simulation results for the bit energy of each gate. The fourth through eighth gates exhibit linearity of the bit energy with respect to the rise/fall time of excitation currents. $\beta_c = 0.89$, $L_{in,n} = L_{q,n}$, $\beta_L = 0.1$, $\beta_q = 1.6$, $k_q = 0.3$, $I_{in1} = 0.1I_c$, and $\phi_x/2\pi = 0.5$.



(a)



(b)

Figure 2.4: Parameter mapping with $\beta_c = 0.89$, $L_{in,n} = L_{q,n}$, $k_q = 0.3$, and $I_{in1} = 0.1I_c$, and a rise/fall time of 100 ps. (a) Bit energy as a function of β_L and β_q. (b) Bias margin as a function of β_L and β_q.

2.2.2 Simulation of bit energy

Figure 2.5 shows the transient analysis of the optimized gates. The upper three plots show the excitation currents for the third through fifth gates, respectively. The middle three plots and the lower three plots show the input currents and output currents for these three respective gates. The figure shows the correct operation with the optimized gates, where each gate generates an output current after each excitation current is activated. Figure 2.6 shows the bit energy versus the rise/fall time of excitation currents. For the optimized gate with $(\beta_L, \beta_q) = (0.2, 1.6)$, E_{bit} decreases approximately linearly with a rise/fall time, while the non-optimized gate with (0.8, 2.0) does not exhibit such linearity. Moreover, E_{bit} of (0.2, 1.2) is slightly smaller than that of (0.2, 1.6), but its bias margin is much narrower than that of (0.2, 1.6), as shown in Fig. 2.4b. Therefore, we can consider (0.2, 1.6) to be valid as optimized parameters. If we assume that $I_c = 50\,\mu$A and the rise/fall time is 200 ps with the optimized gate, $E_{bit} = 6.40 \times 10^{-21}$ J $= 0.06 I_c \Phi_0 = 110 k_B T$ for 4.2 K. Moreover, unlike RSFQ circuits, AQFP gates do not require a dc bias current, so their static energy dissipation is zero, which implies that both static and dynamic energy dissipation are quite small in AQFP logic.

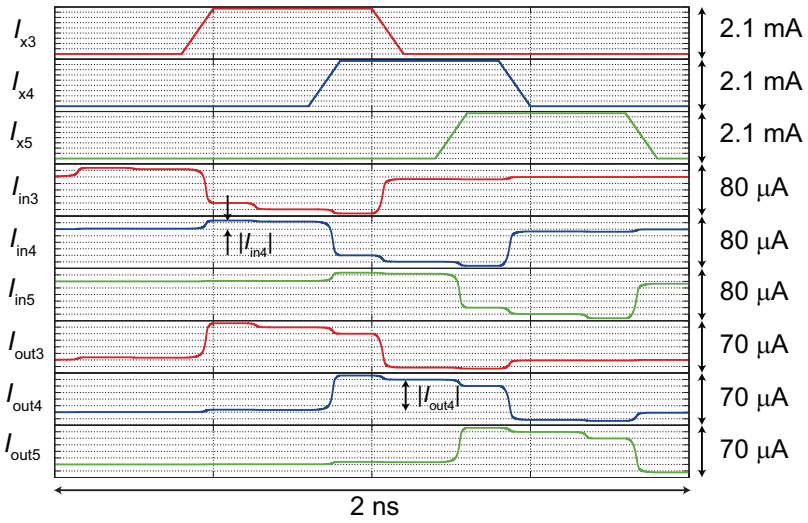


Figure 2.5: Transient analysis of the third through fifth gates for a rise/fall time of 100 ps. The excitation currents are activated in turn, and the output currents are also generated in turn, propagating one-bit information.

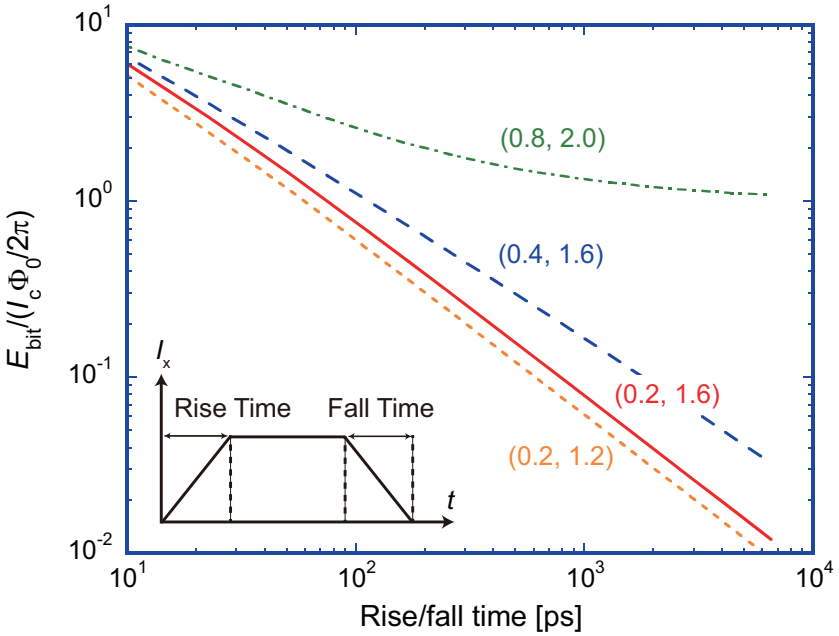


Figure 2.6: Bit energy versus rise/fall time of excitation currents. $\beta_c = 0.89$, $L_{in,n} = L_{q,n}$, $k_q = 0.3$, and $I_{in1} = 0.1I_c$, and $\phi_x/2\pi = 0.5$. The optimized gate with $(\beta_L, \beta_q) = (0.2, 1.6)$ indicates that E_{bit} decreases almost linearly with a rise/fall time of excitation currents.

2.3 Simulation of bit error rate

Since the bit energy of an AQFP gate approaches k_BT, we need to confirm the robustness of the gate against thermal noise. We calculated the BER of the optimized gate with a rise/fall time of 200 ps using WRspice [Whiteley91, WR], which takes thermal noise into account using the Monte Carlo method. Here, correct operation means that the gate switches to the correct state and the output gain is larger than 1, or $I_{out4} \times I_{in4} > 0$ and $|I_{out4}| > |I_{in4}|$, when excited. Figure 2.7 shows the simulation results for the BER for temperatures of 4.2 K, 12 K, and 20 K in order to confirm the relationship between E_{bit}/k_BT and the BER. The plots show the simulation results, and the lines show the fitting curves obtained using a complimentary error function, erfc. Table I shows the BER after fitting, where Π_H is the BER of the higher bias regions and Π_L is the BER of the lower bias regions. The bias margin is defined as the bias region in which the BER is smaller than 1.0×10^{-23}, which indicates that an error occurs during several years in a large computing system, assuming 5 GHz operation with 10^5 gates. For $E_{bit}/k_BT = 110$ at 4.2 K the optimized AQFP gate has a very wide margin of ±19.4%, and even for $E_{bit}/k_BT = 23.2$ at 20 K the gate still has a wide margin of ±8.8%.

If the switching event is non-adiabatic like CMOS and RSFQ, the BER, Π, is given by (see Chap. 1): $\Pi = \exp(-E_{bit}/k_BT)$, where the energy barrier between the two states ("0" and "1") is assumed to be equal to the bit energy. When $E_{bit}/k_BT = 23.2$, its BER becomes 8.4×10^{-11}. This is because a non-adiabatic gate consumes as much energy as the energy barrier in a switching event, whereas an adiabatic gate consumes much less energy than the energy barrier because its potential varies gradually between single and double potential wells, as shown in Fig. 2.2.

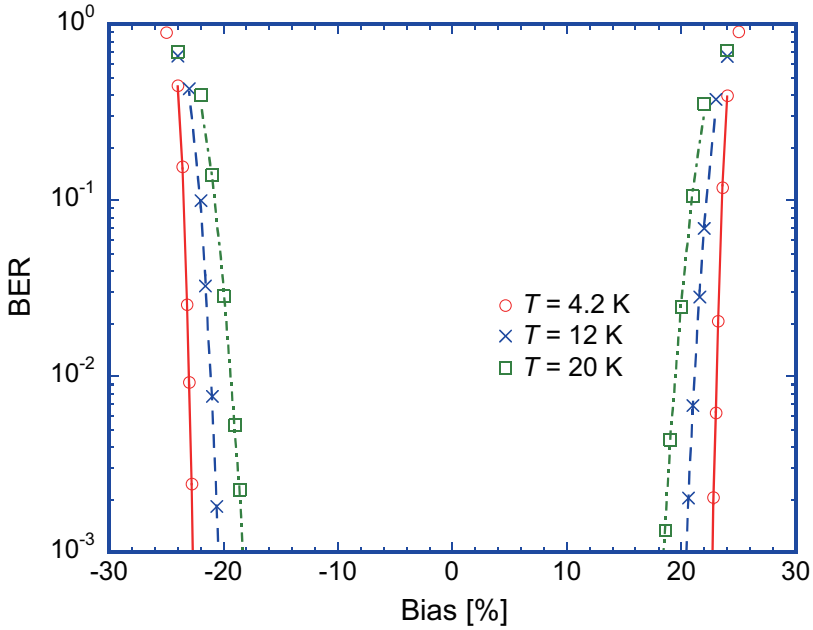


Figure 2.7: BER of the optimized gate. Here, $\beta_L = 0.2$, $\beta_q = 1.6$, $I_c = 50\,\mu$A ($\beta_c = 0.89$), $L_{in,n} = L_{q,n}$, $k_q = 0.3$, $I_{in1} = 0.1I_c$, and the rise/fall time is 200 ps. The number of iterations for each BER is 10,000. A bias of 0% corresponds to $\phi_x/2\pi = 0.5$.

Table 2.1: BER and bias margin versus bit energy

T[K]	E_{bit}/k_BT	BER	Bias margin
4.2	110	$\Pi_H = 0.5 \times \mathrm{erfc}[(0.621 - 2\pi\phi_x)/0.00330]$, $\Pi_L = 0.5 \times \mathrm{erfc}[(2\pi\phi_x - 0.380)/0.00317]$	±19.4%
12	38.6	$\Pi_H = 0.5 \times \mathrm{erfc}[(0.617 - 2\pi\phi_x)/0.00696]$, $\Pi_L = 0.5 \times \mathrm{erfc}[(2\pi\phi_x - 0.384)/0.00630]$	±13.8%
20	23.2	$\Pi_H = 0.5 \times \mathrm{erfc}[(0.613 - 2\pi\phi_x)/0.00954]$, $\Pi_L = 0.5 \times \mathrm{erfc}[(2\pi\phi_x - 0.387)/0.00973]$	±8.8%

2.4 Measurement of bit energy

2.4.1 Superconducting resonator-based method

Superconducting resonators are used to measure the small resistances of superconducting strips [Oates91, Chin92]. This is because a superconducting resonator can have quite a high external Q, which transforms the impedances of external loads to much lower impedances, due to its extremely high unloaded Q. This also means that the very small power consumption of AQFP gates can be measured by coupling the gate with a superconducting resonator. Figure 2.8a shows the schematic of the circuit used to measure the power consumption of an AQFP gate, where the gate is magnetically coupled with a superconducting resonator composed of L and C. R_g is the impedance of external loads ($= 50\,\Omega$), Q_{es} is the Q between each port and the resonator, V is the voltage of a power supply, and it is assumed that the resonator has no resistance because it is superconductive.

The resonator supplies power to the AQFP gate for switching, which appears as small losses in the resonator. Therefore, Fig. 2.8a can be transformed to Fig. 2.8b, where the AQFP gate is simply expressed as a small resistance in the resonator, r. In addition, the magnetic couplings between the resonator and the ports function as impedance invertors, so that R_g and V are converted to equivalent elements, Z_K and V_K. The power consumption caused by r, P_u, is given by:

$$Q_u = \omega_0 \frac{W}{P_u}, \tag{2.2}$$

where Q_u is the internal Q, ω_0 is the resonant angular frequency, and W is the energy stored in the resonator per second. Similarly, the power consumption of the external loads, P_e, is given by $Q_e = \omega_0 W/P_e$, where Q_e ($= Q_{es}/2$) is the external Q. By combining these equations, P_u is given by:

$$P_u = P_e \frac{Q_e}{Q_u}. \tag{2.3}$$

Equation (2.3) shows that P_u can be calculated using P_e, Q_u, and Q_e; however, P_u cannot be measured directly using a network analyzer. Therefore, Eq. (2.3) is transformed to calculate P_u using scattering parameters, which can be easily measured using a network analyzer.

At the resonant frequency, the current in the resonator, I_0, is expressed as $I_0 = V_K/(2Z_K + r)$. Therefore, P_e is given by:

$$P_e = \frac{1}{2} \cdot 2Z_K \cdot I_0^2 = \frac{1}{2} \cdot \left(\frac{2Z_K}{2Z_K + r} \right)^2 \cdot \frac{V_K^2}{2Z_K}. \tag{2.4}$$

Here, $V_K^2/2Z_K$ corresponds to the input power from the power supply, P_{in}. $2Z_K/(2Z_K + r)$ is equal to the insertion loss, S_{21}, and it can be also expressed using Q_u and Q_e:

$$\frac{2Z_K}{2Z_K + r} = \frac{Q_e^{-1}}{Q_e^{-1} + Q_u^{-1}}. \tag{2.5}$$

Therefore, the relation between Q_u, Q_e, and S_{21} is given by:

$$\frac{Q_e}{Q_u} = \frac{1}{S_{21}} - 1. \tag{2.6}$$

From Eqs. (2.3), (2.4), and (2.6), P_u is given by:

$$P_u = \frac{P_{in}}{2} S_{21}(1 - S_{21}), \tag{2.7}$$

which shows that the power consumption of the AQFP gate can be calculated by measuring S_{21}. Moreover, Eq. (2.6) indicates that S_{21} can be measured with high accuracy by increasing Q_e because S_{21} decreases as Q_e increases. A high Q_e is available due to the extremely high Q of superconducting resonators.

In the actual measurement system, there are losses in the resonator, probes, and cables. Therefore, the resistance, r, in Fig. 2.8b includes such losses and must be deduced to measure the power consumption of the AQFP gate. Q_u is expressed as $1/Q_u = 1/Q_{meas} + 1/Q_{qfp}$, where Q_{meas} is the Q of the measurement system and Q_{qfp} is that of the AQFP gate. Using Eq. (2.6), each Q is expressed as $Q_e/Q_{meas} = 1/S_{meas} - 1$ and $Q_e/Q_{qfp} = 1/S_{qfp} - 1$, where S_{meas} is the loss in the measurement system and S_{qfp} is that in the AQFP gate. Combining these equations, S_{qfp} is given by:

$$S_{qfp} = \frac{1}{S_{21}^{-1} - S_{meas}^{-1} + 1}, \tag{2.8}$$

where S_{21} is the measured insertion loss. The power consumption of the AQFP gate, P_{qfp}, is expressed by converting Eq. (2.7):

$$P_{qfp} = \frac{P_{in}}{2} S_{qfp}(1 - S_{qfp}). \tag{2.9}$$

Using Eqs. (2.8) and (2.9), the power consumption of the AQFP gate is measurable, even if non-negligible losses are present in the measurement system.

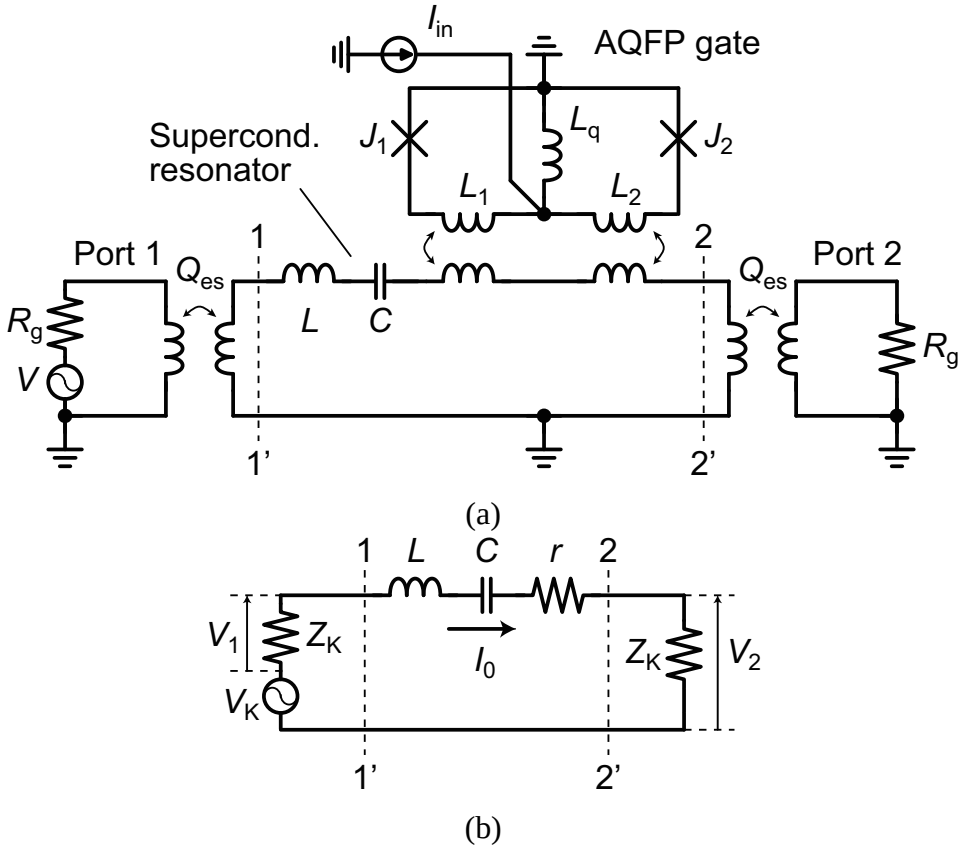


Figure 2.8: (a) Schematic of the circuit used to measure the power consumption of an AQFP gate, where the AQFP gate is magnetically coupled with a resonator and (b) its equivalent circuit. The energy dissipation of the AQFP gate is expressed as a resistance, r.

2.4.2 Measurement results

A superconducting resonator was designed through use of the electromagnetic field simulator, SONNET [Sonnet] and fabricated using the STP2 to measure the energy dissipation of the AQFP gate at 4.2 K. Figure 2.9 shows the micrograph of the 5 GHz superconducting resonator magnetically coupled with an AQFP gate. Figure 2.10 shows the measurement setup for the superconducting resonator-based method. The parameters of the gate were determined as $\beta_L = 0.4$, $\beta_q = 1.6$, and $I_c = 50\,\mu$A ($\beta_c = 0.89$), with which we had experimentally confirmed correct logic operations [小澤 11, Takeuchi13a]. The micrographs correspond to Fig. 2.8a, though a dc offset for the excitation current is added in the measurement. The resonator is a stepped-impedance resonator (SIR) [Makimoto00] that combines low-impedance and high-impedance lines for miniaturization, and the measured resonant frequency was 4.998 GHz and the loaded Q was 357, which is sufficiently high to measure S_{21} with high accuracy.

Figure 2.11a shows the measurement results of S_{21} and P_{qfp} for 5 GHz operation calculated using Eq. (2.9), where a vector network analyzer and a high-speed cryoprobe with a band width of approximately 20 GHz were used for the measurement, and it was assumed that $S_{meas} = -4.0\,\mathrm{dB} = 0.63$. The input current of the AQFP gate was fixed to $5\,\mu$A during the measurement. S_{21} drops when P_{in} is approximately -57 dBm, which indicates that the AQFP gate starts to switch with the flux applied by the resonator. P_{qfp} increases as P_{in} increases because the microwave rises more sharply as its amplitude increases, which varies the potential energy of the gate more quickly and generates more energy dissipation. P_{qfp} is $\sim 50\,$pW for P_{in} of -57 dBm, which corresponds to the bit energy per switching event of $1.0 \times 10^{-20}\,\mathrm{J} \sim 0.1 I_c \Phi_0$ for 5 GHz operation. Figure 2.11b shows the simulation results using the JSIM, where S_{21} was calculated using the circuit shown in Fig. 2.8a. P_{qfp} was obtained by integrating the product of the excitation currents and voltages across L_{x1} and L_{x2} shown in Fig. 2.1. Comparison of Figs. 2.11a and 2.11b indicates good agreement between the measurement and simulation results.

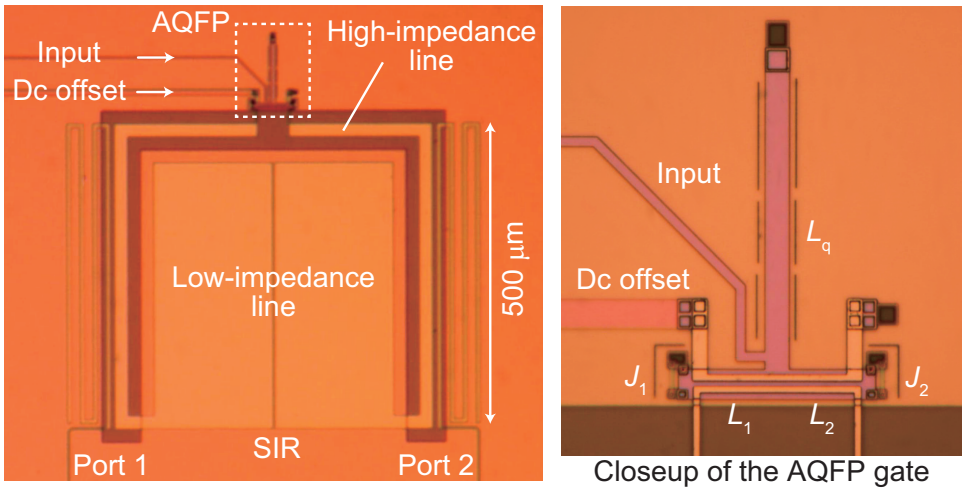


Figure 2.9: Micrographs of the 5 GHz resonator coupled with an AQFP gate with $\beta_L = 0.4$, $\beta_q = 1.6$, and $I_c = 50\,\mu$A ($\beta_c = 0.89$). The dc offset current is necessary to avoid the gate from switching several times within a cycle of the microwave applied by the resonator.

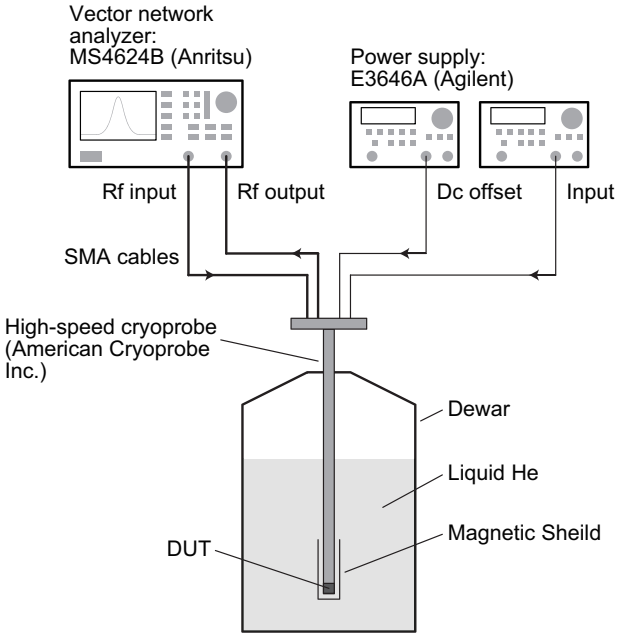


Figure 2.10: Measurement setup for the superconducting resonator-based method.

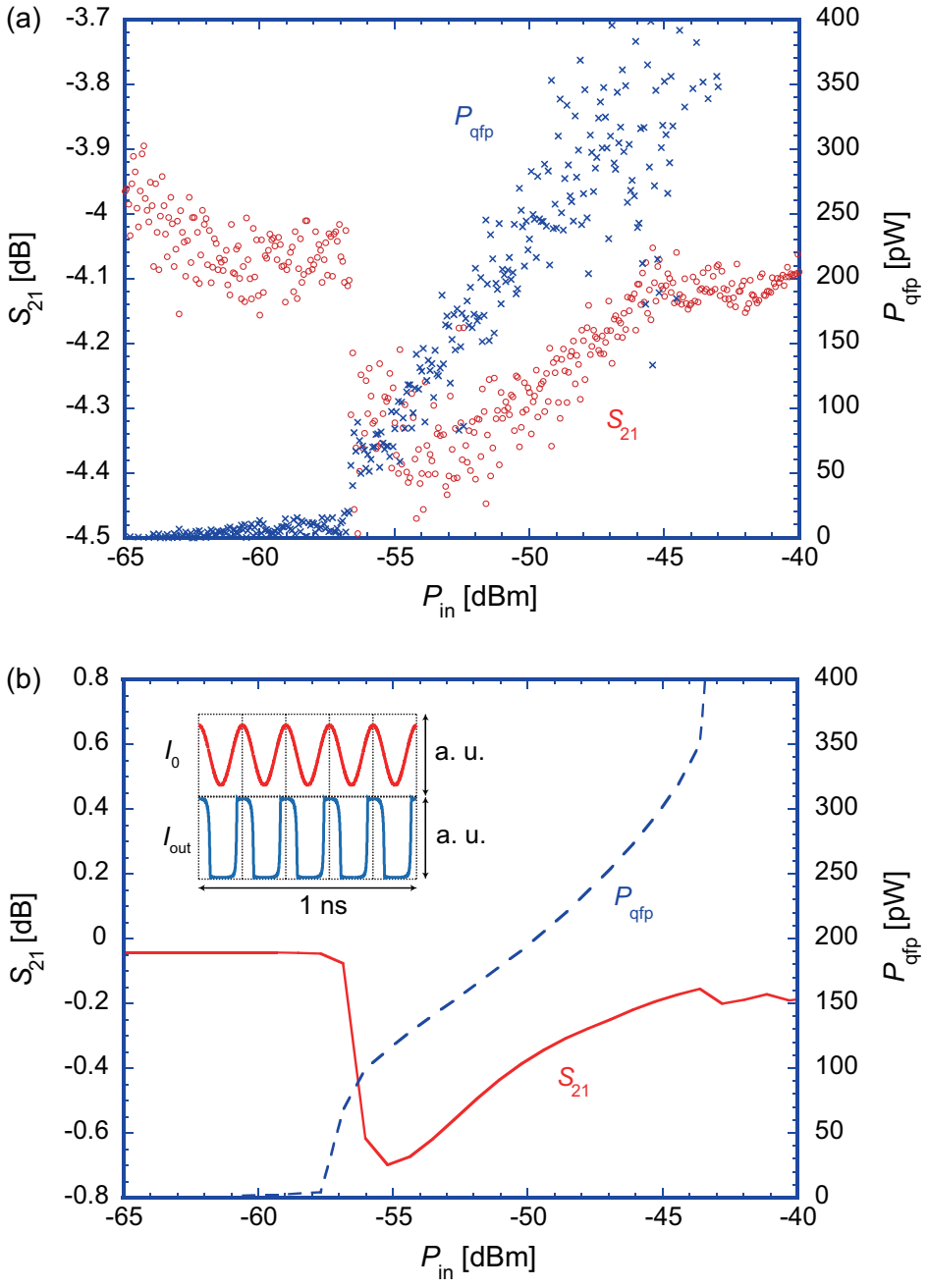


Figure 2.11: (a) Power consumption measured at 5 GHz operation, assuming $S_{meas} = -4.0$ dB. (b) Simulation results of power consumption at 5 GHz operation. The inset shows the transient analysis of I_0 and I_{out}, which confirms that the AQFP gate switches in accordance with the frequency of the microwave applied by the resonator.

2.5 Summary

We investigated the relationship among circuit parameters of an AQFP gate, the bit energy, and the bias margin through circuit simulation and optimized the parameters in terms of both energy and bias margins. The bit energy of the optimized AQFP gate can be decreased to $110k_BT$ for 4.2 K with $I_c = 50\,\mu$A ($\beta_c = 0.89$) and a rise/fall time of 200 ps, which is 6% of $I_c\Phi_0$ and much smaller than that of RSFQ circuits. We also calculated the BER of the optimized gate, and the fitting curves show that the bias margin of the gate is ±19.4% for $E_{bit}/k_BT = 110$ and ±8.8% for $E_{bit}/k_BT = 23.2$, which shows that an AQFP gate can operate in a large computing system with a bit energy approaching k_BT.

We measured the extremely small energy dissipation of an AQFP gate using a superconducting resonator-based method, by which the bit energy of the AQFP gate was evaluated to be 1.0×10^{-20} J with $\beta_L = 0.4, \beta_q = 1.6$, and $I_c = 50\,\mu$A ($\beta_c = 0.89$) for 5 GHz operation. This result provides evidence for ultra-low energy logic operations of the AQFP gate. While the bit energy of an AQFP gate can be further decreased to the order of k_BT by optimizing β_L and β_q, the utilized method can be applied to measure it by increasing Q_e.

Chapter 3

Sub-k_BT bit-energy operation

In Chap. 2, we showed that AQFP gates can operate with sub-$I_c\Phi_0$ bit energy, through both simulation and measurement. More important, in principle, there is no minimum energy dissipation for operations of AQFP gates, unless the entropy of the system decreases. In this chapter, we show it by using underdamped Josephson junctions, through simulation of bit energy and bit error rates. The results obtained in this chapter have been reported in [Takeuchi13d].

3.1 Analytical expression of bit energy

We analytically estimate the energy dissipation of adiabatic switching operations in AQFP logic, which arises from the viscous flow of the system. The switching energy, E_{sw}, is given as follows [Likharev82]:

$$\begin{aligned} E_{sw} &= \int_0^{x_0} \eta \frac{\mathrm{d}x}{\mathrm{d}t} \mathrm{d}x = \int_0^{\tau} \eta \left(\frac{\mathrm{d}x}{\mathrm{d}t} \right)^2 \mathrm{d}t \\ &= \frac{\eta x_0^2}{\tau}, \end{aligned} \tag{3.1}$$

where η is a viscosity factor, τ is the time required for a switching event, x is an arbitrary position on potential, x_0 is the position where a local minimum occurs, as shown in Fig. 3.1. Note that η arises from the subgap resistance and the shunt resistance of a junction. Equation 3.1 indicates that the energy dissipation of an AQFP gate reduces linearly with an increase in a rise/fall time of ac excitation currents, which corresponds to the simulation results in Fig. 2.6.

Additionally, here we focus on the two time constants: an intrinsic switching time of Josephson junctions, τ_{sw}, and a rise/fall time of ac excitation currents, τ_{rf}. When the system varies slowly compared to the time constants of junctions ($\tau_{sw} << \tau_{rf}$), the state of the gate can follow the variation of the potential as shown in Fig. 3.1a.

However, if the system varies fast ($\tau_{sw} \sim \tau_{rf}$), the state cannot follow the variation and eventually shows rapid and irreversible state transition as shown in Fig. 3.1b. Therefore, the bit energy of an AQFP gate, E_{bit}, is given by:

$$E_{bit} = 2I_c\Phi_0\frac{\tau_{sw}}{\tau_{rf}}, \tag{3.2}$$

where $I_c\Phi_0$ is the non-adiabatic energy dissipation for $\tau_{rf} = \tau_{sw}$. The factor of two represents that the junction in the gate switches twice during one clock cycle; it switches when the excitation current rises and falls, respectively. The intrinsic switching time is considered to be the time required for the phase difference to increase by 2π with the junction voltage, I_cR, where R is the combined resistance of the subgap resistance and the shunt resistance. Therefore, τ_{sw} can be given by:

$$\tau_{sw} \approx \frac{\Phi_0}{I_cR} = \sqrt{\frac{2\pi\Phi_0 C}{\beta_c I_c}}, \tag{3.3}$$

where C is the junction capacitance. The bit energy of an AQFP gate can be estimated using Eqs. (3.2) and (3.3), and it is expected to be significantly reduced by increasing β_c ($= Q^2$) of the junctions and lowering the operation frequency.

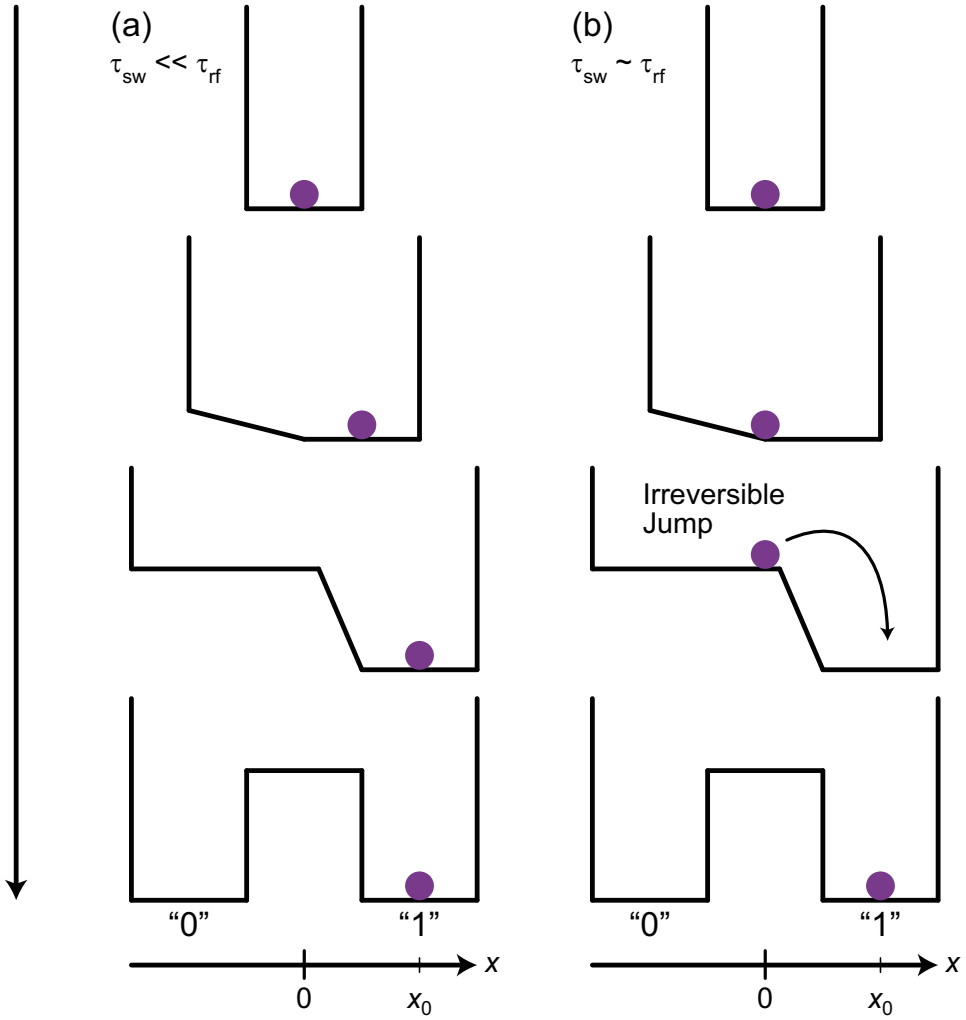


Figure 3.1: Time sequence of a potential energy of an AQFP gate. (a) Slow system with $\tau_{sw} << \tau_{rf}$. (b) Fast system with $\tau_{sw} \sim \tau_{rf}$.

3.2 Simulation of bit energy

Figure 3.2 shows the schematic diagram for calculating the bit energy and the BER of AQFP gates, where six AQFP gates with the same circuit parameters are coupled in series with $I_{in1} = 0.1I_c$, $L_{in} = L_q$, and $k_q = 0.3$. Each excitation current was activated in turn to propagate bit information. These gates are physically and logically reversible, therefore the propagation of the bit information is bidirectional. The bit energy per switching event of each gate was calculated by integrating the product of excitation currents and voltages over time using JSIM. We assumed the use of the STP2. As discussed in Chap. 2, we evaluated the fourth gate of the six because the balance between the energy supplied by the previous gate and that applied to the next gate is complicated near the edge of cascaded AQFP gates.

Figure 3.3 shows E_{bit} as a function of β_c for a rise/fall time of 1000 ps, and Fig. 3.4 shows E_{bit} as a function of a rise/fall time for unshunted junctions ($\beta_c \sim 2600$), where the red solid lines are the simulation results using JSIM and the blue broken lines are the calculation results using Eq. (3.2). In both figures, the simulation results agree well with the calculation results. However, in the region where the rise/fall time is less than ~ 200 ps in Fig. 3.4, the bit energy does not decrease linearly with the rise/fall time. This is because, as the inset shows, long-lasting plasma oscillations dissipate extra energy during a switching event. For a sufficiently long rise/fall time, the frequency of an excitation current is much lower than the plasma frequency, thereby the plasma oscillation can be suppressed. These simulation results confirm that if the rise/fall time is sufficiently long, the energy dissipation of the AQFP gates decreases linearly with the increase of both the rise/fall time of the excitation currents and the intrinsic switching speed of the junctions. Moreover, the bit energy goes below the thermal limit of $k_B T \ln 2 \sim 40$ yJ at 4.2 K. We will show that this extremely small bit energy is achievable, even if we take account of thermal noise at finite temperature.

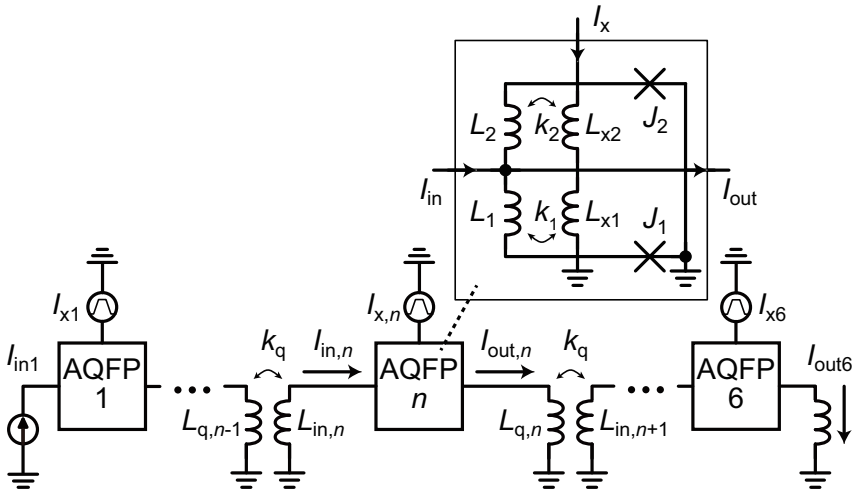


Figure 3.2: Circuit schematic for calculating bit energy and BERs; $\phi_x/2\pi = 0.5$, $\beta_L = 0.2$, $\beta_q = 1.6$, $I_c = 50\,\mu$A, $I_{in1} = 5\,\mu$A, $L_{in} = L_q$, and $k_q = 0.3$. The fourth gate was evaluated because the energy balance with neighboring gates is complicated near the edges of cascaded gates.

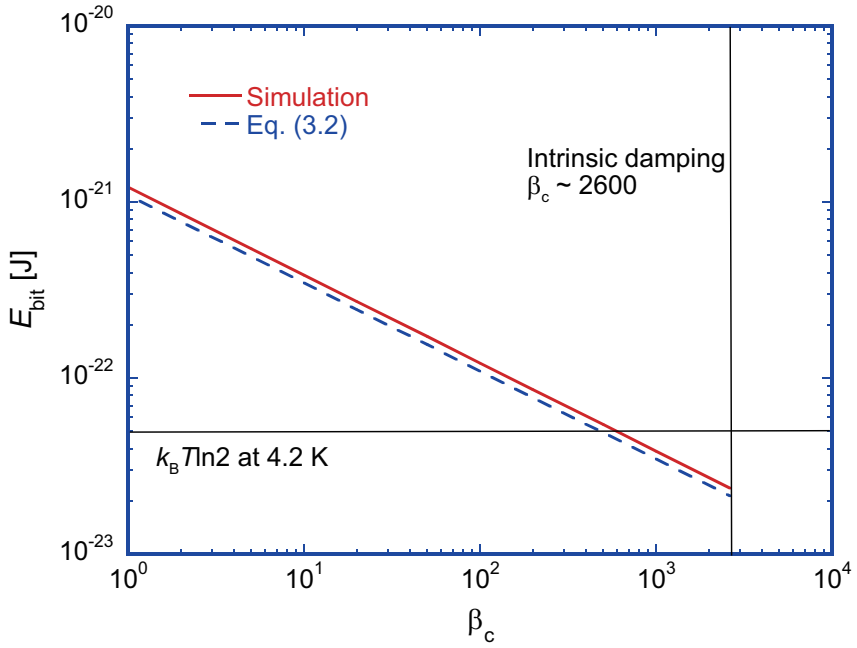


Figure 3.3: Bit energy versus β_c; $\phi_x/2\pi = 0.5$, $\beta_L = 0.2$, $\beta_q = 1.6$, $I_c = 50\,\mu$A, $I_{in1} = 5\,\mu$A, $L_{in} = L_q$, $k_q = 0.3$, and a rise/fall time of 1000 ps.

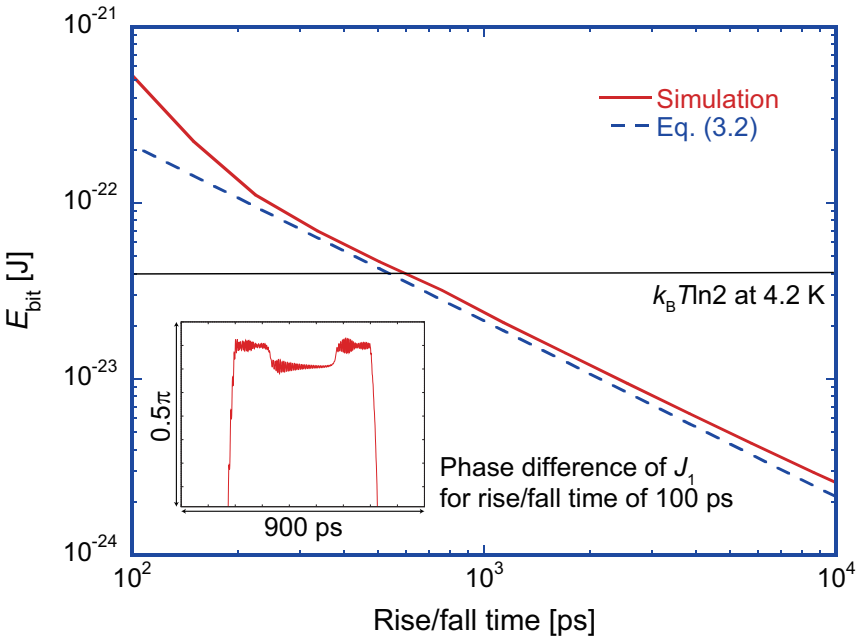


Figure 3.4: Bit energy versus rise/fall time; $\phi_x/2\pi = 0.5$, $\beta_L = 0.2$, $\beta_q = 1.6$, $I_c = 50\,\mu$A, $I_{in1} = 5\,\mu$A, $L_{in} = L_q$, $k_q = 0.3$, and the junctions are unshunted with $\beta_c \sim 2600$.

3.3 Simulation of bit error rate

As shown in Chap. 1, the bit energy of non-adiabatic devices is at least larger than $\sim 1000 k_B T$ to ensure a stable logic state with a long lifetime. On the other hand, the bit energy of an AQFP gate can be decreased by increasing the rise/fall time of ac excitation currents or the intrinsic switching speed of junctions, even though the energy barrier is kept sufficiently large. This means that the energy dissipation of the AQFP gates can be reduced while a sufficiently low BER is maintained. In early studies on QFP gates, there were some analytical and experimental results about the BER of QFP gates [Ruby93, Ko92]. However, these results do not include the relationship between energy dissipation and a BER.

To investigate the relationship between the bit energy, the energy barrier, and the BER of AQFP gates, BERs were calculated using the WRspice. We iterated the simulation 10,000 times for each BER with a time step of $\Delta t = 0.2$ ps. A thermal noise current source, I_n, was added to each subgap resistance, of which the amplitude distribution followed the Gaussian law with the standard deviation given by [Jeffery99] $I_n = (4k_B T f_c/R)^{0.5}$, where f_c is the cutoff frequency given by $1/2\Delta t = 2.5$ THz. Figure 3.5 shows the calculation results at 4.2 K using AQFP gates with unshunted junctions, where the data points are the simulated results and the lines are fitting curves obtained using a complimentary error function. In Fig. 3.5a, I_c was maintained at 50 μA and the rise/fall time was varied from 200 to 2,000 ps to investigate the relationship between the bit energy and the BER. In Fig. 3.5b, the rise/fall time was kept at 200 ps and I_c was varied from 50 to 0.5 μA to investigate the relationship between the energy barrier and the BER. Table 3.1 shows the bias margin, where the BER is smaller than 10^{-23}, as a function of E_b and E_{bit}, where $E_b = I_c \Phi_0$, Π_H and Π_L are the obtained BERs of higher and lower bias regions, respectively. As I_c decreases, both the bit energy and the bias margin decrease. However, as the rise/fall time increases, the bit energy decreases, but the bias margin does not change, because the energy barrier is fixed with $I_c = 50\,\mu$A or $I_c = 5\,\mu$A. This corresponds to the argument of Likharev [Likharev82], that the energy dissipation of a reversible device can be significantly decreased by lowering the operation frequency while the BER is kept sufficiently low. For a rise/fall time of 2,000 ps, the bit energy reaches 12 yJ $= 0.207 k_B T$, but the bias margin is ±21.7% and the BER is still very low. This is even wider than that of gates with critically damped junctions calculated in Chap. 2 and [Takeuchi13b], because the thermal noise current is decreased by the removal of shunt resistors. Such a small bit energy with a very small BER is not achievable for non-adiabatic devices.

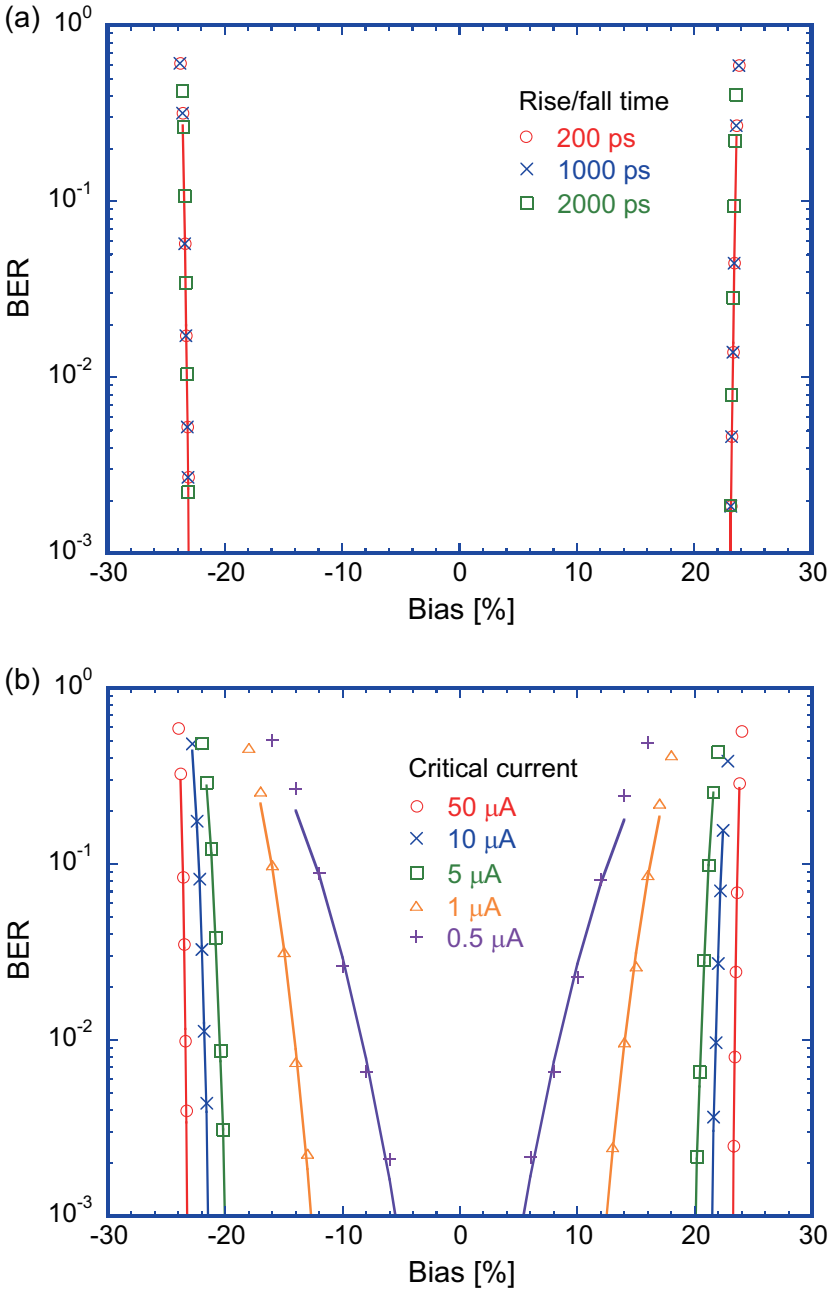


Figure 3.5: BER of the unshunted AQFP gates at 4.2 K; $\beta_L = 0.2$, $\beta_q = 1.6$, $L_{in} = L_q$, $k_q = 0.3$, $I_{in1} = 0.1I_c$. The number of iterations for each BER is 10,000. A bias of 0% corresponds to $\phi_x/2\pi = 0.5$. (a) I_c is kept at 50 μA and the rise/fall time is varied from 200 to 2,000 ps. (b) The rise/fall time is kept at 200 ps and I_c is varied from 50 to 0.5 μA.

Table 3.1: BER and bias margin versus bit energy

I_c [μA]	Rise/fall time [ps]	E_b/k_BT	E_{bit}/k_BT	BER	Bias margin [%]
50	200	$\sim 1,800$	2.28	$\Pi_H = 0.5 \times \text{erfc}[(0.620 - 2\pi\phi_x)/0.00159]$, $\Pi_L = 0.5 \times \text{erfc}[(2\pi\phi_x - 0.380)/0.00162]$	$\pm$21.7
50	1000	$\sim 1,800$	0.41	$\Pi_H = 0.5 \times \text{erfc}[(0.619 - 2\pi\phi_x)/0.00149]$, $\Pi_L = 0.5 \times \text{erfc}[(2\pi\phi_x - 0.381)/0.00147]$	$\pm$21.7
50	2000	$\sim 1,800$	0.207	$\Pi_H = 0.5 \times \text{erfc}[(0.618 - 2\pi\phi_x)/0.00142]$, $\Pi_L = 0.5 \times \text{erfc}[(2\pi\phi_x - 0.382)/0.00130]$	$\pm$21.7
10	200	~ 360	0.456	$\Pi_H = 0.5 \times \text{erfc}[(0.614 - 2\pi\phi_x)/0.00330]$, $\Pi_L = 0.5 \times \text{erfc}[(2\pi\phi_x - 0.386)/0.00337]$	$\pm$18.2
5	200	~ 180	0.228	$\Pi_H = 0.5 \times \text{erfc}[(0.610 - 2\pi\phi_x)/0.00450]$, $\Pi_L = 0.5 \times \text{erfc}[(2\pi\phi_x - 0.390)/0.00460]$	$\pm$15.6
1	200	~ 36	0.0456	$\Pi_H = 0.5 \times \text{erfc}[(0.594 - 2\pi\phi_x)/0.0146]$, $\Pi_L = 0.5 \times \text{erfc}[(2\pi\phi_x - 0.408)/0.0133]$	$\pm$0
0.5	200	~ 18	0.0228	$\Pi_H = 0.5 \times \text{erfc}[(0.588 - 2\pi\phi_x)/0.0281]$, $\Pi_L = 0.5 \times \text{erfc}[(2\pi\phi_x - 0.414)/0.0268]$	$\pm$0
5	1000	$\sim 1,800$	0.041	$\Pi_H = 0.5 \times \text{erfc}[(0.607 - 2\pi\phi_x)/0.00419]$, $\Pi_L = 0.5 \times \text{erfc}[(2\pi\phi_x - 0.393)/0.00427]$	$\pm$15.5

3.4 Quantum-mechanical bound

So far, we have investigated the classical bound in adiabatic switching. Here we estimate the quantum-mechanical bound contributed by the energy-time uncertainty relation [Likharev82]. The energy-time uncertainty condition is given by:

$$\Delta E \times \Delta t \geq \frac{\hbar}{2} \tag{3.4}$$

For $\tau_{rf} = 2000\,\mathrm{ps}$ and $E_{bit} = 0.207 k_B T$, the energy-time product is $4.8 \times 10^{-32}\,\mathrm{J \cdot s}$, which is still much larger than $\hbar/2 \approx 5.28 \times 10^{-35}\,\mathrm{J \cdot s}$. Hence, the energy-time uncertainty relation can be neglected.

3.5 Experimental demonstration of unshunted AQFP gates

We designed and fabricated unshunted AQFP gates using the STP2, to see if the gates can operate correctly without shunt resistors. Figure 3.6 is the micropgraph of the unshunted buffer gates with $\beta_L = 0.2$, $\beta_q = 1.6$, and $I_c = 50\,\mu\mathrm{A}$. A dc-SQUID with $I_c = 50\,\mu\mathrm{A}$ was used for readout and a high-I_c gate with $I_c = 100\,\mu\mathrm{A}$ was inserted before it to reduce backactions from the dc-SQUID. Also, we applied an ac bias current, I_{sq}, to the dc-SQUID to reduce backactions. Figure 3.7 shows the measurement results at 100 kHz, where I_{x1}, I_{x2}, and I_{x3} are three-phase excitation currents. (The measurement setup is shown in Fig. 5.7.) It can be seen that output sequences correspond to the inputs, thus we confirmed correct operations of unshunted AQFP gates. The obtained bias margins were ±25.4%, ±26.3%, ±26.6%, and ±17.4% for I_{x1}, I_{x2}, I_{x3}, and I_{sq}, respectively, which are wide enough to achieve logic circuits using the unshunted gates.

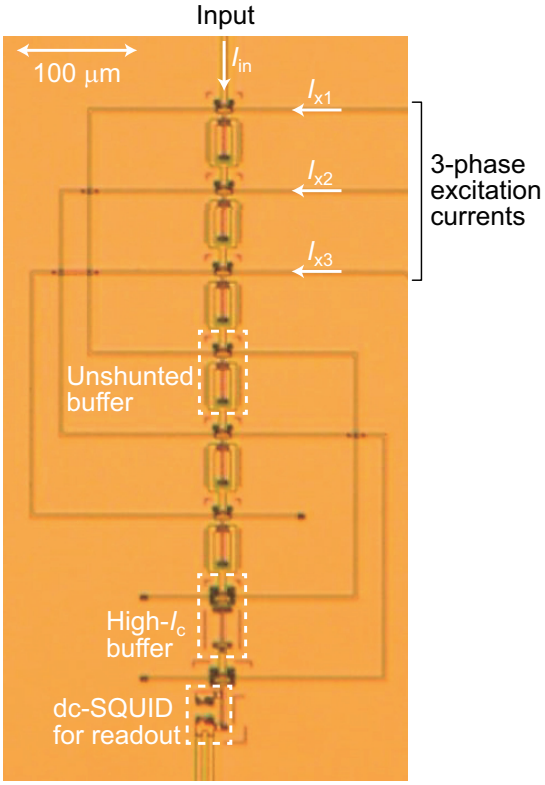


Figure 3.6: Micrograph of unshunted AQFP gates.

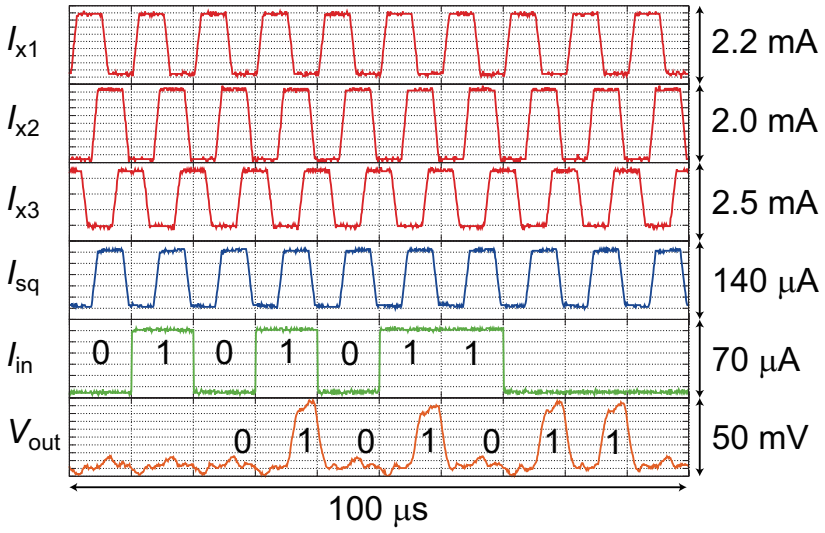


Figure 3.7: Measurement results of unshunted AQFP gates at 100 kHz.

3.6 Summary

We calculated the bit energy and the BER of AQFP gates with underdamped junctions. The bit energy reaches 12 yJ using unshunted 50 μA junctions and excitation currents with a rise/fall time of 2000 ps. Moreover, the BER is still low, even though the bit energy is below the thermal energy; the bias margin, where the BER is smaller than 10^{-23}, is ±21.7%. These results indicate that there is no minimum energy dissipation for operating AQFP gates, unless the entropy of the system decreases. This conclusion is very important to achieve practical computing systems with extremely small bit energy. Also, we discussed the quantum-mechanical bound on operations of AQFP gates. Calculation results showed that the energy-time uncertainty relation can be neglected for our design parameters. Finally, we experimentally demonstrated AQFP gates with unshunted junctions, to see if they can work without shunt resistors.

Chapter 4

Purely reversible logic gates

One of the obstacles to achieve practical reversible logic gates is that they must be built by using very energy-efficient logic devices with bit energy around the order of thermal energy. Another difficulty is that reversible logic gates must be both logically and physically reversible, or purely reversible. In this chapter, we propose the first practical reversible logic gate using AQFP gates, whose bit energy can be below thermal energy as shown in Chap. 3, and experimentally demonstrate the logical and physical reversibility of the gate. Additionally, we estimate the energy dissipation of the gate, and discuss the minimum energy dissipation required for reversible logic operations. The results obtained in this chapter have been reported in [Takeuchi14a].

4.1 Physical reversibility

A logic gate is considered to be physically reversible if its potential energy changes adiabatically and reversibly. Konstantin K. Likharev argued that physical reversibility is necessary to prevent non-adiabatic energy dissipation during a switching event [Likharev82], as well as logical reversibility. The bit information in a physically reversible gate can propagate bi-directionally, therefore the circuit topology of a reversible logic gate must be symmetrical in the data flow direction. In this study, we utilize 3-in majority (MAJ) gates and 3-out splitter (SPL) gates as the building blocks for reversible logic gates. Figure 4.2 shows the block diagram of the 3-in MAJ gate with three input buffers, where the white block corresponds to an AQFP buffer gate (Fig. 4.1). The state of the buffer gate in the MAJ gate is determined by the sum of the three input currents, I_{ina}, I_{inb}, and I_{inc}. Therefore, the logic state of the output port, x, is defined as $x = \mathrm{MAJ}(a, b, c) = a \cdot b + b \cdot c + c \cdot a$, where a, b, c are the logic states of the three input ports. Figure 4.3 is the block diagram of the 3-out SPL gate with an input buffer. The input current, I_{ina}, is shared by the three buffer gates in the SPL gate, and the logic states of each output port are determined to be $x = y = z = a$. The

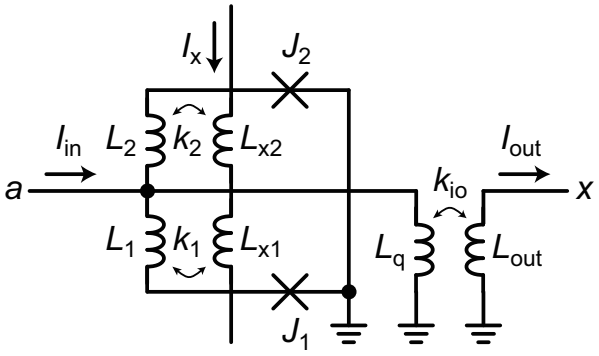


Figure 4.1: Schematic of an AQFP buffer/NOT gate. For $k_{io} > 0$, the gate operates as a buffer gate, and for $k_{io} < 0$, it operates as a NOT gate. Circuit parameters were optimized as $\phi_x/2\pi = 0.5$, $\beta_L = 0.2$, and $\beta_q = 1.6$. The critical current, I_c, is $50\,\mu$A (unshunted).

3-in MAJ gate and the 3-out SPL gate have the same circuit topologies, while the data flow direction, or the order of the excitation of each gate, is opposite. Furthermore, although the 3-in MAJ and 3-out SPL gate themselves are not reversible, a logically and physically reversible gate can be obtained by combining several 3-in MAJ gates and 3-out SPL gates.

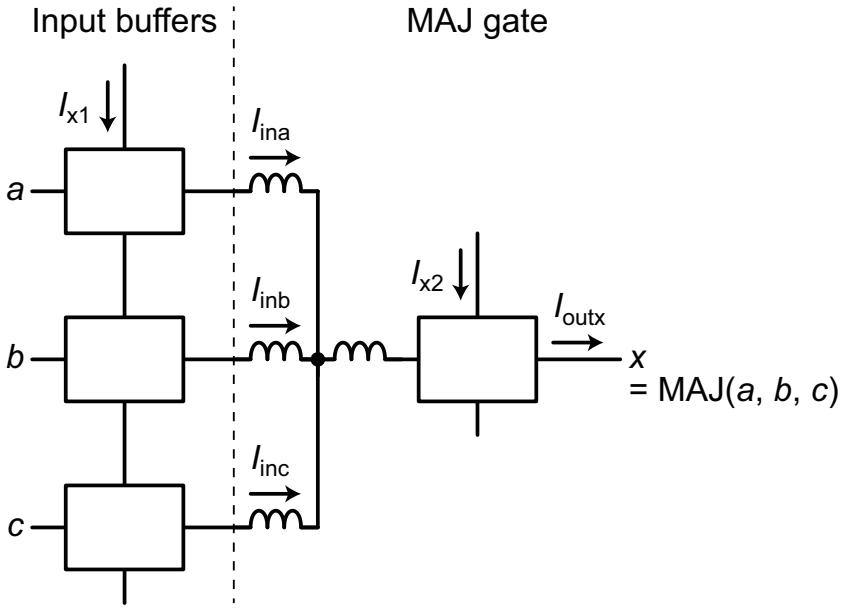


Figure 4.2: Schematic of an AQFP 3-in MAJ gate. White blocks correspond to AQFP buffer gates.

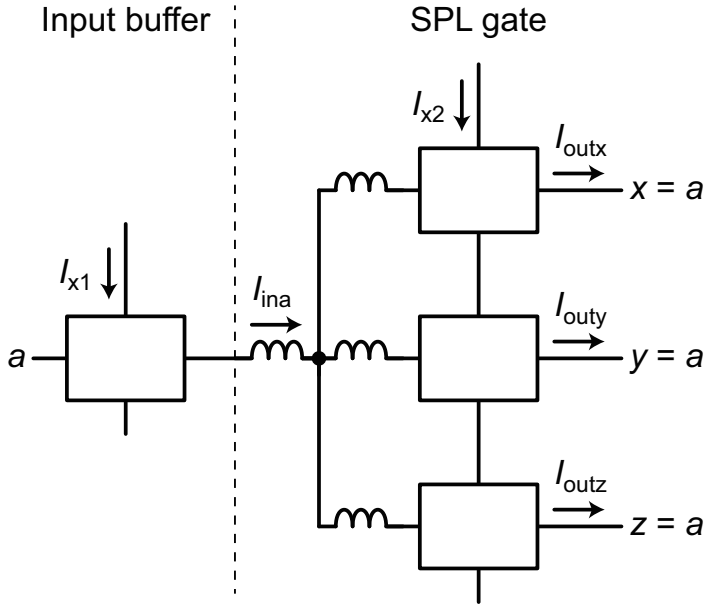


Figure 4.3: Schematic of an AQFP 3-out SPL gate, whose circuit topology is the same as that of a 3-in MAJ gate.

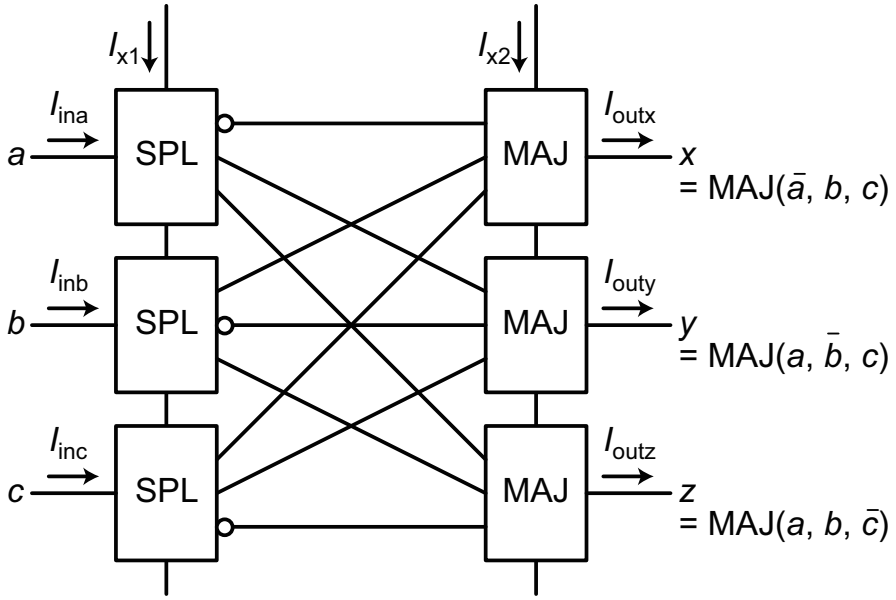


Figure 4.4: Schematic of the RQFP gate. $x = \mathrm{MAJ}(\overline{a}, b, c)$, $y = \mathrm{MAJ}(a, \overline{b}, c)$, $z = \mathrm{MAJ}(a, b, \overline{c})$, which are logically reversible. The circuit topology of the RQFP gate is symmetrical, because those of a 3-in MAJ gate and a 3-out SPL gate are the same.

4.2 Reversible QFP gate

Figure 4.4 shows the block diagram of our proposed 3-in and 3-out reversible logic gate, which we have designated as the reversible quantum-flux-parametron (RQFP) gate. The RQFP gate is composed of three 3-in MAJ gates and three 3-out SPL gates, whose function is represented by the following equation:

$$F(a, b, c) = (\mathrm{MAJ}(\overline{a}, b, c), \mathrm{MAJ}(a, \overline{b}, c), \mathrm{MAJ}(a, b, \overline{c})). \tag{4.1}$$

Table 4.1 is the truth table of the RQFP gate. This table clearly shows that the gate is injective and logically reversible by operating the function two times: $F(F(a, b, c)) = (a, b, c)$. Additionally, the RQFP gate is considered to be a primitive gate in reversible computing, because MAJ gates, NOT gates, and constant inputs constitute a logical primitive. Because a 3-in MAJ gate and a 3-out SPL gate have the same circuit topologies, that of the RQFP gate is symmetrical. The data in the RQFP gate can propagate bi-directionally due to this symmetrical circuit topology, depending on the order of excitation. Specifically, if the SPL gates are excited earlier (excitation current, I_{x1} is provided earlier than I_{x2}), the data propagate from the ports, *a*, *b*, and *c* to *x*, *y*, and *z*. If the MAJ gates are excited earlier, the data propagate in the opposite direction. Therefore, the RQFP gate is physically reversible.

Table 4.1: Truth table of the RQFP gate

a	b	c	d	e	f
0	0	0	0	0	0
1	0	0	0	1	1
0	1	0	1	0	1
1	1	0	0	0	1
0	0	1	1	1	0
1	0	1	0	1	0
0	1	1	1	0	0
1	1	1	1	1	1

4.2.1 Simulation of energy dissipation

We calculated the energy dissipation of the RQFP gate by integrating the product of excitation currents and voltages over time using JSIM. Figure 4.5a shows the block diagram for the simulation, where input and output buffers are inserted to avoid interactions with input and output ports. Figure 4.5b provides the simulation results and shows the total energy dissipation per clock cycle, including an RQFP gate, input and output buffers, as a function of a rise/fall time of excitation currents. As can be seen in the figure, energy dissipation decreases almost linearly with an increase in the rise/fall time for all input patterns, which indicates that all gates operate adiabatically and reversibly during logic operations as shown in Chap. 3. For a rise/fall time of 10,000 ps, the total energy dissipation of the RQFP gate and buffers composed of 69 AQFP gates reaches $\sim 1\times10^{-21}$ J/cycle. The bit energy per AQFP gate is $\sim 2\times10^{-23}$ J/cycle, which is much smaller than the energy barrier, $I_c\Phi_0 \sim 1.0\times10^{-19}$ J for $I_c = 50\,\mu$A and around the same order of magnitude as the Landauer bound at 4.2 K, $k_BT\ln2 \sim 4.0\times10^{-23}$ J. These calculation results show that there is no minimum energy dissipation for reversible logic operations using the RQFP gates.

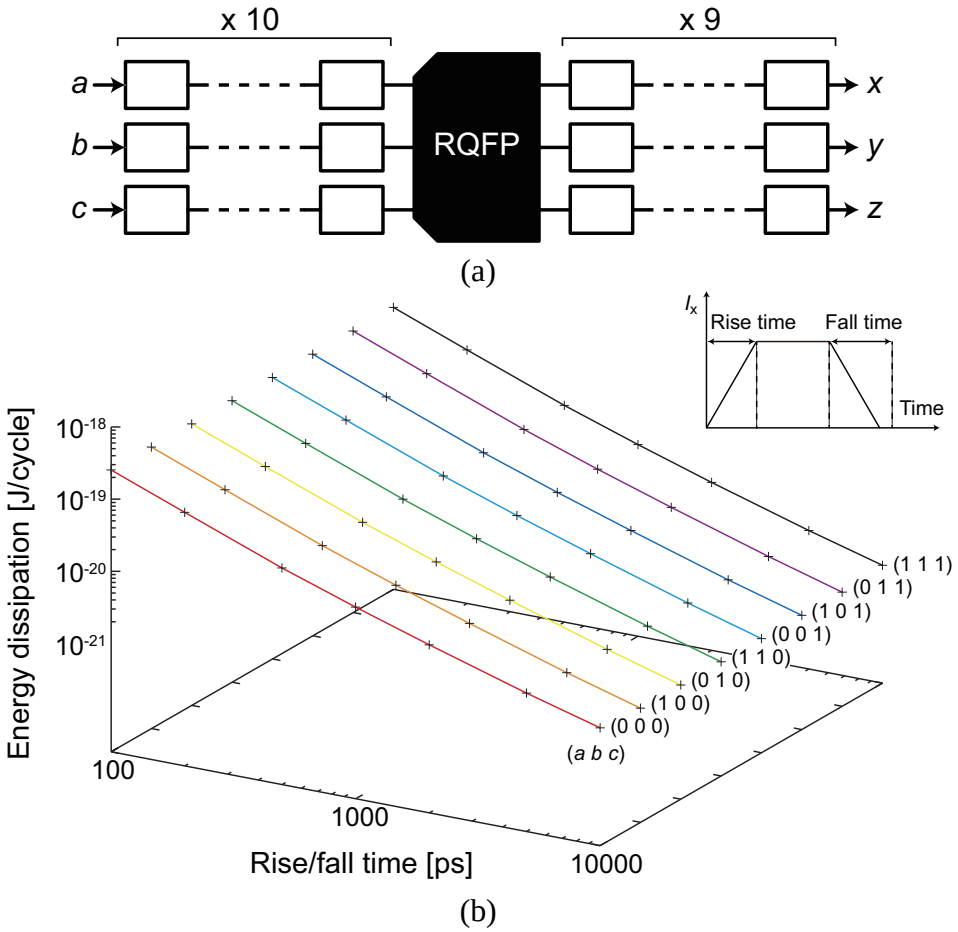


Figure 4.5: Energy dissipation of the RQFP gate. (a) Block diagram for simulation. Input and output buffers were inserted to avoid interactions with input and output ports. (b) Simulated energy dissipation, including an RQFP gate, input and output buffers. It was assumed that $L_{out} = L_q$ and $k_{io} = 0.1$ for AQFP buffer gates, and that each wiring inductance is 10 pH for 3-in MAJ gates and 3-out SPL gates. For all input patterns, the dissipation decreases almost linearly with an increase of a rise/fall time of excitation currents. The inset shows the definition of the excitation current.

4.2.2 Experimental demonstration of logical and physical reversibility

To demonstrate the logical and physical reversibility of an RQFP gate, we conducted three kinds of experiments, α, β, and γ. The block diagrams of these three experiments are shown in Fig. 4.6, where a, b, and c are input ports and x, y, and z are output ports. In the experiment α, we demonstrate logic operations of an RQFP gate. In β, two RQFP gates are serially connected to demonstrate logical reversibility. Specifically, if $a = a'$, $b = b'$, and $c = c'$, the RQFP gate is injective and proven to be logically reversible. In γ, two RQFP gates are connected but one is physically mirrored to demonstrate physical reversibility. Specifically, if $a = a''$, $b = b''$, and $c = c''$, data can propagate bi-directionally in an RQFP gate, and the gate is proven to be physically reversible. The RQFP gates were designed with the inductance extractor, InductEx [Fourie11] and fabricated using the STP2. Figure 4.7 is the micrograph of the circuits used in the experiment γ, where I_{x1}, I_{x2}, and I_{x3} are three-phase excitation currents. Here, it can be seen that two RQFP gates are serially connected but their physical layouts are horizontally mirrored. Figure 4.8 shows the measurement results of the experiments α, β, and γ, using trapezoidal excitation currents of 100 kHz at 4.2K. (The measurement setup is shown in Fig. 5.7.) In the experiment α, the correct logic operations of the RQFP gate were confirmed, with bias margins of ±22.0%, ±26.3% and ±30.3% for I_{x1}, I_{x2}, and I_{x3}, respectively. In β, the obtained outputs (a', b', and c') corresponded to the inputs (a, b, and c), which proves the logical reversibility of the RQFP gate. Similarly, the outputs corresponded to the inputs in γ, which proves its physical reversibility. These results confirm that the RQFP gate is logically and physically reversible, and that the RQFP gate is a practical reversible logic gate.

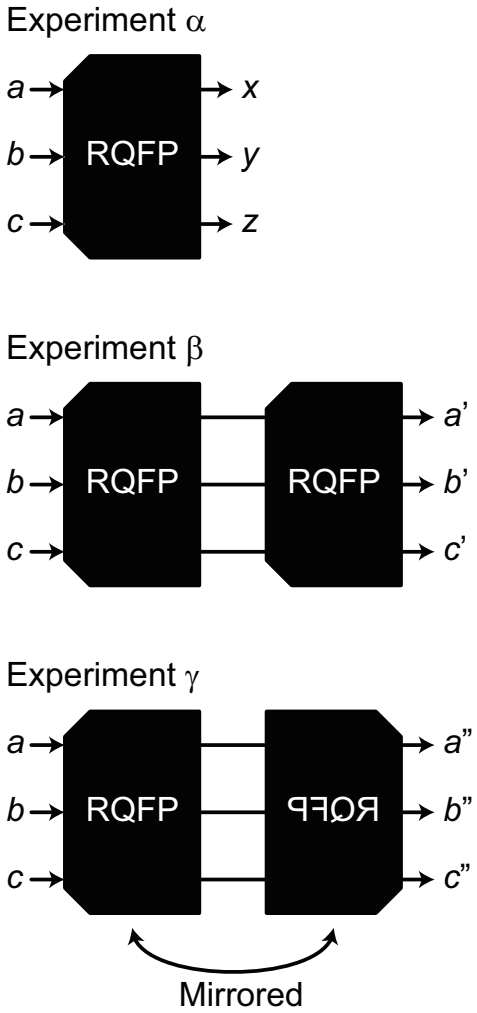


Figure 4.6: Block diagrams for the experiments α, β, and γ. In α, three inputs (a, b, and c) are externally applied and three outputs (x, y, and z) are observed to confirm its logic operations. In β, two RQFP gates are serially connected to determine if the gate is injective. In γ, two RQFP gates are serially connected but one is mirrored to determine if data can propagate bi-directionally.

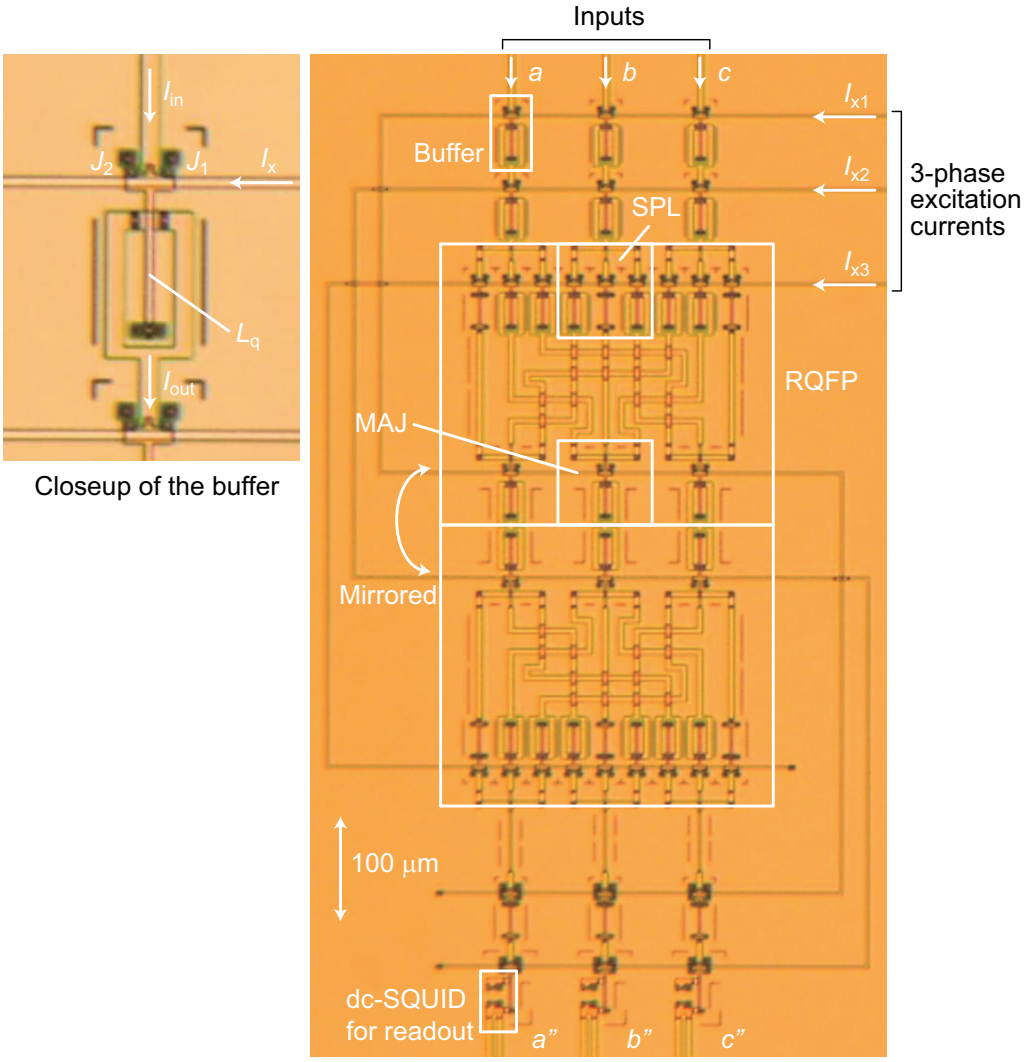


Figure 4.7: Micrograph of circuits for the experiment γ. dc-SQUIDs were used for the readout of output ports (a'', b'', and c''), which detect output currents of buffer gates. One of the two RQFP gates is physically mirrored.

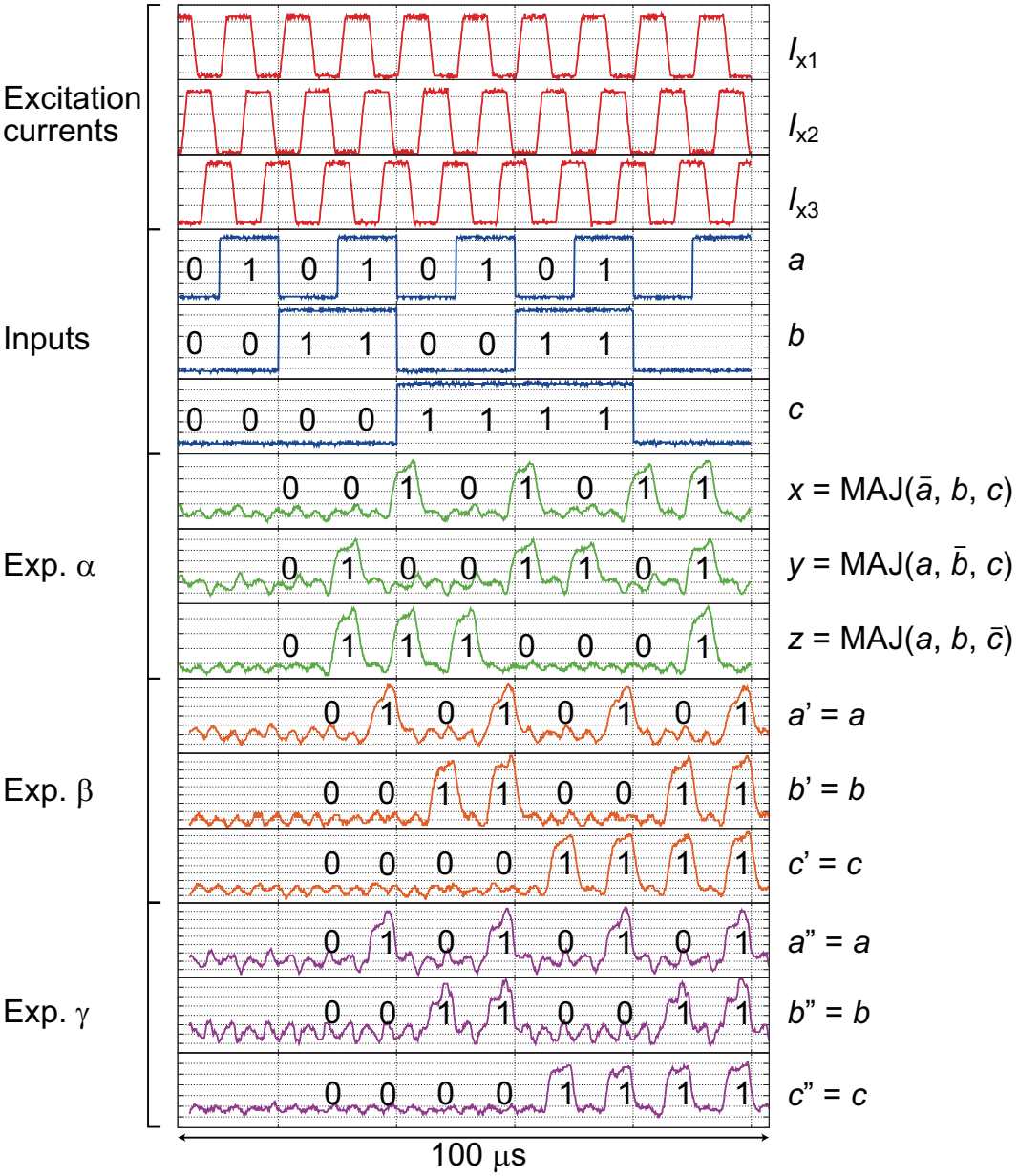


Figure 4.8: Measurement results, which were conducted at 4.2 K in liquid He. We used three-phase trapezoidal excitation currents of 100 kHz (I_{x1}, I_{x2}, and I_{x3}). Input currents (a, b, and c) were given by using a data-pattern generator. Output voltages were amplified by differential amplifiers.

4.3 Energy dissipation of irreversible logic gates

In this section, we show the energy dissipation of irreversible logic gates using AQFP logic, in order to clearly show that reversible logic gates must be both logically and physically reversible. Section 4.3.1 shows the energy dissipation of an AND gate, which is logically and physically irreversible. Section 4.3.2 shows that of a CNOT gate, which is logically reversible but physically irreversible. In both circuits, there are minimum energy bounds for logic operations, because of logical or physical irreversibility. These results support the calculation results in Fig. 4.5, where we showed that there is no minimum energy dissipation for logic operations using our proposed logically and physically reversible devices, RQFP gates.

4.3.1 Logically and physically irreversible gates

AND gates are logically and physically irreversible, where inputs are not uniquely determined from outputs. An AND gate is achieved by using a 3-in MAJ gate, one of whose inputs is fixed to “0”. Similarly, an OR gate is achieved by fixing one of the inputs to “1”. Figure 4.9a shows the block diagram for the calculation of the energy dissipation of AND gates, and Fig. 4.9b shows the calculation results. Energy dissipation depends on input data due to interactions between each gate, and it can be seen that there is a minimum energy dissipation when an input is “0” and the other is “1”. This is because, as Likharev argued [Likharev82], back actions from AND gates to the input buffer gates cause irreversible and non-adiabatic state transition when the input buffer gates are reset.

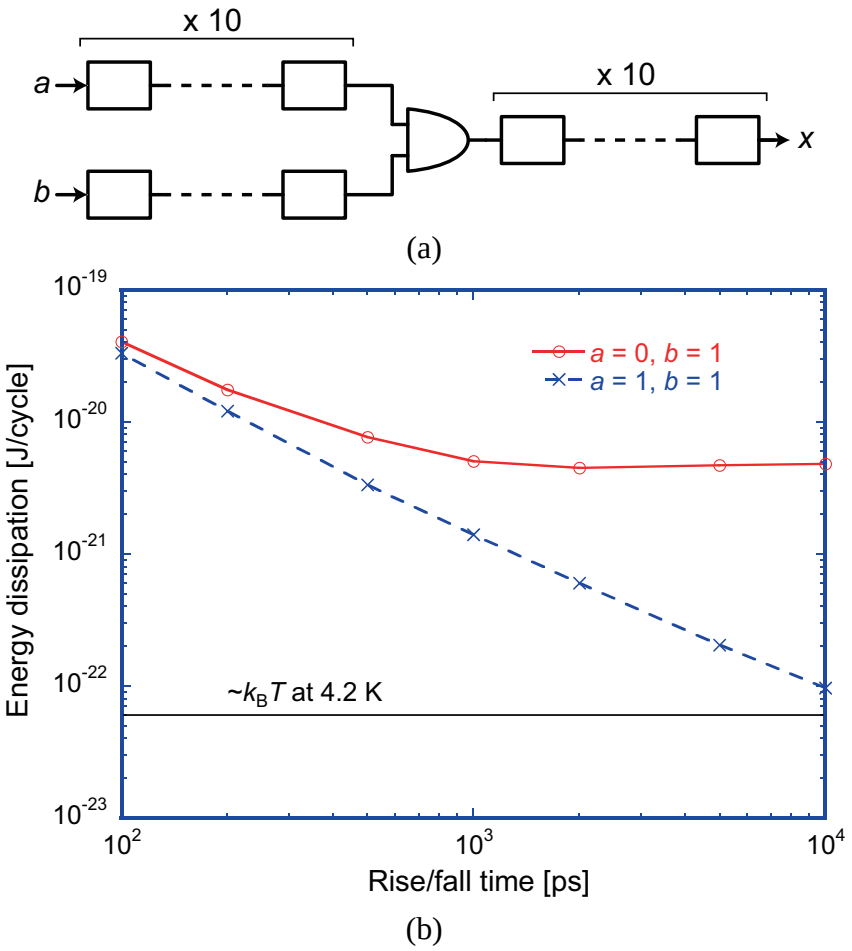


Figure 4.9: Energy dissipation of the AND gate. AND is achieved by using a 3-in MAJ gate, one of whose inputs is fixed to "0". (a) Block diagram for simulation. (b) Simulated energy dissipation, including an AND gate, input and output buffers.

4.3.2 Logically reversible but physically irreversible gates

CNOT gates are logically reversible but physically irreversible in our circuit design. Figure 4.10a shows the block diagram for the calculation of the energy dissipation, and Fig. 4.10b shows the calculation results. It can be seen that there is a minimum energy dissipation, even though the gate is logically reversible. This is because the circuit topology of a CNOT gate, which is composed of AND, OR, 2-out SPL, and 3-out SPL gates, is not symmetrical, and hence the CNOT gate is physically irreversible. These calculation results indicate that physical reversibility, as well as logical reversibility, is necessary for reversible logic operations.

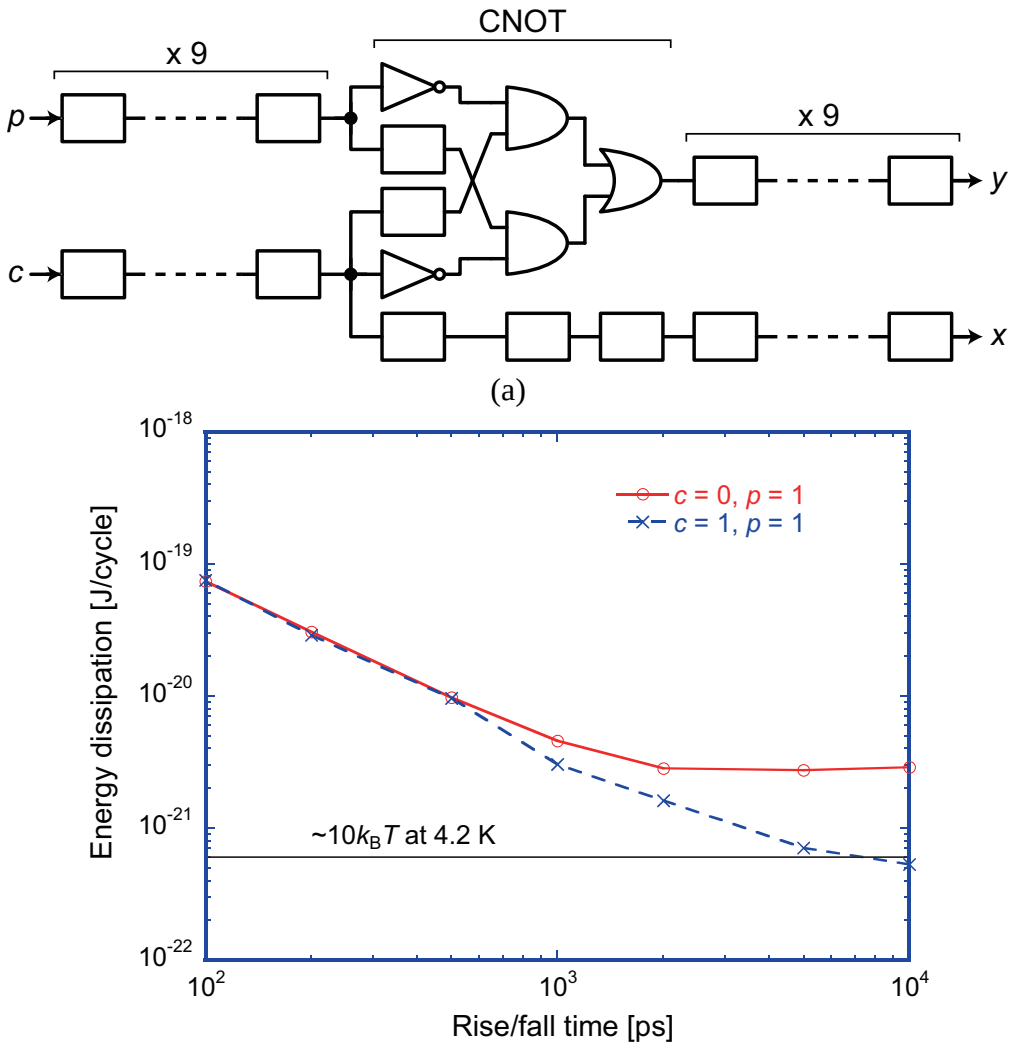


Figure 4.10: Energy dissipation of the CNOT gate. (a) Block diagram for simulation. (b) Simulated energy dissipation, including a CNOT gate, input and output buffers.

4.4 Summary

We proposed a logically and physically reversible logic gate using adiabatic superconducting devices, which we designated as the RQFP gate. We calculated the energy dissipation and confirmed that there is no minimum energy dissipation for logic operations using RQFP gates. To the best of our knowledge, these are the first calculation results that show no minimum energy dissipation in reversible computing that use practical circuit structures. Moreover, we experimentally demonstrated the logical and physical reversibility of the RQFP gate. We believe that our research results will enable "reversible computing" to move from the theoretical stage into practical usage. Additionally, these results will facilitate detailed discussions and investigations related to the energy efficiency of reversible computing.

Chapter 5

Novel energy-efficient latches

Experimental demonstrations of logic circuits using AQFP logic have been reported [Inoue13]. However, at present, there exists no latch for AQFP logic so far, which is an essential component of digital computing systems. In the early study of QFP logic, several latches were proposed [Harada87, Casas92], but none were practical due to their operation principles. For example, the ring shift register [Casas92] holds data by permanently propagating data in a ring of serially connected gates. This type of register requires large area and many Josephson junctions, and it requires several clock cycles for both read and write. In this chapter, we propose the quantum-flux-latch (QFL) as a compact and compatible latch for AQFP logic, that can be read or written in one clock cycle. We discuss its energy efficiency through simulation and experimentally demonstrate the QFL and a 1-bit shift register using a QFL. Also, we propose a high-speed test circuit using QFLs. The results obtained in this chapter have been reported in [Takeuchi14b, Takeuchi14c].

5.1 Quantum-flux-latch

Figure 5.1 shows the circuit schematic of a QFL, which is composed of an AQFP buffer gate whose input inductance is replaced with a storage loop with a write junction, J_0. The existence or the absence of an SFQ stored in this loop determines its internal state. The buffer gate, which we refer to as the read gate, can read the internal state non-destructively. The flux state in the storage loop changes only when an SFQ is stored or escapes. The circuit parameters of the read gate, which is excited by the ac excitation current, I_x, were determined so that the read gate can drive the readout dc-SQUID, which is directly coupled with the read gate; $\beta_L = 0.4$, $\beta_q = 3.3$, and $I_c = 100\,\mu$A ($\beta_c = 1.0$). The parameters of the storage loop, which is biased by the dc bias current, I_b, were determined so that the applied flux from AQFP write gates is large enough to change the internal state; $L_{ina} = L_{inb} = 22.4\,$pH, $L_b = 2.86\,$pH,

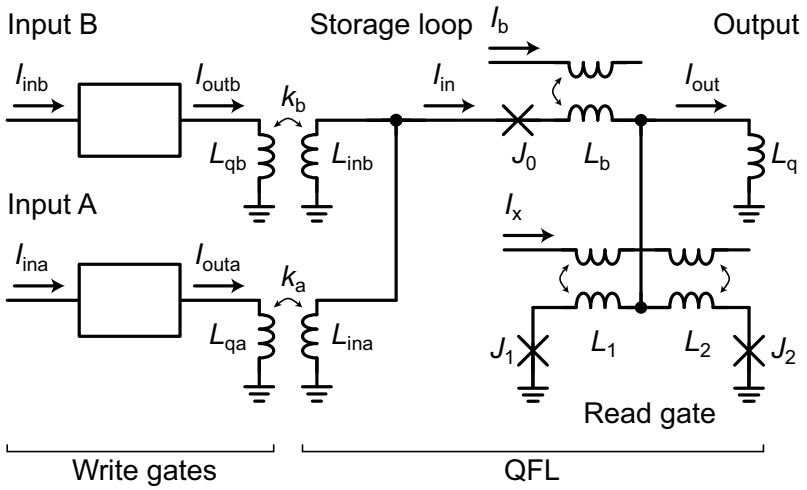


Figure 5.1: Circuit schematic of a QFL. $J_0 = 40\,\mu$A ($\beta_c = 4.0$), $L_{ina} = L_{inb} = 22.4$ pH, $L_b = 2.86$ pH, $k_a = k_b = 0.482$. For the write gates, $\beta_L = 0.2$, $\beta_q = 2.6$ and $I_c = 50\,\mu$A ($\beta_c = 1.0$). For the read gate, $\beta_L = 0.4$, $\beta_q = 3.2$ and $I_c = 100\,\mu$A ($\beta_c = 1.0$).

$k_a = k_b = 0.482$, $J_0 = 40\,\mu$A ($\beta_c = 4.0$). The write gates are buffer gates with $\beta_L = 0.2$, $\beta_q = 2.6$ and $I_c = 50\,\mu$A ($\beta_c = 1.0$). Because AQFP gates switch at every clock cycle of excitation currents, the write gates need to achieve three states: "Write 0", "Write 1" and "Hold". This is why a QFL needs two write gates, which is significantly different from the previously studied latch circuit [Harada87]. When both of the two write gates are in the logic state "1", J_0 switches and the storage loop stores an SFQ, which corresponds to "Write 1". When both of them are in "0", the stored SFQ escapes from the storage loop, which corresponds to "Write 0". When the two write gates are in the different logic states, the QFL holds its current state, which is "Hold", because the applied fluxes from the write gates cancel each other. The advantage of QFLs is its compactness, the compatibility with AQFP logic gates, and quick readout. A QFL is composed of only three Josephson junctions. The read gate has the same structures with buffer gates. Moreover, a QFL requries only one clock cycle for read and write.

5.1.1 Simulation results

Figure 5.2 shows the simulation results of the QFL operating at 5 GHz, using the JSIM. We assumed the use of the STP2. The write gates and the read gates are driven by three-phase sinusoidal excitation currents. Here, I_{out} is the output current of the read gate, and θ_0 is the phase difference of J_0. When the write gates achieve "Write 0" or "Write 1", θ_0 exhibits 2π leaps, resulting in the inversion of I_{out}. Otherwise, I_{out} holds the same logic values. Figure 5.3 shows the results of margin analysis, which

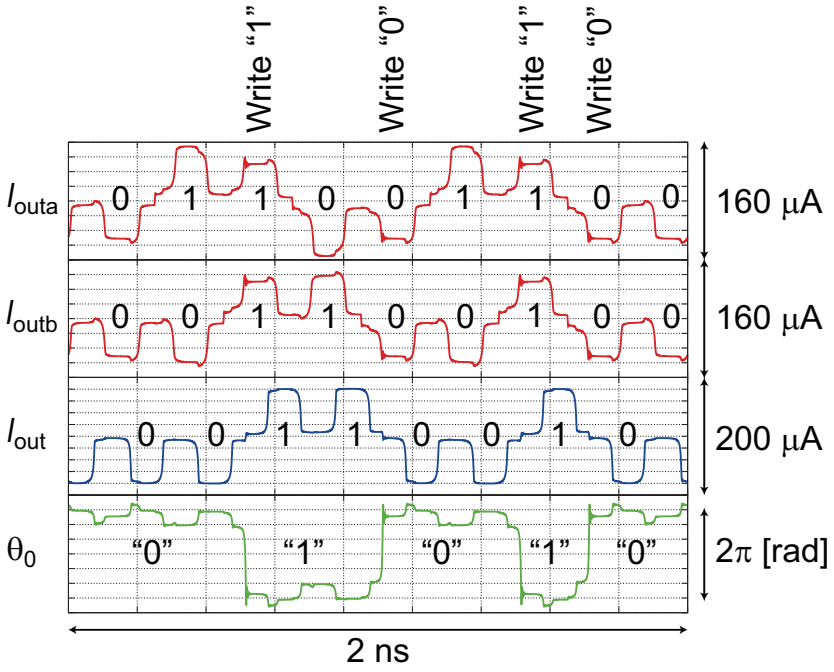


Figure 5.2: Transient analysis of the QFL operating at 5 GHz. When θ_0 shows 2π leaps, the output current of the read gate is inverted.

indicates that the QFL has very wide parameter margins and the critical parameter is I_b, which has a margin of ±22%. This is because the storage loop inductance must be small enough to be driven by the write gates, where LI_c product is $\sim 0.3\Phi_0$.

5.1.2 Energy efficiency

We calculated the energy dissipation of the QFL by integrating the product of excitation currents and voltages over time. The energy dissipation including the two write gates is ~ 0.1 aJ/bit, which results in an EDP of 20 aJ · ps. Table 5.1 shows the EDPs of latches in superconductor logics [Tanaka12, Volkmann13b]. The QFL has the smallest EDP. Note that a reduction in critical currents also contributes to achieving such a small EDP. One of the most important advantages in AQFP logic is that critical currents can be significantly reduced (~ 50 μA or even smaller) while keeping the BER very low (see Chap. 3). On the other hand, critical currents in RSFQ logic and its variants have to be relatively large (~ 100 μA), because the junctions are biased at approximately 80% of critical currents.

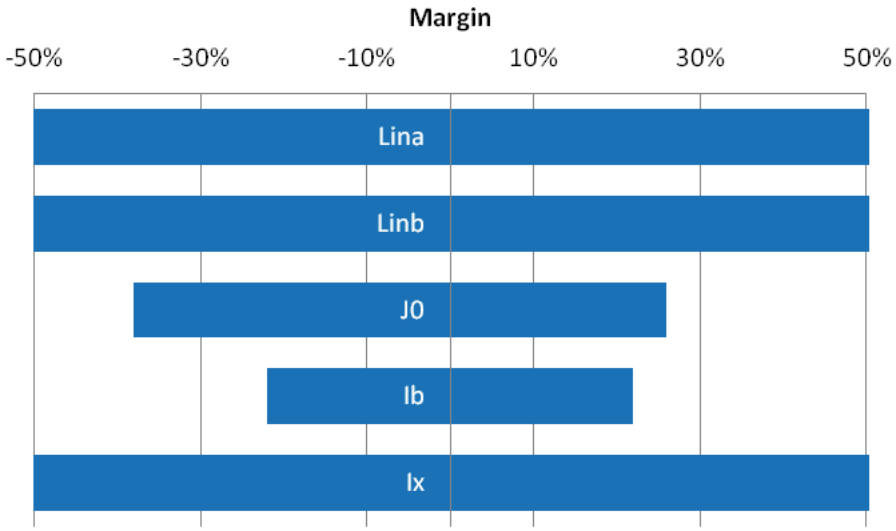


Figure 5.3: Margin Analysis of the QFL. The critical parameter is I_b, whose margin is ±22%.

Table 5.1: Comparison of EDPs of latches in superconductor logics

Logic	Circuit	Energy, E [aJ]	Frequency, f [GHz]	EDP, E/f [aJ·ps]
RSFQ	Shift register	30	55	2364
LV-RSFQ	Shift register	4.0	18	222
eSFQ	Shift register	1.1	24	46
AQFP	QFL	~ 0.1	5	20
AQFP	Shift register	~ 0.6	5	120

5.2 Shift register

We designed shift registers using QFLs to demonstrate somewhat complex circuits. Figure 5.4 shows the block diagram of the shift register, that is driven by four-phase sinusoidal excitation currents, where the white blocks are AQFP buffer gates. The shift signals flow against the data propagation. When the shift signal is “0”, the selector prevents the two write gates from having the same logic states in order to retain the state of the QFL. The state is written only when the shift signal is “1”. Figure 5.5 shows the simulation results of the shift register operating at 5 GHz, where I_{shift} is the output current of the buffer gate, which propagates shift signals, and I_{data} is the output current of the neighbor shift register. The simulation results indicate that the shift register latches only when the shift signal is “1”. With 33 junctions/bit, the energy dissipation is $\sim 0.6\,\mathrm{aJ/bit}$. Further reduction of the energy dissipation can be achieved by the following two methods. In the current design, the junctions in the AQFP gates are critically damped with $\beta_c \sim 1.0$. However, as β_c increases with an increase in shunt resistances, the intrinsic switching speed of the junctions increases and the phase differences change more adiabatically, which results in a further reduction in energy dissipation as discussed in Chap. 3 and [Takeuchi13d]. The other method is to reduce the number of the junctions per bit. Here, we drive the shift register by using four-phase excitation currents. However, we expect the write gates of the fourth phase can be incorporated into the OR gate of the third phase, which would enable driving with three-phase excitation currents. As a result, the number of the junctions per bit can be expected to decrease to 27 junctions/bit.

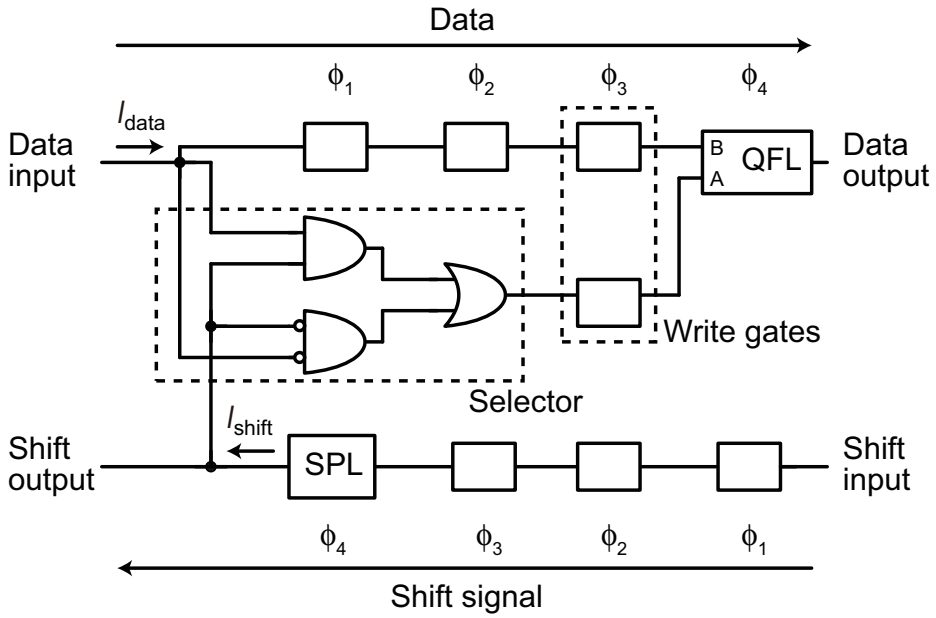


Figure 5.4: Block diagram of a shift register using a QFL, driven by four-phase excitation currents. The phase numbers are ϕ_1 through ϕ_4.

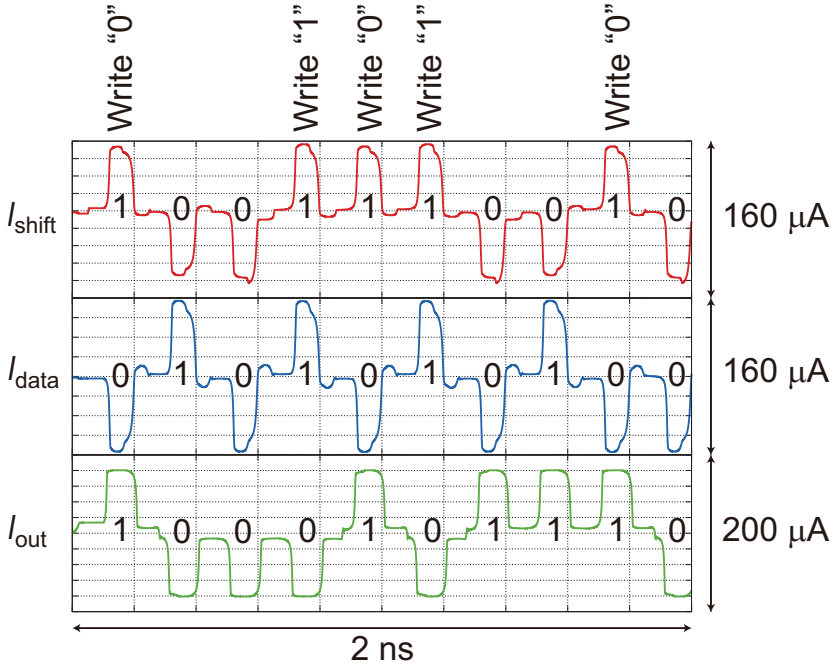
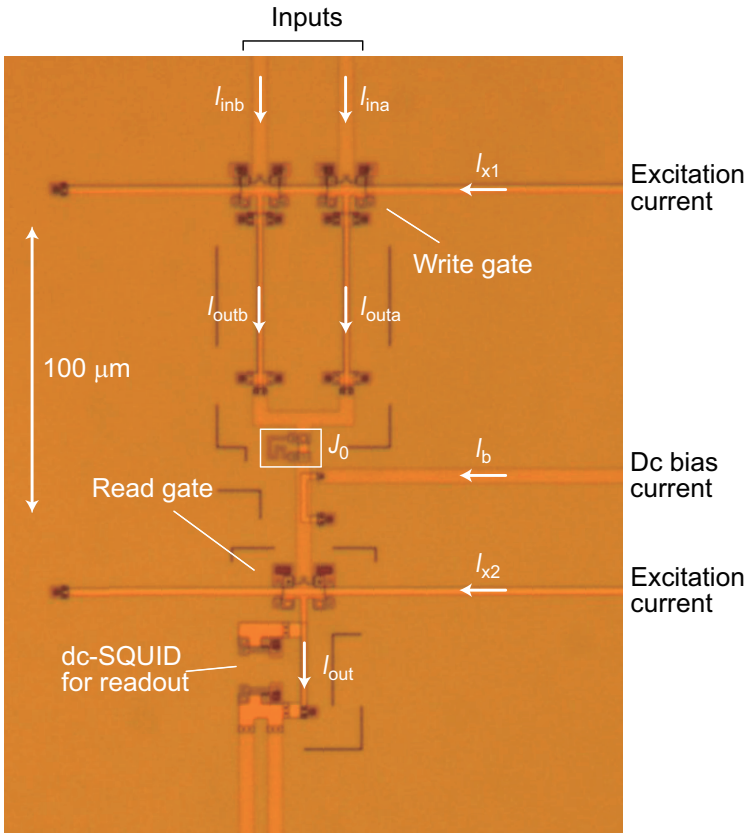


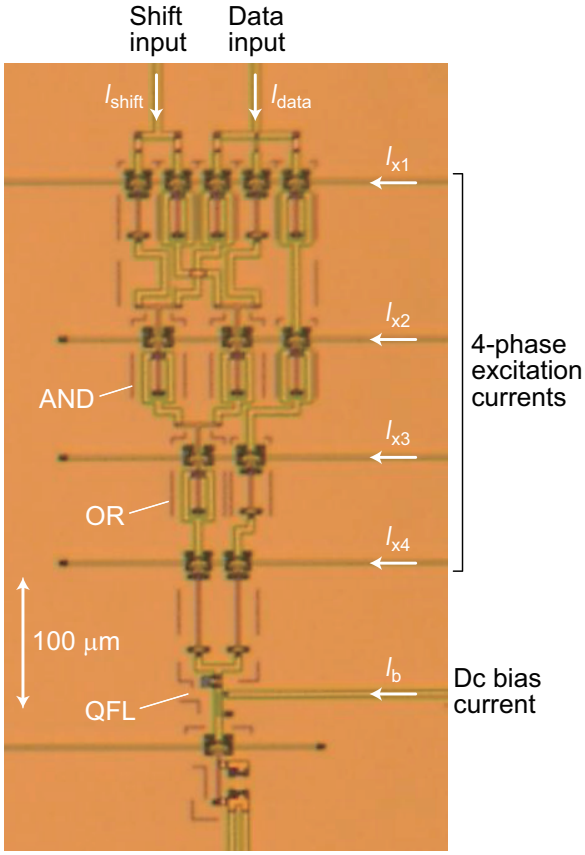
Figure 5.5: Transient analysis of the shift register operating at 5 GHz. When the shift signal is "1", the shift register latches the data of the neighbor shift register.

5.3 Experimental demonstration

We designed and fabricated the QFL and the 1-bit shift register using the STP2, where the inductance extractor, InductEx, was used through layout design. Figure 5.3 shows the micrographs of these circuits. A dc-SQUID was used to read out the states of the gate, which enters a voltage state depending on the logic state of the gate. Figure 5.7 shows the measurement setup for a low-speed test. Figure 5.8 shows the measurement results obtained using four-phase excitation currents (I_{x1} through I_{x4}) at 100 kHz, where V_{out} is the output voltage of the dc-SQUID and I_{sq} is the bias current to the dc-SQUID. Here, I_{sq} is ac in order to reduce the backaction to other gates. Comparison of the measurement results with the simulation results shown in Fig. 5.2 and 5.5 reveals that both circuits operated correctly. Table 5.2 shows the measured bias margins. In both circuits, the obtained margins of I_b were ±2%, which is much smaller that that for the simulation results, i.e, ±22%, which is believed to be due to the critical current density of the fabricated chips being higher than expected. Also, the margins of each excitation current for the shift register were small. This is because the write gates were not optimized to be combined with other AQFP gates.


Inputs
I_{inb}
I_{ina}
I_{x1}
Excitation current
Write gate
I_{outb}
I_{outa}
100 μm
J_0
I_b
Dc bias current
Read gate
I_{x2}
Excitation current
dc-SQUID for readout
I_{out}

(a)



(b)

Figure 5.6: Micrographs of the fabricated circuits. (a) QFL. A dc-SQUID was used to read out the state of the gate. (b) 1-bit shift register.

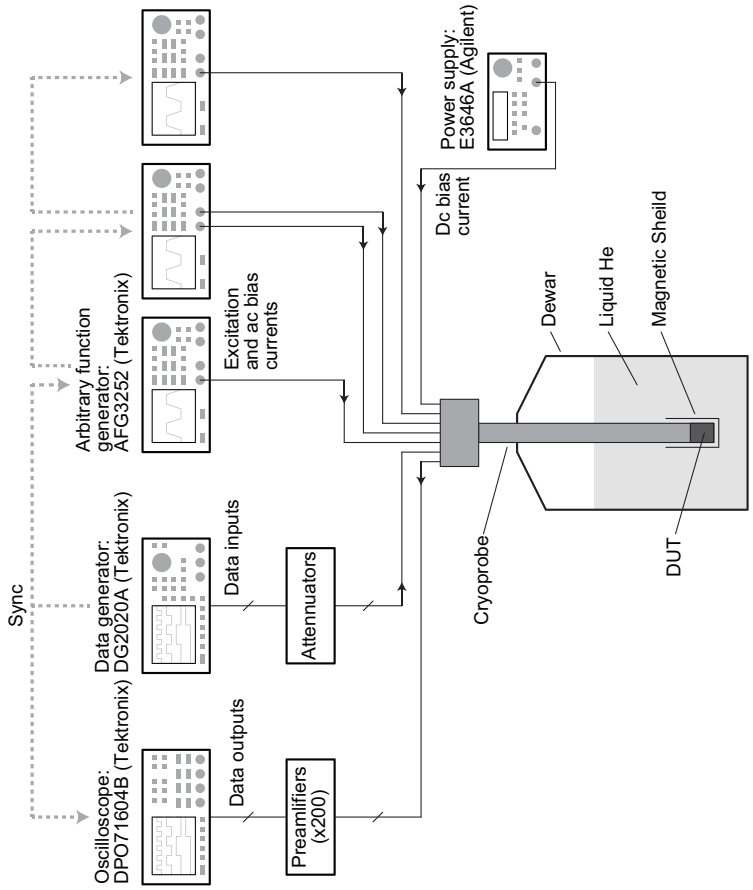
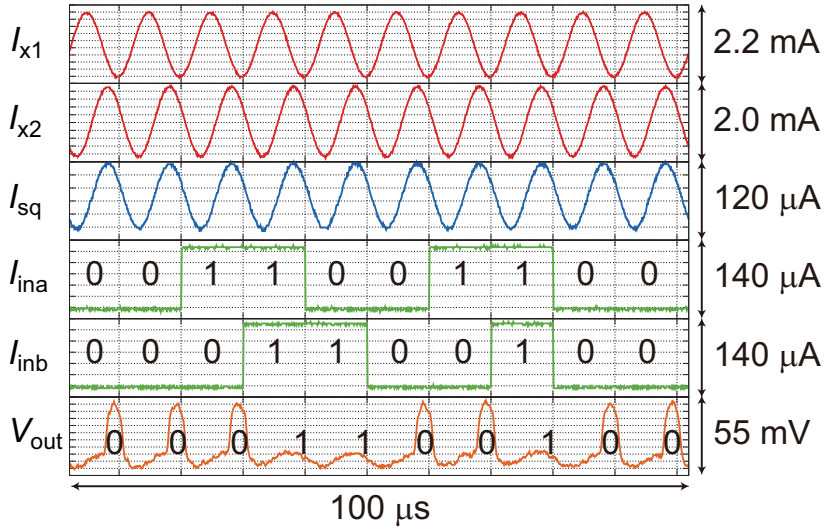
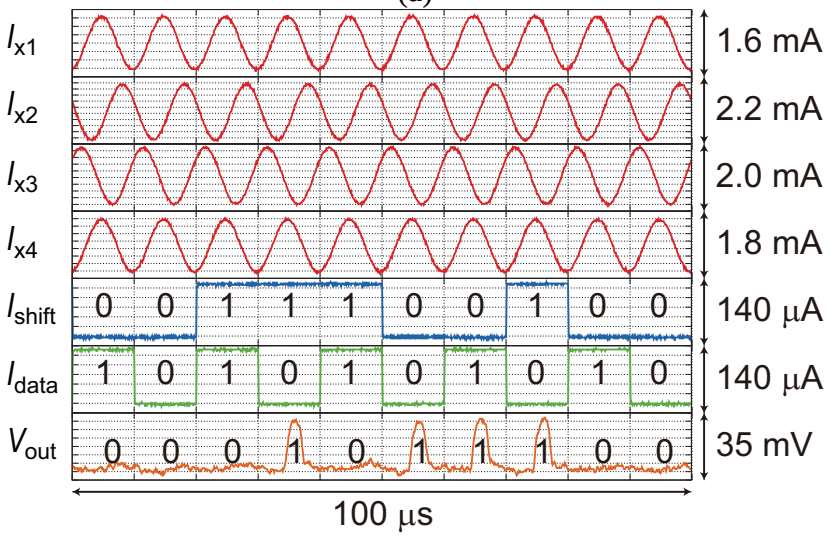


Figure 5.7: Measurement setup for a low-speed test.



(a)



(b)

Figure 5.8: Measurement results at 100 kHz. (a) QFL. Because of the coupling direction between the QFL and the dc-SQUID, the dc-SQUID turns into a voltage state when the state of the QFL is “0”. (b) 1-bit shift register. The dc-SQUID turns into a voltage state when the state of the QFL is “1”.

Table 5.2: Measured bias margins of the QFL and the shift register

	QFL	Shift register
I_{x1}	-	±7.9%
I_{x2}	±38.5%	±15.4%
I_{x3}	-	±6.7%
I_{x4}	-	±1.4%
I_{sq}	±18.7%	±18.4%
I_b	±1.9%	±1.9%

5.4 High-speed demonstration of AQFP logic gates using QFLs

5.4.1 QFL-based high-speed test circuits

Here we propose a high-speed test circuit using QFLs and experimentally demonstrate high-speed logic operations of AQFP gates. To demonstrate AQFP circuits at high speed (in the GHz range), we use QFLs to hold and read out data. Figure 5.9 shows the schematic of the modified QFL for the high-speed tests, where critical currents of the write gates are larger than those of the previous QFLs in order to reduce backactions and increase bias margins. Figure 5.10 shows the block diagram of a QFL-based high-speed test circuit (QHTC), where circuits under test (CUTs) are driven by high-speed excitation currents, I_{xhi}, and the QFLs and readout buffers are driven by low-speed excitation currents, I_{xlo1} and I_{xlo2}, respectively. Three-phase high-speed excitation currents, I_{xhi1}, I_{xhi2}, and I_{xhi3}, are generated by using a power divider, which also adds a dc-offset to each excitation current, and are terminated by on-chip 50 Ω resistances. Before the QFLs are driven by I_{xlo1}, low-speed inputs are fixed and the output data of the CUTs are stored in the storage loops of the QFLs after split by SPL gates. Although the CUTs switch at every cycle of the high-speed excitation currents, the stored data can be latched by the QFLs when I_{xlo1} rises without timing synchronization between the low-speed inputs and the high-speed excitation currents. The latched data are read out at low speed by using dc-SQUIDs, where we inserted the readout buffers to reduce backactions from the dc-SQUIDs to the QFLs. The dc-SQUIDs turn into voltage states when the states of the readout buffers are “1”.

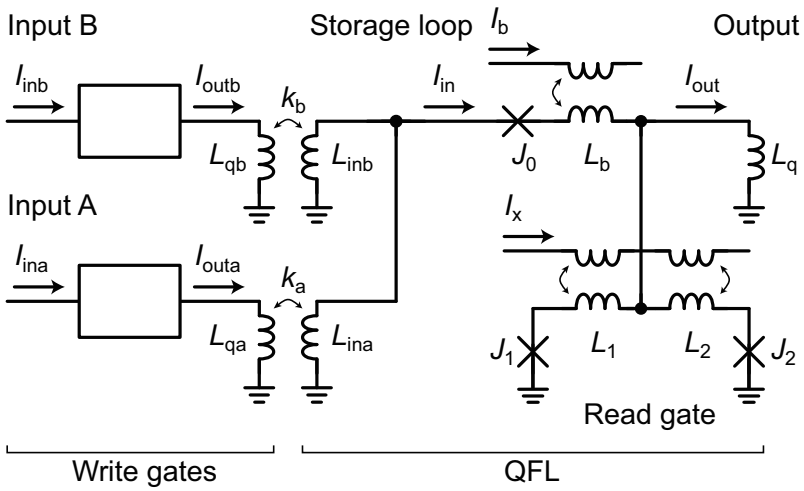


Figure 5.9: Circuit schematic of the QFL used in QHTCs. $J_0 = 40\,\mu$A or $30\,\mu$A ($\beta_c = 4.0$), $L_{ina} = L_{inb} = 22.9$ pH, $L_b = 2.86$ pH, and $k_a = k_b = 0.482$. For the write gates, $\beta_L = 0.4$, $\beta_q = 5.5$, and $I_c = 100\,\mu$A ($\beta_c = 1.0$). For the read gate, $\beta_L = 0.4$, $\beta_q = 3.2$, and $I_c = 100\,\mu$A ($\beta_c = 1.0$).

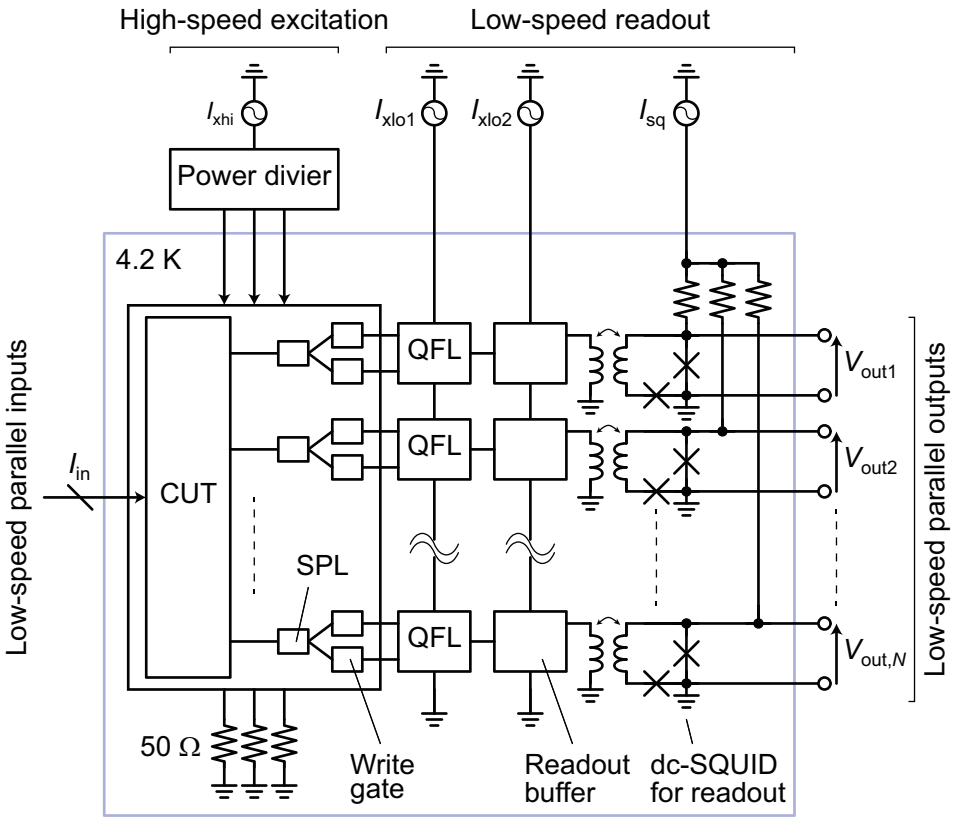


Figure 5.10: Block diagram of a QHTC. The output data of the CUT operating at high speed are stored in QFLs and read out at low speed. dc-SQUIDs are used to read out the internal states of QFLs.

5.4.2 Measurement results

We designed three types of QHTCs, α, β, and γ, by means of the InductEx and fabricated QHTCs using the STP2. In α, the CUT is a buffer gate, and the QFL has $J_0 = 40\,\mu$A. In β, the CUT is a buffer gate, and the QFL has $J_0 = 30\,\mu$A. In γ, the CUT is an AND gate, and the QFL has $J_0 = 40\,\mu$A. We used two J_0 settings because J_0 and I_b are the critical parameters in a QFL. Figure 5.11 shows the micrograph of these three QHTCs.

Figure 5.12 shows the measurement setup for the high-speed test. Figure 5.13 shows the high-speed measurement results at 1 GHz, where we applied ac bias currents, I_{sq}, to the dc-SQUIDs in order to reduce backactions to the readout buffers, and V_{out} is the output voltage of the dc-SQUIDs amplified by 200 times through the use of differential amplifiers. Figure 5.13a shows the three-phase high-speed excitation currents at 1 GHz generated by a power divider, where the small oscillations are due to reflections between the power divider and an oscilloscope. Figure 5.13b shows the measurement results for α, and Fig. 5.13c shows the measurement results for γ. In both α and γ, the CUTs operated correctly at 1 GHz. We also confirmed correct operations in β at 1 GHz. The bandwidth of the probe that we used was $\sim 1\,$GHz, which prevented demonstrations at a higher frequency.

Table 5.3 shows the obtained margins for each bias current. Here, I_{xhi} has wide bias margins of more than ±30% in all QHTCs, and I_b has a small margin of only ±5.3% in α, which is much smaller than the simulation results of ±17%. We believe that this is because J_0 was larger than the designed value in this fabrication. In fact, in β with smaller junctions, the measured margin increased to ±16%. Therefore, we can obtain reasonably wide margins of I_b by reducing the junction size of J_0, even if the parameter variation is larger than expected.

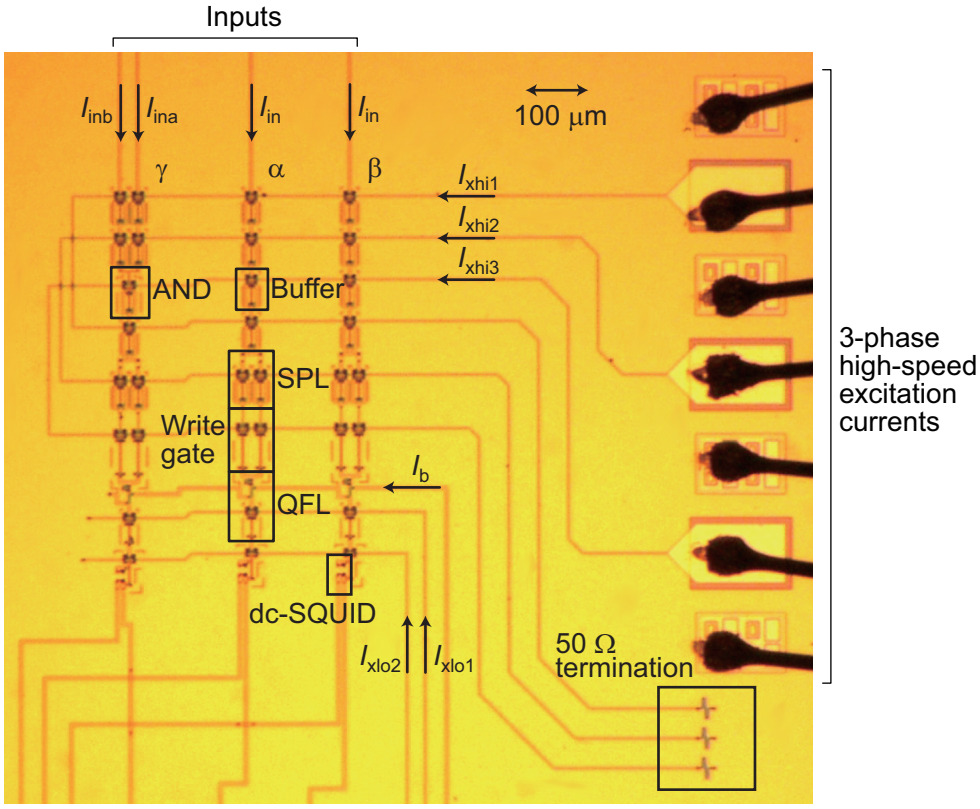


Figure 5.11: Micrograph of QHTCs. The three-phase high-speed excitation currents, I_{xhi}, are externally provided and terminated by the on-ship 50 Ω resistances.

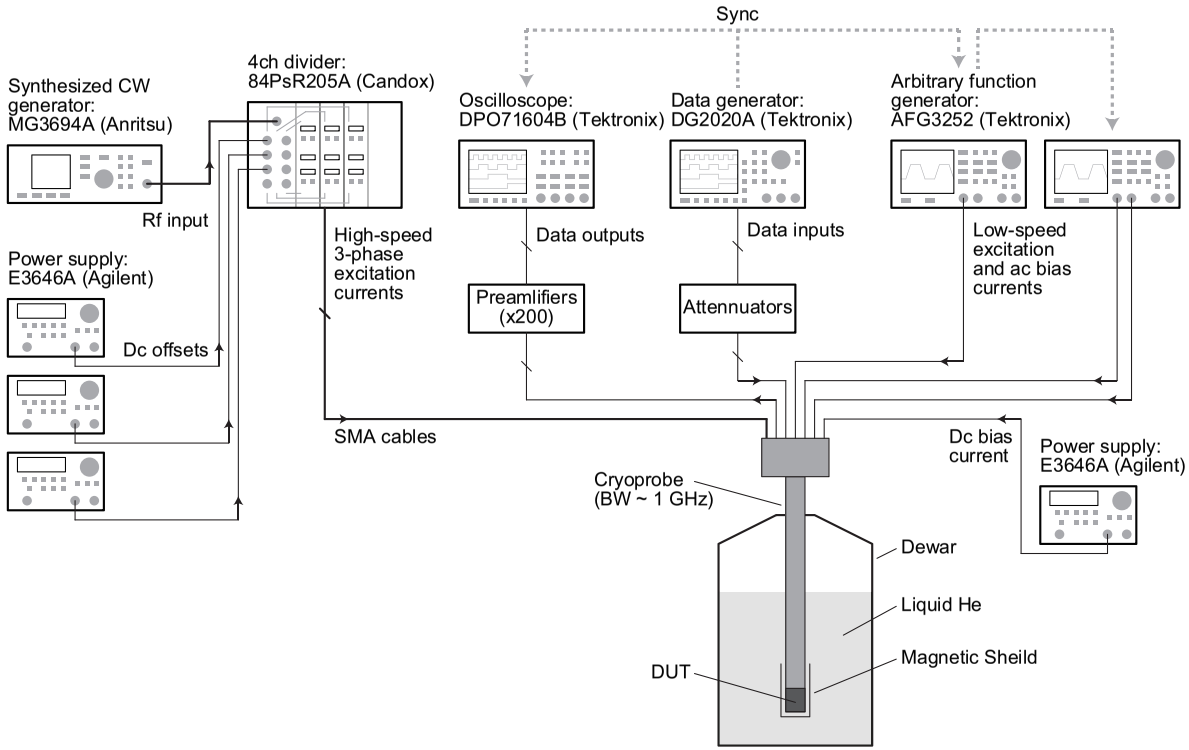


Figure 5.12: Measurement setup for a high-speed test.

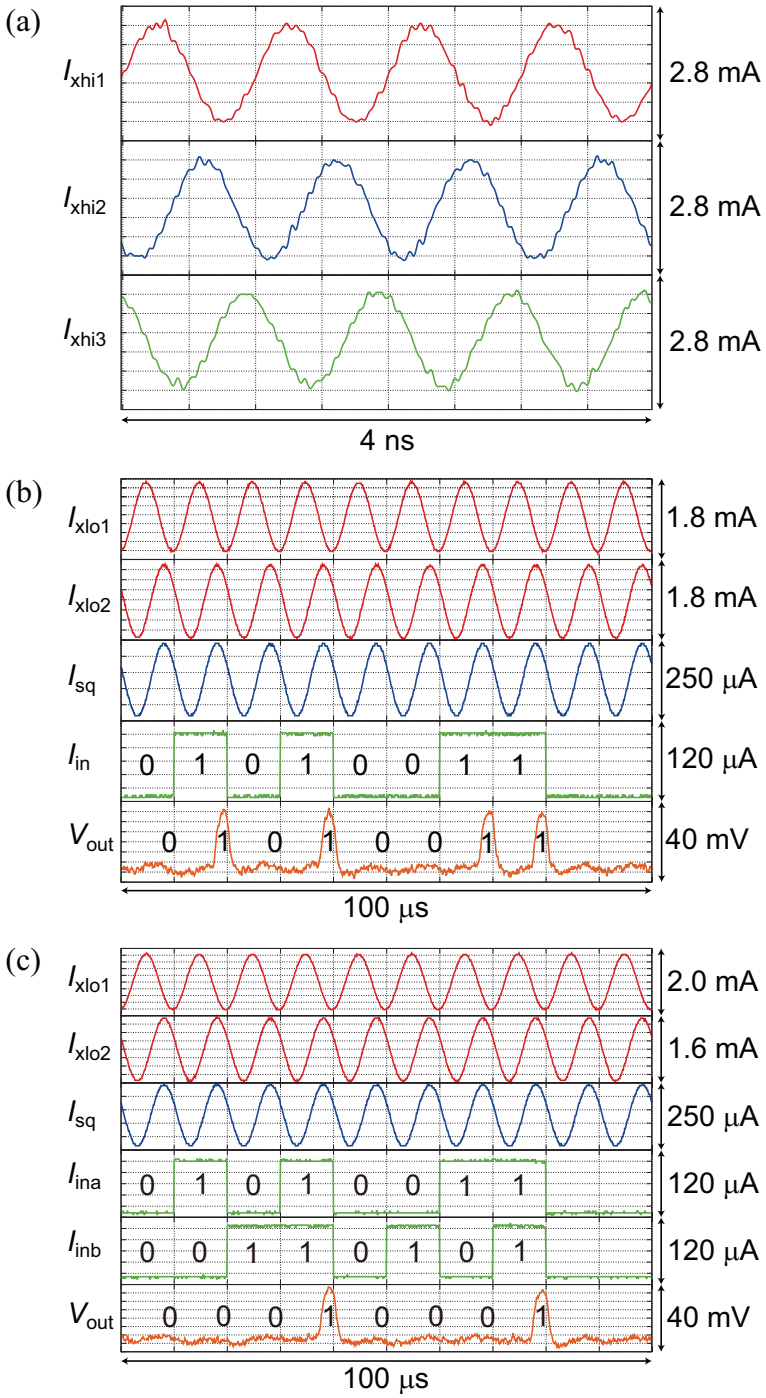


Figure 5.13: High-speed measurement results at 1 GHz. (a) Three-phase excitation currents at 1 GHz generated by a power divider. (b) α: the CUT is a buffer gate. (c) γ: the CUT is an AND gate.

Table 5.3: Measured bias margins of each QHTC

	α	β	γ
I_{xhi}	±31.0%	±34.9%	±31.0%
I_{xlo1}	±43.8%	±37.2%	±45.0%
I_{xlo2}	±31.2%	±30.7%	±27.5%
I_{sq}	±18.1%	±15.8%	±17.4%
I_{dc}	±5.3%	±16.2%	±6.3%

5.5 Summary

We proposed the QFL, which is composed of an AQPF buffer gate with a storage loop, as a novel latch for AQFP logic. The QFL is compact and compatible with AQFP logic gates and can be read or written in only one clock cycle. We simulated the QFL operating at 5 GHz, and margin analysis revealed that the QFL has wide parameter margins, where the critical parameter is the dc bias currents with a margin of ±22%. The calculated energy dissipation was only $\sim$ 0.1 aJ/bit and the obtained EDP was 20 aJ $\cdot$ ps, which is approximately 100 times smaller than that of RSFQ shift registers. Moreover, we designed and simulated a shift register operating at 5 GHz, using QFLs. We designed and fabricated the QFL and the 1-bit shift register using the STP2. Finally, we successfully demonstrated the correct operation of these circuits. From these results, we have achieved the first solution to data storage in AQFP logic circuits.

Also, we proposed the QHTC as a high-speed test circuit for AQFP logic gates, where output data of CUTs, operating at high speed, are stored in QFLs and read out at low speed. We experimentally demonstrated the high-speed operation of AQFP buffer gates and AND gates at 1 GHz. Obtained margins of high-speed excitation currents were more than ±30%, which is wide enough for practical systems using AQFP logic gates. The margin of the dc bias currents to QFLs was smaller than expected but increased to ±16% by reducing the size of junctions in QFLs.

Chapter 6

Conclusion

In Chap. 2, we numerically and experimentally demonstrated the sub-$I_c\Phi_0$ bit-energy operation. Through numerical analyses, the bit energy of an AQFP gate with critically damped junctions was estimated to be $6.40\,\mathrm{zJ} = 0.06 I_c\Phi_0 = 110 k_B T$ at 4.2 K for $\beta_L = 0.2$, $\beta_q = 1.6$, $I_c = 50\,\mu\mathrm{A}$ ($\beta_c \sim 1$) and a rise/fall time of 200 ps. The calculated bias margin at 4.2 K was ±19.4%, where the bias margin was defined as the bias region where the BER is smaller than 10^{-23}. Additionally, we measured the energy dissipation of the gate by using the superconducting resonator-based method. The bit energy was only $\sim 10\,\mathrm{zJ} \sim 0.1 I_c\Phi_0$ for $\beta_L = 0.4$, $\beta_q = 1.6$, $I_c = 50\,\mu\mathrm{A}$ ($\beta_c \sim 1$), and an operation frequency of 5 GHz. These results show that the AQFP gates can operate with bit energy smaller than its energy barrier, $I_c\Phi_0$, which is one of the most important advantages of adiabatic switching operations.

In Chap. 3, we numerically demonstrated the sub-$k_B T$ bit-energy operation. By using underdamped junctions, the bit energy reaches $12\,\mathrm{yJ} \sim 0.2 k_B T$ at 4.2 K for $\beta_L = 0.2$, $\beta_q = 1.6$, $I_c = 50\,\mu\mathrm{A}$ ($\beta_c \sim 2600$), and a rise/fall time of 2000 ps, which agreed well with analytical estimation. The calculated bias margin at 4.2 K was ±21.7%. Also, we confirmed that the BER does not change as the rise/fall time increases and bit energy decreases. These results show that there is no minimum energy dissipation for operations of AQFP gates, unless the entropy decreases. Moreover, we confirmed that the energy-time uncertainty relation can be neglected for the current design parameters.

In Chap. 4, we built the purely reversible logic gate, which we designated as the RQFP gate. The RQFP gate has a symmetric circuit topology, which is composed of three 3-in MAJ gates and three 3-out SPL gates. We confirmed that there is no minimum energy dissipation for reversible logic operations using RQFP gates, through numerical analyses. Moreover, we experimentally demonstrated the logical and physical reversibility of the gate. To the best of our knowledge, the RQFP gate is the first practical reversible logic gate. Detailed discussions on the energy efficiency of reversible computing will be possible by using RQFP gates.

In Chap. 5, we proposed the novel energy-efficient latch, which we designated as the QFL. The QFL is composed of only three junctions and is compatible with other AQFP logic gates. Also, it requires only one clock cycle for both read and write, which is a great advantage over previously proposed latches. The energy dissipation was numerically estimated to be ~ 0.1 aJ, which achieves quite a low EDP of 20 aJ $\cdot$ ps. We experimentally demonstrated the correct operations of the QFL and the 1-bit shift register using QFLs. Also, we proposed the high-speed test circuits using QFLs, with which we demonstrated AQFP buffer gates and AND gates at 1 GHz with sufficiently wide bias margins.

From the above results, we have successfully shown the extremely high energy efficiency of the AQFP logic. Especially in Chap. 4, we reached a very important conclusion that there is no minimum energy bound for logic operations using purely reversible devices. It can be expected that low-power computing systems with bit energy around k_BT will be possible by using AQFP logic.

6.1 Future works

In order to achieve practical computing systems using AQFP logic, much effort is still needed. Below are the challenges to be overcome.

Interconnects Because input currents decrease as wiring inductances increase, it is difficult to interconnect AQFP gates using long wires. Therefore, PTL drivers for AQFP gates, which convert output currents of AQFP gates into SFQ pulses, are necessary for long interconnections [Ortlepp13].

Architectures Although energy dissipation of QFLs is much smaller than RSFQ shift registers, it still costs much energy to hold data in comparison with executing logic operations. Hence, we need to conceive an architecture suitable for computing using AQFP logic, which is expected to need more logic gates but less cashes and memory bandwidth. Large-scale reconfigurable data-paths (LSRDPs) [Takagi08] might be well suitable, because it does not need cashes and large memory bandwidth. Logic-in-memory architectures such as MAGIC cells [Semenov13] could be also possible candidates.

On-chip ac power sources One of the problems of ac excitation is that bandwidth of off-chip interconnects could limit the maximum operation frequency. Another difficulty is that signal attenuation and phase delay on excitation lines due to AQFP gates could limit circuit density, which would be even more serious in multi-chip modules. In order to deal with these problems, on-chip ac power sources using relax-

ation oscillators and superconducting resonators have been proposed [Mukaiyama13a, Mukaiyama13b, 向山 13]. However, its energy efficiency is too large for energy-efficient computing systems; power consumption of the ac power source is approximately 100 times larger than that of power available for driving AQFP gates. Thereby, more energy-efficient ac power sources are needed.

Reduction in latency As described in Chap. 1, latency of AQFP logic is large because it can perform only one logic operation per clock cycle. Therefore, new operation modes to reduce latency should be conceived. Otherwise, good architectures or applications, where large latency is allowable, are necessary.

Appendix A

Potential energy of rf-SQUIDs

Because superconducting-quantum-interference-devices (SQUIDs) are the building blocks in most superconductor logics, it is important to understand how it achieves a bi-stable state, or double-well potential. Here we take an rf-SQUID as an example, because it includes only one Josephson junction and easy to analyze. Figure A.1 shows the circuit schematic of an rf-SQUID composed of a Josephson junction, J, and an inductance, L. Its potential energy, U, includes energy stored in a Josephson junction, U_j, and that stored in an inductance, U_L, as follows:

$$U = U_j + U_L. \tag{A.1}$$

We apply a bias current, I_b, and a control flux, Φ_{con}, to change the potential, using a mutual inductance, M, and a control current, I_{con}. Current through J, I_j, current through L, I_L, phase difference through J, θ, and phase difference through L, $\theta_L + \theta_{con}$, are defined as follows:

$$\frac{I_j}{I_c} = \sin\theta, \tag{A.2}$$

$$I_j + I_L = I_b, \tag{A.3}$$

$$\frac{\theta_L}{2\pi} = \frac{\Phi_L}{\Phi_0} = \frac{LI_L}{\Phi_0}, \tag{A.4}$$

$$\frac{\theta_{con}}{2\pi} = \frac{\Phi_{con}}{\Phi_0} = \frac{MI_{con}}{\Phi_0}, \tag{A.5}$$

$$\theta - \theta_L - \theta_{con} = 0, \tag{A.6}$$

where I_c is a critical current and Eq. (A.6) shows the flux quantization. From the above equations, each phase difference is described as follows:

$$\begin{aligned} \sin\theta &= -\frac{\Phi_0}{2\pi LI_c}\left(\theta_L - \frac{2\pi LI_c}{\Phi_0}\frac{I_b}{I_c}\right) \\ &= -\frac{1}{\beta_L}(\theta_L - \theta_b) = -\frac{1}{\beta_L}\theta'_L, \end{aligned} \tag{A.7}$$

where the normalized inductance, β_L, phase difference due to I_b, θ_b and effective phase difference through L, θ'_L, are given by:

$$\beta_L = \frac{2\pi L I_c}{\Phi_0}, \tag{A.8}$$

$$\theta_b = \beta_L \frac{I_b}{I_c}, \tag{A.9}$$

$$\begin{aligned} \theta'_L &= \theta_L - \theta_b \\ &= \theta - \theta_{con} - \theta_b. \end{aligned} \tag{A.10}$$

U_j and U_L are given by:

$$U_j = E_j(1 - \cos\theta), \tag{A.11}$$

$$\begin{aligned} U_L &= \frac{1}{2} L I_L'^2 = \frac{1}{2} L \left(\frac{\theta'_L}{2\pi L} \Phi_0 \right)^2 \\ &= \frac{1}{2} \frac{I_c \Phi_0}{2\pi} \frac{\Phi_0}{2\pi L I_c} \theta_L'^2 = \frac{E_j}{2\beta_L} \theta_L'^2, \end{aligned} \tag{A.12}$$

where the effective current through L, I'_L, and the Josephson energy, E_j, are given by:

$$I'_L = \frac{\theta'_L}{2\pi L} \Phi_0, \tag{A.13}$$

$$E_j = \frac{I_c \Phi_0}{2\pi}. \tag{A.14}$$

As a result, potential energy and junction currents are given as follows:

$$\frac{U}{E_j} = \frac{1}{2\beta_L} (\theta - \theta_{con} - \theta_b)^2 + 1 - \cos\theta, \tag{A.15}$$

$$\frac{I_j}{I_c} = \sin\theta = -\frac{1}{\beta_L} (\theta - \theta_{con} - \theta_b). \tag{A.16}$$

Figure A.2 shows the time sequence of potential energy and junction currents when an SFQ is stored in an rf-SQUID, using Eqs. (A.15) and (A.16) for $\beta_L = 2\pi$ ($LI_c = \Phi_0$). Maxima and minima of the potential correspond to the intersections of sin curves ($\sin\theta$) and load curves ($-(\theta - \theta_{con} - \theta_b)/\beta_L$) of junction currents. When I_b and Φ_{con} are 0, the shape of the potential is a single well (Fig. A.2a). As I_b or Φ_{con} increases, it varies to a double well, which enables two distinguishable states (Fig. A.2b). Finally, it varies to a single well again ($I_j = I_c$), which induces rapid and irreversible state transition (Fig. A.2c). As a result, an SFQ is stored in the rf-SQUID. Note that I_b and Φ_{con} have the same impacts on this process for $\beta_L = 2\pi$. During this non-adiabatic process, switching energy, E_{sw} ($\sim I_c \Phi_0$), is dissipated. Correctly speaking, as can be seen in

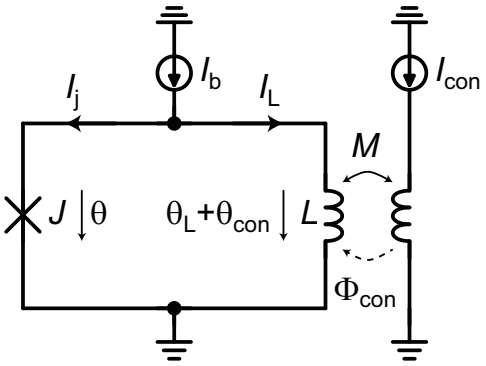


Figure A.1: Circuit schematic of an rf-SQUID.

Figs. A.2b and c, the barrier height, E_b ($\sim E_j = I_c\Phi_0/2\pi$), is not equal to E_{sw} in most superconductor logics. However, in this study we assume that $E_{sw} = E_b = I_c\Phi_0$ for simplicity as described in Chap. 1, because it does not make a difference in our discussion on physical energy bounds. Figure A.3 shows the time sequence when an SFQ escapes from the rf-SQUID.

In order to use an rf-SQUID in logic devices, it must have two distinguishable states of "0" and "1". Therefore, SQUIDs are biased in most superconductor logics so that it can achieve bi-stable states, by applying bias currents or control fluxes. Figure A.4a shows double-well potential for $\beta_L = 2\pi$ and $I_b/I_c = 0.5$ or $\Phi_{con}/\Phi_0 = 0.5$, where the two states have the same potential energy. Figure A.4b shows the dependence of phase differences on bias currents or control fluxes for $\beta_L = 2\pi$. It can be seen that each state can switch to the other from the bias point ($I_b/I_c = 0.5$ or $\Phi_{con}/\Phi_0 = 0.5$) by applying the same magnitude of energy, which indicates that the rf-SQUID can be used as a digital switch. Moreover, β_L determines the hysteresis of the θ-I_b or θ-Φ_{con} curves. As β_L (or LI_c) increases, the state becomes more stable with a larger barrier height and a larger operation margin (bias margin) but needs more energy and time for a switching event. Therefore, in superconductor logics, it is important to optimize LI_c products in terms of energy, speed, and operation margins.

In conventional superconductor logics, dc-SQUIDs, which include two Josephson junctions in a SQUID loop, are used as building blocks rather than rf-SQUIDs. However, the behaviors of potential energy and SFQs are the same, whether the building block is an rf-SQUID or a dc-SQUID. The detailed analysis on potential energy of dc-SQUIDs have been reported in [Ortlepp07].

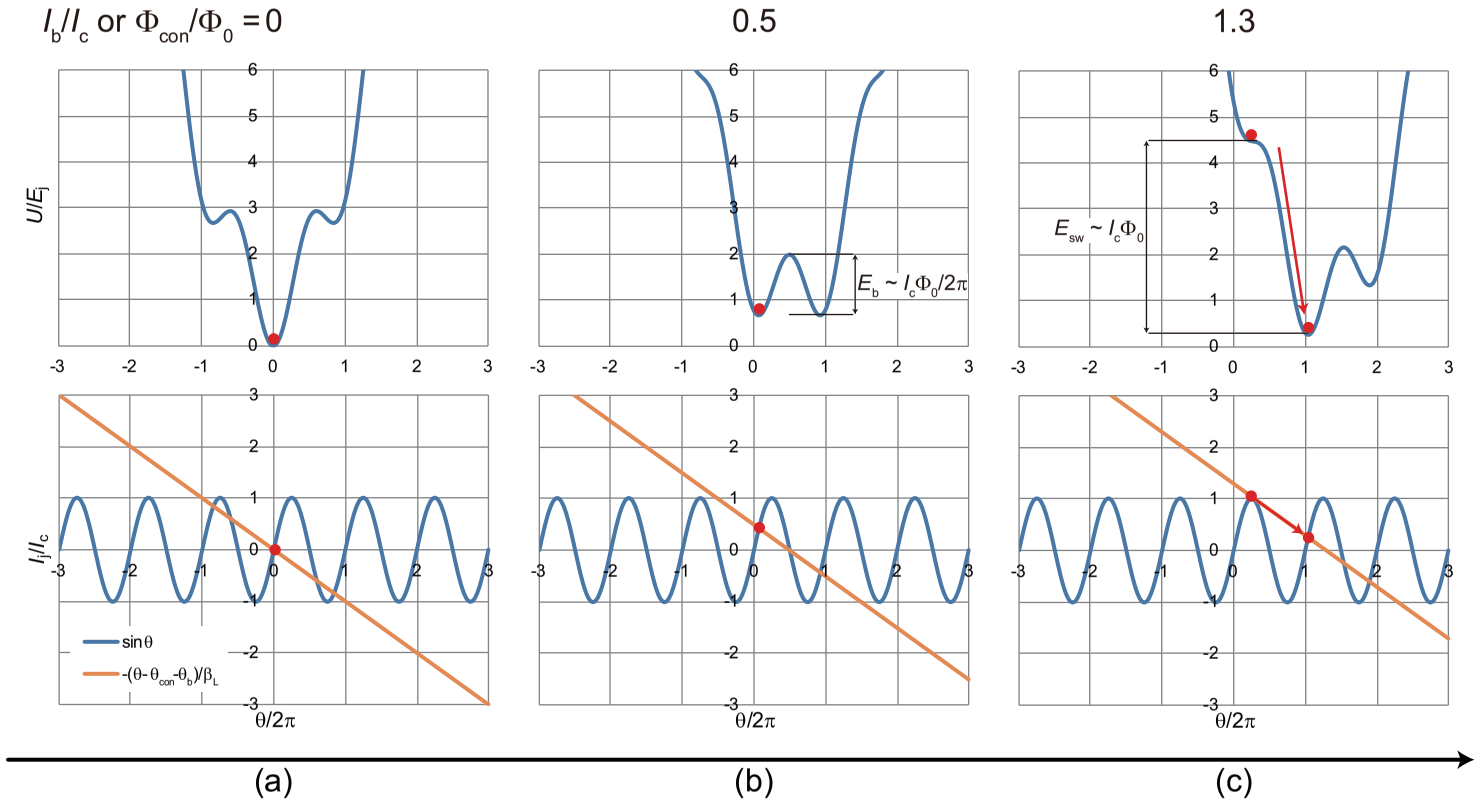


Figure A.2: Time sequence of the potential energy of an rf-SQUID while an SFQ is being stored ($\beta_L = 2\pi$).

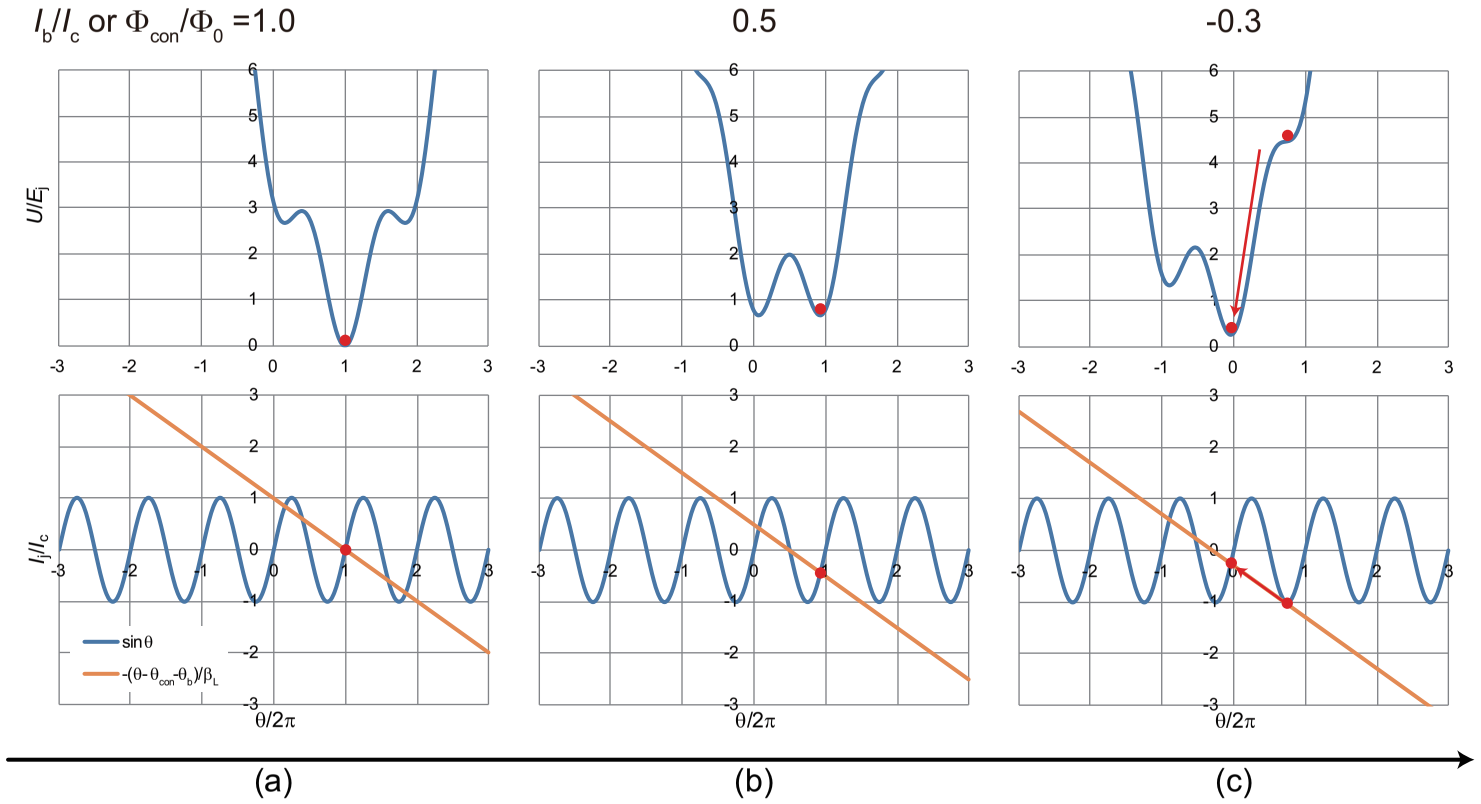


Figure A.3: Time sequence of the potential energy of an rf-SQUID while an SFQ is escaping ($\beta_L = 2\pi$).

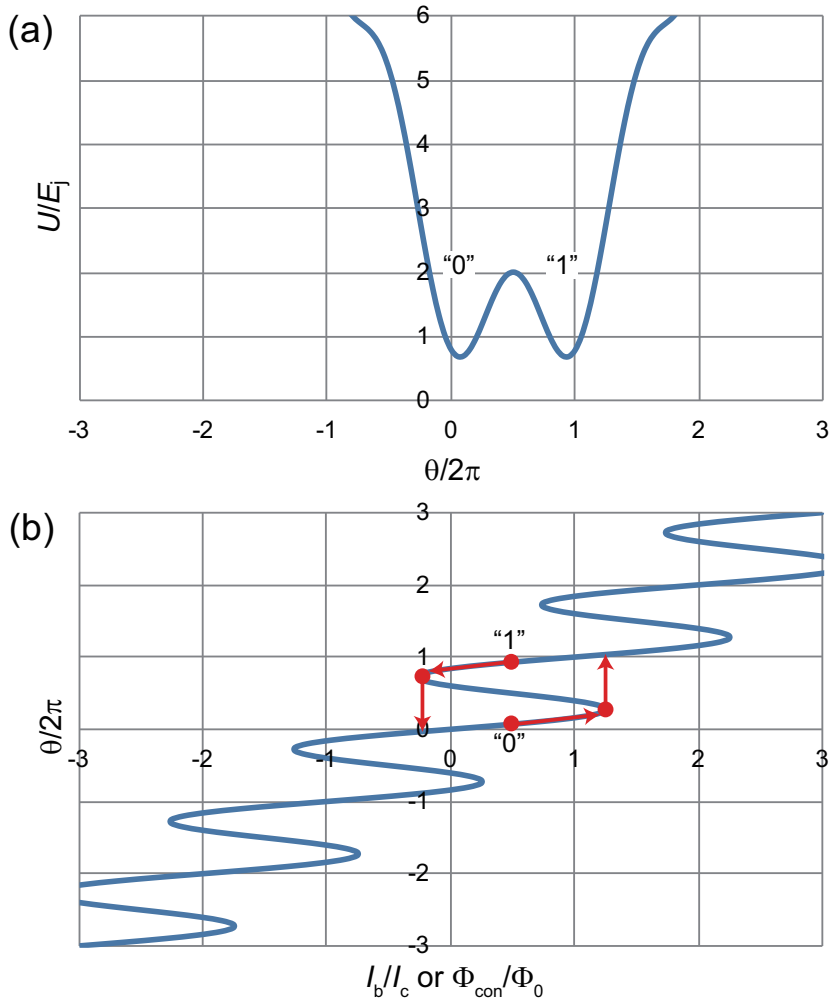


Figure A.4: Bi-stable states for digital applications. (a) Double-well potential energy for $\beta_L = 2\pi$. $I_b/I_c = 0.5$ or $\Phi_{con}/\Phi_0 = 0.5$. (b) Phase difference for $\beta_L = 2\pi$.

Appendix B

Transient analysis of *RLC* circuits

Because Josephson junctions can be treated as a parallel resonator, as will be shown in App. C, it it important to understand the transient response of *RLC* circuits. Figure B.1 shows the schematic of an *RLC* series circuit. The transient response of this circuit is given by the following differential equation:

$$Eu(t) = Ri + \frac{1}{C}\int i\mathrm{d}t + L\frac{\mathrm{d}i}{\mathrm{d}t}. \tag{B.1}$$

If we assume that $i = \mathrm{d}i/\mathrm{d}t = 0$ for $t = 0$, the current, i, is given as follows:

$$\frac{i}{I_0} = \frac{\omega_0}{\gamma}\exp(-\alpha t)\cdot\sinh\gamma t \qquad \text{for } R > R_{cri}\,(Q < 0.5), \tag{B.2}$$

$$\frac{i}{I_0} = \omega_0\exp(-\alpha t)\cdot t \qquad \text{for } R = R_{cri}\,(Q = 0.5), \tag{B.3}$$

$$\frac{i}{I_0} = \frac{\omega_0}{\beta}\exp(-\alpha t)\cdot\sin\beta t \qquad \text{for } R < R_{cri}\,(Q > 0.5), \tag{B.4}$$

where

$$R_{cri} = 2\sqrt{\frac{L}{C}}, \tag{B.5}$$

$$Z_0 = \sqrt{\frac{L}{C}}, \tag{B.6}$$

$$I_0 = \frac{E}{Z_0}, \tag{B.7}$$

$$\omega_0 = \sqrt{\frac{1}{LC}}, \tag{B.8}$$

$$T_0 = \frac{2\pi}{\omega_0}, \tag{B.9}$$

$$\alpha = \frac{\omega_0}{2Q}, \tag{B.10}$$

$$\beta = \sqrt{\omega_0^2 - \alpha^2}, \tag{B.11}$$

$$\gamma = \sqrt{\alpha^2 - \omega_0^2}. \tag{B.12}$$

The quality factor, Q, is given by using characteristic time constants as follows:

$$\begin{aligned} Q &= \frac{\tau_1}{\tau_0} = \sqrt{\frac{\tau_1}{\tau_2}} \\ &= \frac{R_{cri}}{2R} = \frac{Z_0}{R}, \end{aligned} \tag{B.13}$$

$$\tau_0 = \frac{1}{\omega_0} = \sqrt{\tau_1 \tau_2}, \tag{B.14}$$

$$\tau_1 = \frac{L}{R}, \tag{B.15}$$

$$\tau_2 = RC, \tag{B.16}$$

$$\tau = \frac{1}{\alpha} = 2\tau_1. \tag{B.17}$$

Using Q, $\exp(-\alpha t)$ is given by:

$$\exp(-\alpha t) = \exp\left(-\frac{t}{QT_0}\pi\right), \tag{B.18}$$

which shows that the amplitude of the damped oscillation reduces to $\exp(-\pi) \sim 4\%$ for $t = QT_0$. In other words, Q indicates the number of oscillations until they converge. Thereby, high-Q circuits can store energy for a long time as long-lasting intrinsic oscillations.

The transient response of this circuit is critical damping for $Q = 0.5$, underdamping for $Q > 0.5$, and overdamping for $Q < 0.5$, as described in Eqs. (B.2), (B.3), and (B.4). For practical circuit design, it is sometimes important to determine Q so that the oscillation rises and converges the fastest. The *RLC* circuit has two time constants, $\tau_1 = L/R$ and $\tau_2 = RC$. The transient response converges the fastest for $\tau_1 = \tau_2$, which results in $Q = 1.0$. Therefore, sometimes the response for $Q = 1.0$ is also defined as critical damping. Figure B.2 shows the transient responses for different Q. It can be seen that the waveform rises and converges fast for $Q = 1.0$, and the oscillation lasts long for $Q = 5.0$.

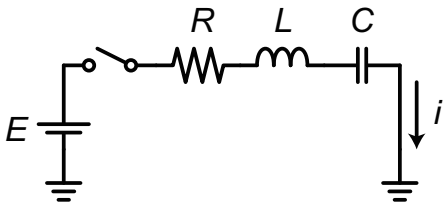


Figure B.1: Circuit schematic of an *RLC* series circuit.

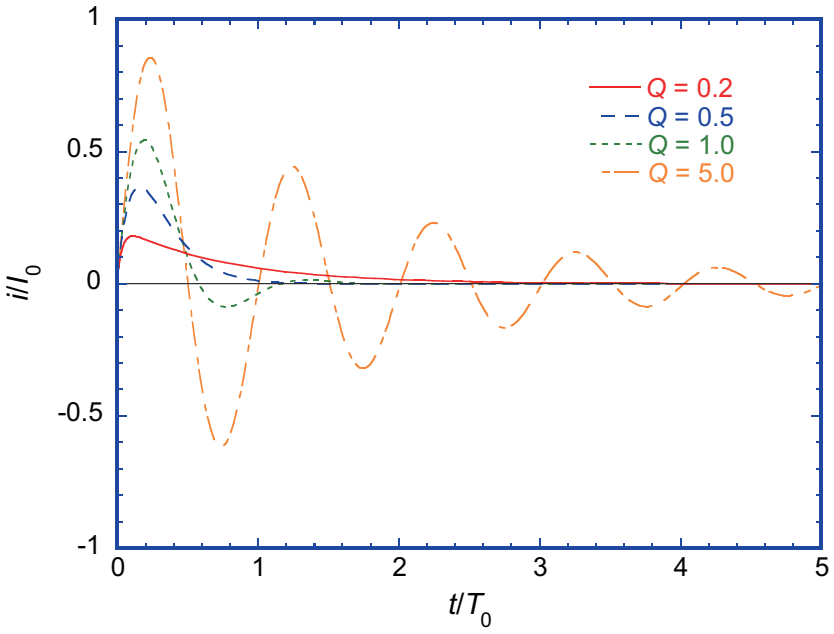


Figure B.2: Transient response of an RLC series circuit.

Appendix C

Transient analysis of Josephson junctions

The transient response of Josephson devices is determined by the quality factor of Josephson junctions, Q. Figure C.1a shows the schematic of a Josephson junction, J, shunted by the shunt resistance, R_s, which is used to adjust Q. Figure C.1b is its equivalent circuit, where Josephson junction is replaced with its CRSJ model, which is composed of Josephson inductance, L_j, junction capacitance, C, and subgap resistance, R_{sg}. A Josephson junction can be treated as a parallel resonator, which has two time constants, τ_1 and τ_2. These time constants are given by [Kadin99]:

$$\tau_1 = RC, \tag{C.1}$$

$$\tau_2 = \frac{L_j}{R}, \tag{C.2}$$

where R is the combined resistance of R_{sg} and R_s. The ratio of these time constants gives the McCmber parameter [McCumber68, Stewart68], β_c, which shows the damping condition and Q of the junction as below:

$$\begin{aligned} \beta_c = Q^2 = \frac{\tau_1}{\tau_2} = \frac{R^2 C}{L_j} \\ \approx \frac{R^2 C}{L_{j0}} = 2\pi \frac{R^2 C I_c}{\Phi_0}, \end{aligned} \tag{C.3}$$

where $L_j = L_{j0}/\cos\theta$, $L_{j0} = \Phi_0/2\pi I_c$, and θ is a phase difference of a Josephson junction. When $\beta_c = 1$ ($\tau_1 = \tau_2$), the voltage across the junction returns to zero the fastest, which corresponds to critical damping. Therefore, in conventional superconductor logics such as RSFQ, β_c is determined to be ~ 1 ($Q \sim 1$) by adding a shunt resistance, in order to achieve a very high operation frequency and small pulse interactions.

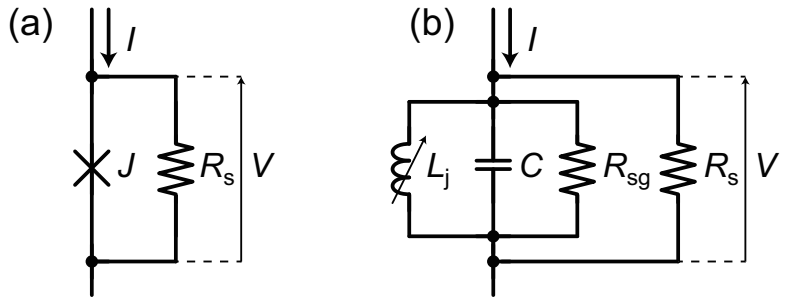


Figure C.1: (a) Circuit schematic of a Josephson junction and (b) its equivalent circuit.

Additionally, the switching time, τ_{sw}, and the pulse height, V_h, are given by using β_c, as shown below:

$$\begin{aligned}\tau_{sw} &\approx 2\pi\tau_2 \approx 2\pi\frac{L_{j0}}{R} \\ &= \frac{\Phi_0}{I_c R} = \sqrt{\frac{2\pi\Phi_0 C}{\beta_c I_c}},\end{aligned} \tag{C.4}$$

$$\begin{aligned}V_h &= \frac{\Phi_0}{2\pi}\frac{\mathrm{d}\theta}{\mathrm{d}t} \approx \frac{\Phi_0}{2\pi}\frac{2\pi}{\tau_{sw}} \\ &= I_c R \propto \sqrt{\beta_c}.\end{aligned} \tag{C.5}$$

Figure C.2 shows the transient analysis of SFQ pulses in JTLs with different β_c. For $\beta_c > 1$, the pulse shows an underdamped response with a fast rise time, a large pulse height, and a long-lasting plasma oscillation. This is because the phase difference of the junction changes fast due to the weak damping. For $\beta_c < 1$, the junction is overdamped, where the pulse height is small and plasma oscillations do not occur. Although the junction is critically damped for $\beta_c = 1.0$, there are small oscillations due to the non-linearity of Josephson inductance. Therefore, in our conventional RSFQ circuit design, β_c is designed to be 0.89 to reduce interactions between SFQ pulses.

Also, β_c determines the hysteresis of I-V characteristics of junctions. Fig. C.3 shows the I-V characteristics for critical damping ($\beta_c = 1.0$) and underdamping ($\beta_c = 4.0$). The underdamped junction shows a large hysteresis in I-V characteristics, where the voltage across the junction remains until the applied current reduces significantly. For high operation frequencies, the hysteresis should be designed to be small by using critically damped junctions.

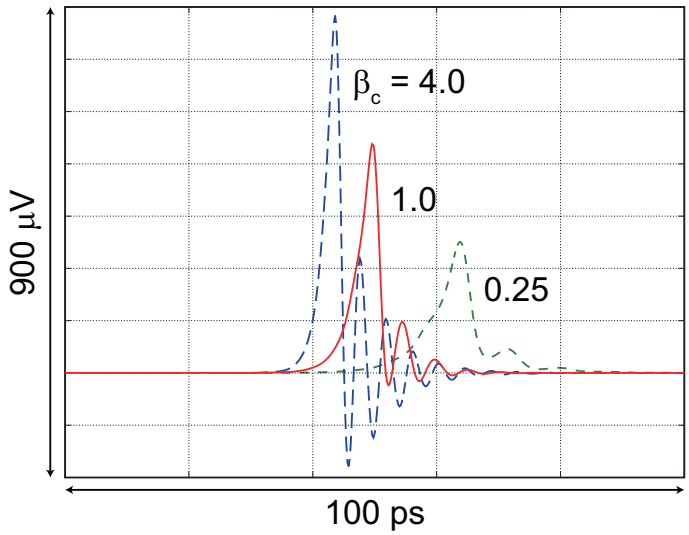


Figure C.2: Transient analysis of SFQ pulses in JTLs. The junction is critically damped for $\beta_c = 1$, overdamped for $\beta_c < 1$, underdamped for $\beta_c > 1$.

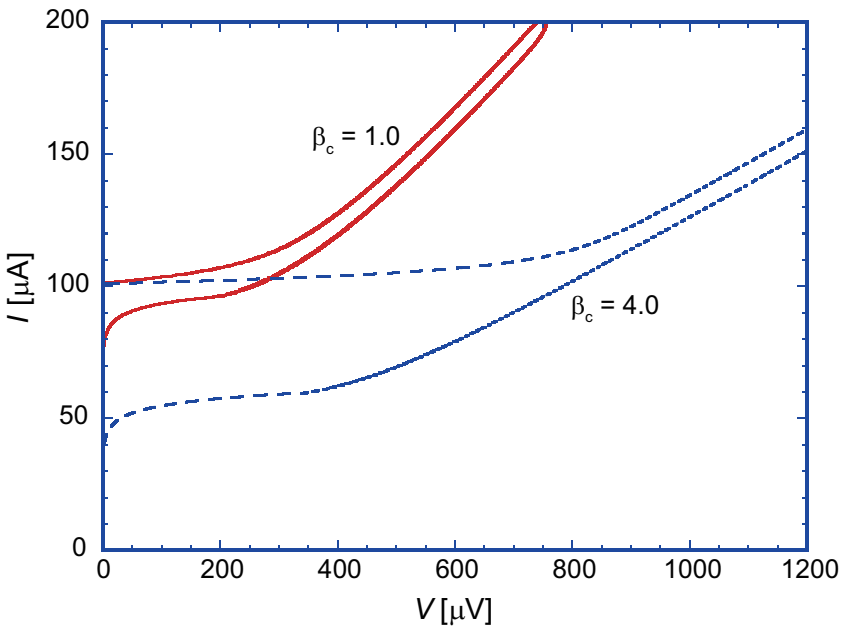


Figure C.3: *I*-*V* characteristics of Josephson junctions.

Appendix D

Scaling of conventional superconductor logic

We briefly introduce the scaling of conventional superconductor logics, such as RSFQ logic [Kadin01]. Table D.1 shows general scaling rules, using scaling factor of α. Here we take a closer look at operation frequencies. We define the pulse width of an SFQ pulse, Δt, as below:

$$\begin{aligned}\Delta t \equiv \frac{\tau_{sw}}{2} &= \frac{\Phi_0}{2I_cR} = \sqrt{\frac{\pi\Phi_0 C}{2\beta_c I_c}} \\ &= \sqrt{\frac{\pi\Phi_0 C'S}{2\beta_c J_c S}} = \sqrt{\frac{\pi\Phi_0 C'}{2\beta_c J_c}} \\ &\propto \sqrt{\frac{1}{J_c}},\end{aligned} \tag{D.1}$$

$$J_c \propto \exp(-\gamma d), \tag{D.2}$$

where C' is junction capacitance per area, J_c is critical current density, S is junction area, d is junction thickness, and γ is a constant. Equation (D.1) shows that as the critical current density increases, the pulse width becomes narrower and a higher operation frequency is achievable. This is because the gate capacitance reduces as the critical current density increases, which reduces τ_1 as a result. And Eq. (D.2) shows that larger critical current density is obtained by reducing the junction thickness. Using Eq. D.1, we estimate the operation frequency, f_{clk}, for the two available Nb processes, the STP2 with $J_c = 2.5\,\mathrm{kA/cm^2}$ [Nagasawa95] and the ADP2 with $J_c = 10\,\mathrm{kA/cm^2}$ [Nagasawa04], whose parameters are shown in Table D.2. For the STP2:

$$\Delta t \sim 2.7\,\mathrm{ps} \quad \text{for}\,\beta_c = 1.0,$$

$$f_{clk} \sim 1/10\Delta t \sim 40\,\mathrm{GHz}.$$

For the ADP2:

$$\Delta t \sim 1.4\,\text{ps} \quad \text{for}\,\beta_c = 1.0,$$

$$f_{clk} \sim 1/10\Delta t \sim 70\,\text{GHz}.$$

Furthermore, by using an extremely high critical current density of $250\,\text{kA/cm}^2$, a frequency divider operating at up to 770 GHz has been successfully demonstrated [Chen98, Chen99].

Table D.1: Scaling rules in conventional superconductor logic

Quantity	Transformation
Junction length	$a \rightarrow a/\alpha$
Junction area	$S \rightarrow S/\alpha^2$
Current	$I \rightarrow I$
Voltage	$V \rightarrow V\alpha$
Flux	$\Phi \rightarrow \Phi$
Distance on chip	$\Delta x \rightarrow \Delta x/\alpha$
Time delays	$\Delta t \rightarrow \Delta t/\alpha$
Resistance	$R \rightarrow R\alpha$
Capacitance	$C \rightarrow C/\alpha^2$
Inductance	$L \rightarrow L$
Junction/area	$N \rightarrow N\alpha^2$
Power/area	$P \rightarrow P\alpha^3$

Table D.2: Junction parameters of the STP2 and the ADP2

Quantity	STP2	ADP2
Critical current density, J_c [kA/cm^2]	2.5	10
Minimum junction area, S_{min} [μm^2]	2.0×2.0	1.0×1.0
Critical current, I_c [μA]	100 for S_{min}	100 for S_{min}
Junction capacitance, C [pF]	0.218 for S_{min}	0.064 for S_{min}
Normal-state resistance, R_n [Ω]	17 for S_{min}	16 for S_{min}
Subgap resistance, R_{sg} [Ω]	200 for S_{min}	100 for S_{min}
Gap voltage, V_g [mV]	2.8	2.7

Bibliography

[Ayala13] C. L. Ayala, “Energy-Efficient Wide Datapath Integer Arithmetic Logic Units Using Superconductor Logic”, PhD thesis, Stony Brook Univ., 2013. (Cited on page 13).

[Ball12] P. Ball, “Computer engineering: Feeling the heat.,” *Nature*, vol. 492, no. 7428, pp. 174-6, Dec. 2012. (Cited on page 1).

[Bennett73] C. H. Bennett, “Logical Reversibility of Computation,” *IBM J. Res. Dev.*, vol. 17, no. 6, pp. 525-532, Nov. 1973. (Cited on page 2).

[Berut12] A. Bérut, A. Arakelyan, A. Petrosyan, S. Ciliberto, R. Dillenschneider, and E. Lutz, “Experimental verification of Landauer’s principle linking information and thermodynamics.,” *Nature*, vol. 483, no. 7388, pp. 187-9, Mar. 2012. (Cited on page 3).

[Boechler10] G. P. Boechler, J. M. Whitney, C. S. Lent, A. O. Orlov, and G. L. Snider, “Fundamental limits of energy dissipation in charge-based computing,” *Appl. Phys. Lett.*, vol. 97, no. 10, p. 103502, 2010. (Cited on page 3).

[Borkar11] S. Borkar and A. A. Chien, “The future of microprocessors,” *Commun. ACM*, vol. 54, no. 5, p. 67, May 2011. (Cited on page 1).

[Bunyk03] P. Bunyk, M. Leung, J. Spargo, and M. Dorojevets, “A FLUX-1 RSFQ micro-processor: Physical design and test results, A FLUX-1 microprocessor and beyond,”” *IEEE Trans. Appl. Supercond.*, vol. 13, pp. 433-436, June 2003. (Cited on page 10).

[C3] Cryogenic Computing Complexity (C3) Program: `https://www.fbo.gov/index?s=opportunity&mode=form&tab=core&id=55cefaec5a3dcac236383a90951e7f71` (Cited on page 11).

[Casas91] J. Casas, R. Kamikawai, Y. Harada, N. Miyamoto, H. Nakane, and E. Goto, “Subharmonic generators and error detection by using the quantum flux parametron (QFP),” *IEEE Trans. Magn.*, vol. 27, no. 2, pp. 2851-2854, Mar. 1991. (Cited on page 14).

[Casas92] J. Casas, R. Kamikawai, and R. Goto, “High-frequency operation of quantum flux parametron (QFP) based shift registers and frequency prescalers,” *IEEE J. Solid-St. Circ.*, vol. 27, no. 1, pp. 97-105, 1992. (Cited on pages 14 and 61).

[Chen98] W. Chen, a. V. Rylyakov, V. Patel, J. E. Lukens, and K. K. Likharev, “Superconductor digital frequency divider operating up to 750 GHz,” *Appl. Phys. Lett.*, vol. 73, no. 19, p. 2817, 1998. (Cited on pages 10 and 96).

[Chen99] W. Chen, A. V. Rylyakov, V. Patel, J. E. Lukens, and K. K. Likharev, “Rapid single flux quantum T-flip flop operating up to 770 GHz,” *IEEE Trans. Appl. Supercond.*, vol. 9, no. 2, pp. 3212-3215, Jun. 1999. (Cited on pages 10 and 96).

[Chin92] C. Chin, D. Oates, G. Dresselhaus, and M. Dresselhaus, “Nonlinear electrodynamics of superconducting NbN and Nb thin films at microwave frequencies,” *Phys. Rev. B*, vol. 45, no. 9, pp. 4788-4798, Mar. 1992. (Cited on pages 17 and 27).

[Cockshott12] P. Cockshott, L. M. Mackenzie, and G. Michaelson, “Computation and Its Limits,” Oxford University Press, 2012. (Cited on page 15).

[Dillenschneider09] R. Dillenschneider and E. Lutz, “Memory Erasure in Small Systems,” *Phys. Rev. Lett.*, vol. 102, no. 21, pp. 1-4, May 2009. (Cited on page 3).

[Dorojevets01] M. Dorojevets, P. Bunyk, and D. Zinoviev, “FLUX chip: design of a 20-GHz 16-bit ultrapipelined RSFQ processor prototype based on 1.75-μm LTS technology,” *IEEE Trans. Appl. Supercond.*, vol. 11, no. 1, pp. 326-332, Mar. 2001. (Cited on page 10).

[Ehara13] K. Ehara, A. Takahashi, Y. Yamanashi, and N. Yoshikawa, “Development of Pulse Transfer Circuits for Serially Biased SFQ Circuits Using the Nb 9-Layer 1-μm Process,” *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, p. 1300504, Jun. 2013. (Cited on page 13).

[Fang89] E. S. Fang and T. Van Duzer, “A Josephson Integrated Circuit Simulator (JSIM) for Superconductive Electronics Application,” *in the extended abstracts of the 1989 international superconductivity electronics conference (ISEC’89)*, Tokyo, Japan, 1989. (Cited on page 19).

[Fourie11] C. J. Fourie, O. Wetzstein, T. Ortlepp, and J. Kunert, “Three-dimensional multi-terminal superconductive integrated circuit inductance extraction,” *Supercond. Sci. Technol.*, vol. 24, no. 12, p. 125015, Dec. 2011. (Cited on page 52).

[Fredkin82] E. Fredkin and T. Toffoli, “Conservative logic,” *Int. J. Theor. Phys.*, vol. 21, no. 3-4, pp. 219-253, Apr. 1982. (Cited on page 15).

[Fujimaki08] A. FUJIMAKI, M. TANAKA, T. YAMADA, Y. YAMANASHI, H. PARK, and N. YOSHIKAWA, “Bit-Serial Single Flux Quantum Microprocessor CORE,” *IEICE Trans. Electron.*, vol. E91-C, no. 3, pp. 342-349, Mar. 2008. (Cited on page 10).

[Fujimaki12] A. Fujimaki, “Advancement of superconductor digital electronics,” *IEICE Electron. Express*, vol. 9, no. 22, pp. 1720-1734, 2012. (Cited on page 10).

[Fung13] Y.-K.-K. Fung, G. W. Gibson, J. F. Bulzacchelli, S. Polonsky, and M. B. Ketchen, “Direct Measurement of Jitter in a JTL,” *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, p. 1701405, Jun. 2013. (Cited on page 13).

[Geist10] A. Geist, “Paving the Roadmap to Exascale,” *SciDAC Rev.*, no. 16, 2010 [Online]. Available: `http://www.scidacreview.org` (Cited on page 1).

[Goto91] E. Goto, W. Hioe, and M. Hosoya, “Physical limits to quantum flux parametron operation,” *Phys. C*, vol. 185-189, pp. 385-390, Dec. 1991. (Cited on page 14).

[Harada87] Y. Harada, H. Nakane, N. Miyamoto, U. Kawabe, E. Goto, and T. Soma, “Basic operations of the quantum flux parametron,” *IEEE Trans. Magn.*, vol. 23, no. 5, pp. 3801-3807, Sep. 1987. (Cited on pages 14, 61, and 62).

[Harada92] Y. Harada and J. B. Green, “High-speed experiments on a QFP-based comparator for ADCs with 18-GHz sample rate and 5-GHz input frequency,” *IEEE Trans. Appl. Supercond.*, vol. 2, no. 1, pp. 21-25, Mar. 1992. (Cited on page 14).

[Hashimoto03] Y. Hashimoto, S. Yorozu, Y. Kameda, and V. K. Semenov, “A design approach to passive interconnects for single flux quantum logic circuits,” *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 535-538, Jun. 2003. (Cited on page 5).

[Herr10] Q. P. Herr, “A high-efficiency superconductor distributed amplifier,” *Supercond. Sci. Technol.*, vol. 23, no. 2, p. 022004, Feb. 2010. (Cited on page 14).

[Herr11] Q. P. Herr, A. Y. Herr, O. T. Oberg, and A. G. Ioannidis, “Ultra-low-power superconductor logic,” *J. Appl. Phys.*, vol. 109, no. 10, p. 103903, 2011. (Cited on page 13).

[Herr13] A. Y. Herr, Q. P. Herr, O. T. Oberg, O. Naaman, J. X. Przybysz, P. Borodulin, and S. B. Shauck, "An 8-bit carry look-ahead adder with 150 ps latency and sub-microwatt power dissipation at 10 GHz," *J. Appl. Phys.*, vol. 113, no. 3, p. 033911, 2013. (Cited on page 13).

[Hioe91] W. Hioe and E. Goto, "Quantum Flux Parametron: A Single Quantum Flux Superconducting Logic Device (Studies in Josephson Supercomputers)," World Scientific Co. Pre. Ltd., 1991. (Cited on page 7).

[Hioe95] W. Hioe, M. Hosoya, S. Kominami, H. Yamada, R. Mita, and K. Takagi, "Design and operation of a Quantum Flux Parametron bit-slice ALU," *IEEE Trans. Appiled Supercond.*, vol. 5, no. 2, pp. 2992-2995, Jun. 1995. (Cited on page 14).

[Holmes13] D. S. Holmes, "SFQ COMPUTING IN THE USA," *The 26th International Symposium on Superconductivity (ISS2013)*, Tokyo, Japan, 2013. (Cited on page 11).

[Hosoya91] M. Hosoya, W. Hioe, J. Casas, R. Kamikawai, Y. Harada, Y. Wada, H. Nakane, R. Suda, and E. Goto, "Quantum flux parametron: a single quantum flux device for Josephson supercomputer," *IEEE Trans. Appl. Supercond.*, vol. 1, no. 2, pp. 77-89, Jun. 1991. (Cited on page 7).

[Hosoya93] M. Hosoya and W. Hioe, "Margin analysis of quantum flux parametron logic gates," *IEEE Trans. Appl. Supercond.*, vol. 3, no. 2, pp. 3022-3028, Jun. 1993. (Cited on page 14).

[Hosoya95] M. Hosoya, W. Hioe, K. Takagi, and E. Goto, "Operation of a 1-bit quantum flux parametron shift register (latch) by 4-phase 36-GHz clock," *IEEE Trans. Appl. Supercond.*, vol. 5, no. 2, pp. 2831-2834, Jun. 1995. (Cited on page 14).

[Inoue13] K. Inoue, N. Takeuchi, K. Ehara, Y. Yamanashi, and N. Yoshikawa, "Simulation and Experimental Demonstration of Logic Circuits Using an Ultra-Low-Power Adiabatic Quantum-Flux-Parametron," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, p. 1301105, Jun. 2013. (Cited on pages 8 and 61).

[ITRS] International Technology Roadmap for Semiconductors (ITRS): `http://www.itrs.net/home.html` (Cited on page 1).

[Jeffery99] M. Jeffery, P. Y. Xie, S. R. Whiteley, and T. Van Duzer, "Monte Carlo and thermal noise analysis of ultra-high-speed high temperature superconductor digital circuits," *IEEE Trans. Appiled Supercond.*, vol. 9, no. 2, pp. 4095-4098, Jun. 1999. (Cited on page 40).

[Kadin99] A. M. Kadin, "Introduction to Superconducting Circuits," Wiley-Interscience, 1999. (Cited on pages 10 and 92).

[Kadin01] A. M. Kadin, C. A. Mancini, M. J. Feldman, and D. K. Brock, "Can RSFQ logic circuits be scaled to deep submicron junctions?," *IEEE Trans. Appl. Supercond.*, vol. 11, no. 1, pp. 1050-1055, Mar. 2001. (Cited on page 95).

[Keyes70] R. W. Keyes and R. Landauer, "Minimal Energy Dissipation in Logic," *IBM J. Res. Dev.*, vol. 14, no. 2, pp. 152-157, Mar. 1970. (Cited on pages 5 and 15).

[Keyes81] R. W. Keyes, "Fundamental limits in digital information processing," *Proc. IEEE*, vol. 69, no. 2, pp. 267-278, 1981. (Cited on page 3).

[Kirichenko11] D. E. Kirichenko, S. Sarwana, and A. F. Kirichenko, "Zero Static Power Dissipation Biasing of RSFQ Circuits," *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 776-779, Jun. 2011. (Cited on page 12).

[Ko92] H. L. Ko and G. S. Lee, "Noise analysis of the quantum flux parametron," *IEEE Trans. Appiled Supercond.*, vol. 2, no. 3, pp. 156-164, 1992. (Cited on pages 14, 18, and 40).

[Landauer61] R. Landauer, "Irreversibility and Heat Generation in the Computing Process," *IBM J. Res. Dev.*, vol. 5, no. 3, pp. 183-191, Jul. 1961. (Cited on page 2).

[Lee91] G. S. Lee, R. C. Ruby, H. L. Ko, and A. T. Barfknecht, "Superconducting race arbiter with subpicosecond timing discrimination," *Appl. Phys. Lett.*, vol. 59, no. 22, p. 2892, 1991. (Cited on page 14).

[Leff02] H. Leff and A. F. Rex, "Maxwell's Demon 2: Entropy, Classical and Quantum Information, Computing," Taylor & Francis, 2002. (Cited on page 15).

[Likharev77] K. Likharev, "Dynamics of some single flux quantum devices: I. Parametric quantron," *IEEE Trans. Magn.*, vol. 13, no. 1, pp. 242-244, Jan. 1977. (Cited on page 7).

[Likharev82] K. K. Likharev, "Classical and quantum limitations on energy consumption in computation," *Int. J. Theor. Phys.*, vol. 21, no. 3-4, pp. 311-326, Apr. 1982. (Cited on pages 3, 5, 34, 40, 43, 46, and 56).

[Likharev91] K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: a new Josephson-junction technology for sub-terahertz-clock-frequency digital systems," *IEEE Trans. Appl. Supercond.*, vol. 1, no. 1, pp. 3-28, Mar. 1991. (Cited on pages 5 and 10).

[Likharev12] K. K. Likharev, “Superconductor digital electronics,” *Phys. C*, vol. 482, pp. 6-18, Nov. 2012. (Cited on page 10).

[Lloyd00] S. Lloyd, “Ultimate physical limits to computation,” *Nature*, vol. 406, no. 6799, pp. 1047-54, Aug. 2000. (Cited on page 3).

[Lupascu07] A. Lupaşcu, S. Saito, T. Picot, P. C. de Groot, C. J. P. M. Harmans, and J. E. Mooij, “Quantum non-demolition measurement of a superconducting two-level system,” *Nat. Phys.*, vol. 3, no. 2, pp. 119-125, Jan. 2007. (Cited on page 17).

[Makimoto00] M. Makimoto and S. Yamashita, “Microwave Resonators and Filters for Wireless Communication: Theory, Design and Application (Springer Series in Advanced Microelectronics),” Springer, 2000. (Cited on page 30).

[McCumber68] D. E. McCumber, “Effect of ac Impedance on dc Voltage-Current Characteristics of Superconductor Weak-Link Junctions,” *J. Appl. Phys.*, vol. 39, no. 7, p. 3113, 1968. (Cited on pages 19 and 92).

[Meindl00] J. D. Meindl and J. A. Davis, “The fundamental limit on binary switching energy for terascale integration (TSI),” *IEEE J. Solid-St. Circ.*, vol. 35, no. 10, pp. 1515-1516, Oct. 2000. (Cited on page 3).

[Mukaiyama13a] T. Mukaiyama, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, “Design and demonstration of an on-chip AC power source for adiabatic quantum-flux-parametron logic,” *Supercond. Sci. Technol.*, vol. 26, no. 3, p. 035018, Mar. 2013. (Cited on page 82).

[Mukaiyama13b] T. Mukaiyama, N. Takeuchi, K. Ehara, K. Inoue, Y. Yamanashi, and N. Yoshikawa, “Operation of an Adiabatic Quantum-Flux-Parametron Gate Using an On-Chip AC Power Source,” *IEEE Trans. Appl. Supercond.*, vol. 23, no. 4, p. 1301605, Aug. 2013. (Cited on page 82).

[Mukhanov87] O. Mukhanov, V. Semenov, and K. Likharev, “Ultimate performance of the RSFQ logic circuits,” *IEEE Trans. Magn.*, vol. 23, no. 2, pp. 759-762, Mar. 1987. (Cited on page 10).

[Mukhanov04] O. A. Mukhanov, D. Gupta, A. M. Kadin, and V. K. Semenov, “Superconductor analog-to-digital converters,” *Proc. IEEE*, vol. 92, no. 10, pp. 1564-1584, Oct. 2004. (Cited on page 10).

[Mukhanov11] O. A. Mukhanov, “Energy-Efficient Single Flux Quantum Technology,” *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 760-769, Jun. 2011. (Cited on pages 12 and 13).

[Mukhopadhyay06] S. Mukhopadhyay, “Switching energy in CMOS logic: How far are we from physical limit,” 2006 [Online]. Available: `http://nanohub.org/resources/1250` (Cited on page 5).

[Nagasawa95] S. Nagasawa, Y. Hashimoto, H. Numata, and S. Tahara, “A 380 ps, 9.5 mW Josephson 4-Kbit RAM operated at a high bit yield,” *IEEE Trans. Appiled Supercond.*, vol. 5, no. 2, pp. 2447-2452, Jun. 1995. (Cited on pages 19 and 95).

[Nagasawa04] S. Nagasawa, K. Hinode, T. Satoh, H. Akaike, Y. Kitagawa, and M. Hidaka, “Development of advanced Nb process for SFQ circuits,” *Phys. C Supercond.*, vol. 412-414, pp. 1429-1436, Oct. 2004. (Cited on page 95).

[Oates91] D. Oates, A. Anderson, C. Chin, J. Derov, G. Dresselhaus, and M. Dresselhaus, “Surface-impedance measurements of superconducting NbN films,” *Phys. Rev. B*, vol. 43, no. 10, pp. 7655-7663, Apr. 1991. (Cited on pages 17 and 27).

[Oberg11] O. T. Oberg, Q. P. Herr, A. G. Ioannidis, and A. Y. Herr, “Integrated Power Divider for Superconducting Digital Circuits,” *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 571-574, Jun. 2011. (Cited on page 13).

[Orlov12] A. O. Orlov, C. S. Lent, C. C. Thorpe, G. P. Boechler, and G. L. Snider, “Experimental Test of Landauer’s Principle at the Sub-kBT Level,” *Jpn. J. Appl. Phys.*, vol. 51, p. 06FE10, Jun. 2012. (Cited on page 3).

[Ortlepp07] T. Ortlepp, A. O. Mielke, C. J. M. Verwijs, K. F. K. Foo, A. Andreski, H. Rogalla, F. H. Uhlmann, and H. Hilgenkamp, “RSFQ Circuitry Using Intrinsic $\pi-$PhaseShifts,” *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 659-663, Jun. 2007. (Cited on page 85).

[Ortlepp11] T. Ortlepp, O. Wetzstein, S. Engert, J. Kunert, and H. Toepfer, “Reduced Power Consumption in Superconducting Electronics,” *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 770-775, Jun. 2011. (Cited on page 12).

[Ortlepp13] T. Ortlepp, “Lossless ballistic on-chip interconnects for a superconducting processor based on adiabatic quantum flux parametron,” *The 8th FLUXONICS RSFQ Design Workshop*, Ilmenau, Germany, Sept. 2013. (Cited on page 81).

[Polonsky99] S. Polonsky, “Delay insensitive RSFQ circuits with zero static power dissipation,” *IEEE Trans. Appl. Supercond.*, vol. 9, no. 2, pp. 3535-3538, Jun. 1999. (Cited on page 12).

[Radebaugh09] R. Radebaugh, “Cryocoolers: the state of the art and recent developments.,” *J. Phys. Condens. Matter*, vol. 21, no. 16, p. 164219, Apr. 2009. (Cited on page 10).

[Ren11] J. Ren and V. K. Semenov, "Progress With Physically and Logically Reversible Superconducting Digital Circuits," *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 780-786, Jun. 2011. (Cited on page 15).

[Ruby93] R. Ruby, G. Lee, H. Ko, and A. Barfknecht, "Switching probability of QFP comparators as a function of exciter slew-rate," *IEEE Trans. Appiled Supercond.*, vol. 3, no. 1, pp. 2694-2697, Mar. 1993. (Cited on pages 14 and 40).

[Sagawa09] T. Sagawa and M. Ueda, "Minimal Energy Cost for Thermodynamic Information Processing: Measurement and Information Erasure," *Phys. Rev. Lett.*, vol. 102, no. 25, p. 250602, Jun. 2009. (Cited on page 3).

[Semenov03] V. K. Semenov, G. V. Danilov, and D. V. Averin, "Negative-inductance SQUID as the basic element of reversible Josephson-junction circuits," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 938-943, Jun. 2003. (Cited on page 7).

[Semenov13] V. K. Semenov, "Magic Cells and Circuits: New Convergence of Memory and Logic Functions in Superconductor Devices," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, p. 1700908, Jun. 2013. (Cited on page 81).

[Service12] R. F. Service, "Computer science. What it'll take to go exascale.," *Science*, vol. 335, no. 6067, pp. 394-6, Jan. 2012. (Cited on page 1).

[Shimizu89] N. Shimizu, Y. Harada, N. Miyamoto, and E. Goto, "A new A/D converter with quantum flux parametron," *IEEE Trans. Magn.*, vol. 25, no. 2, pp. 865-868, Mar. 1989. (Cited on page 14).

[Shizume95] K. Shizume, "Heat generation required by information erasure," *Phys. Rev. E*, vol. 52, no. 4, pp. 3495-3499, Oct. 1995. (Cited on page 3).

[Sonnet] Sonnet Software Incorporated: `http://www.sonnetsoftware.com/` (Cited on page 30).

[Stewart68] W. C. Stewart, "CURRENT-VOLTAGE CHARACTERISTICS OF JOSEPHSON JUNCTIONS," *Appl. Phys. Lett.*, vol. 12, no. 8, p. 277, 1968. (Cited on pages 19 and 92).

[Takagi08] N. TAKAGI, K. MURAKAMI, A. FUJIMAKI, N. YOSHIKAWA, K. INOUE, and H. HONDA, "Proposal of a Desk-Side Supercomputer with Reconfigurable Data-Paths Using Rapid Single-Flux-Quantum Circuits," *IEICE Trans. Electron.*, vol. E91-C, no. 3, pp. 350-355, Mar. 2008. (Cited on page 81).

[Takeuchi13a] N. Takeuchi, D. Ozawa, Y. Yamanashi, and N. Yoshikawa, "An adiabatic quantum flux parametron as an ultra-low-power logic device," *Supercond. Sci. Technol.*, vol. 26, no. 3, p. 035010, Mar. 2013. (Cited on pages 7 and 30).

[Takeuchi13b] N. Takeuchi, K. Ehara, K. Inoue, Y. Yamanashi, and N. Yoshikawa, "Margin and Energy Dissipation of Adiabatic Quantum-Flux-Parametron Logic at Finite Temperature," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, p. 1700304, Jun. 2013. (Cited on pages 7, 17, and 40).

[Takeuchi13c] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Measurement of 10 zJ energy dissipation of adiabatic quantum-flux-parametron logic using a superconducting resonator," *Appl. Phys. Lett.*, vol. 102, no. 5, p. 052602, 2013. (Cited on page 17).

[Takeuchi13d] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Simulation of sub-k_BT bit-energy operation of adiabatic quantum-flux-parametron logic with low bit-error-rate," *Appl. Phys. Lett.*, vol. 103, no. 6, p. 062602, 2013. (Cited on pages 34 and 65).

[Takeuchi14a] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Reversible logic gates using adiabatic superconducting devices," *submitted to Phys. Rev. Lett*. (Cited on page 46).

[Takeuchi14b] N. Takeuchi, T. Ortlepp, Y. Yamanashi, and N. Yoshikawa, "Novel latch for adiabatic quantum-flux-parametron logic," *J. Appl. Phys.*, in press, 2014. (Cited on page 61).

[Takeuchi14c] N. Takeuchi, T. Ortlepp, Y. Yamanashi, and N. Yoshikawa, "High-Speed Experimental Demonstration of Adiabatic Quantum-Flux-Parametron Gates Using Quantum-Flux-Latches," *IEEE Trans. Appl. Supercond.*, in press, 2014. (Cited on page 61).

[Tanaka04] M. Tanaka, F. Matsuzaki, T. Kondo, N. Nakajima, Y. Yamanashi, A. Fujimaki, H. Hayakawa, N. Yoshikawa, H. Terai, and S. Yorozu, "A single-flux-quantum logic prototype microprocessor," *in the technical digest of the 2004 International Solid-State Circuits Conference (ISSCC2004)*, San Francisco, US, 2004. (Cited on page 10).

[Tanaka12] M. Tanaka, M. Ito, A. Kitayama, T. Kouketsu, and A. Fujimaki, "18-GHz, 4.0-aJ/bit Operation of Ultra-Low-Energy Rapid Single-Flux-Quantum Shift Registers," *Jpn. J. Appl. Phys.*, vol. 51, p. 053102, May 2012. (Cited on pages 11, 14, and 63).

[Tanaka13] M. Tanaka, A. Kitayama, T. Takinami, Y. Komura, and A. Fujimaki, "Bit Error Rate in Low-Voltage RSFQ Circuits with Small Critical Currents/Lowered Bias Voltages", *The 14th International Superconductive Electronics Conference (ISEC 2013)*, Boston, USA, July 2013. (Cited on page 14).

[Teichmann11] P. Teichmann, "Adiabatic Logic: Future Trend and System Level Perspective (Springer Series in Advanced Microelectronics)," Springer, 2011. (Cited on page 7).

[Terai03] H. Terai, Y. Kameda, S. Yorozu, and A. Fujimaki, "The effects of Dc bias current in large-scale SFQ circuits," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 502-506, Jun. 2003. (Cited on page 13).

[Terai04] H. Terai, Z. Wang, Y. Hishimoto, S. Yorozu, A. Fujimaki, and N. Yoshikawa, "Timing jitter measurement of single-flux-quantum pulse in Josephson transmission line," *Appl. Phys. Lett.*, vol. 84, no. 12, p. 2133, 2004. (Cited on page 13).

[TOP500] TOP500 SUPERCOMPUTER SITES: `http://www.top500.org/` (Cited on page 1).

[Toyabe10] S. Toyabe, T. Sagawa, M. Ueda, E. Muneyuki, and M. Sano, "Experimental demonstration of information-to-energy conversion and validation of the generalized Jarzynski equality," *Nat. Phys.*, vol. 6, no. 12, pp. 988-992, Nov. 2010. (Cited on page 3).

[Van Duzer98] T. Van Duzer, "Principles of Superconductive Devices and Circuits,"" Prentice Hall, 2nd Ed., 1998. (Cited on page 10).

[Van Duzer08] T. V. DUZER, "Superconductor Digital Electronics Past, Present, and Future," *IEICE Trans. Electron.*, vol. E91-C, no. 3, pp. 260-271, Mar. 2008. (Cited on page 10).

[Volkmann13a] M. H. Volkmann, A. Sahu, C. J. Fourie, and O. A. Mukhanov, "Implementation of energy efficient single flux quantum digital circuits with sub-aJ/bit operation," *Supercond. Sci. Technol.*, vol. 26, no. 1, p. 015002, Jan. 2013. (Cited on page 12).

[Volkmann13b] M. H. Volkmann, A. Sahu, A. V. Dotsenko, and O. A. Mukhanov, "Operation of Practical eSFQ Circuits", *The 14th International Superconductive Electronics Conference (ISEC 2013)*, Boston, USA, July 2013. (Cited on pages 13 and 63).

[Wallraff04] A. Wallraff, D. I. Schuster, A. Blais, L. Frunzio, R.-S. Huang, J. Majer, S. Kumar, S. M. Girvin, and R. J. Schoelkopf, “Strong coupling of a single photon to a superconducting qubit using circuit quantum electrodynamics.,” *Nature*, vol. 431, no. 7005, pp. 162-7, Sep. 2004. (Cited on page 17).

[Whiteley91] S. R. Whiteley, “Josephson junctions in SPICE3,” *IEEE Trans. Magn.*, vol. 27, no. 2, pp. 2902-2905, Mar. 1991. (Cited on page 25).

[WR] Whitely Research Incorporated: `http://www.wrcad.com/` (Cited on page 25).

[Yamanashi07] Y. Yamanashi, T. Nishigai, and N. Yoshikawa, “Study of LR-Loading Technique for Low-Power Single Flux Quantum Circuits,” *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 150-153, Jun. 2007. (Cited on page 12).

[Yorozu01] S. Yorozu, Y. Kameda, and S. Tahara, “A hybrid switch system architecture for large-scale digital communication network using SFQ technology,” *IEICE Trans. Electron.*, vol. E84-C, no. 1, pp. 15-19, Jan. 2001. (Cited on page 10).

[Yoshikawa99] N. Yoshikawa and Y. Kato, “Reduction of power consumption of RSFQ circuits by inductance-load biasing,” *Supercond. Sci. Technol.*, vol. 12, no. 11, pp. 918-920, Nov. 1999. (Cited on page 12).

[Zhirnov03] V. V. Zhirnov, R. K. Cavin, J. A. Hutchby, and G. I. Bourianoff, “Limits to binary logic switch scaling-a gedanken model,” *Proc. IEEE*, vol. 9, no. 11, pp. 1934-1939, Nov. 2003. (Cited on page 3).

[井上 14] 井上健太, “磁気シールド構造を用いた断熱型磁束量子パラメトロン回路セルライブラリの構築と動作実証,” 修士論文, 2014. (Cited on page 8).

[小澤 11] 小澤暖, “超低消費電力断熱モード磁束量子パラメトロン回路の研究,” 修士論文, 横浜国立大学, 2011. (Cited on pages 7 and 30).

[早川 09] 早川尚夫, “超伝導ディジタルエレクトロニクスの歴史的展望,” 電子情報通信学会論文誌, vol. J92-C, no. 8, pp. 428-432, 2009. (Cited on page 10).

[向山 13] 向山隆, “断熱型磁束量子パラメトロン回路の高速駆動に向けたオンチップ交流電源の研究,” 修士論文, 横浜国立大学, 2013. (Cited on page 82).

[村上 13] 村上和彰, 本田宏明, “ポストエクサスケールスーパーコンピュータの実現の観点から見た超伝導デジタル技術への期待,” 電子情報通信学会総合大会, 2013. (Cited on page 1).

[森田 12] 森田憲一, “可逆計算 (ナチュラルコンピューティング・シリーズ),” 近代科学社, 2012. (Cited on page 15).

Accomplishments

Research papers

1. N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Reversible logic gates using adiabatic superconducting devices," *submitted to Phys. Rev. Lett*.

2. N. Takeuchi, T. Ortlepp, Y. Yamanashi, and N. Yoshikawa, "High-Speed Experimental Demonstration of Adiabatic Quantum-Flux-Parametron Gates Using Quantum-Flux-Latches," *IEEE Trans. Appl. Supercond.*, in press, 2014.

3. N. Takeuchi, T. Ortlepp, Y. Yamanashi, and N. Yoshikawa, "Novel latch for adiabatic quantum-flux-parametron logic," *J. Appl. Phys.*, in press, 2014.

4. D. Si, N. Takeuchi, K. Inoue, Y. Yamanashi, and N. Yoshikawa, "Yield Analysis of Large-Scale Adiabatic-Quantum-Flux-Parametron Logic: The Effect of the Distribution of the Critical Current," *submitted to Phys. C*.

5. N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Simulation of sub-k_BT bit-energy operation of adiabatic quantum-flux-parametron logic with low bit-error-rate," *Appl. Phys. Lett.*, vol. 103, no. 6, p. 062602, 2013.

6. N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Measurement of 10 zJ energy dissipation of adiabatic quantum-flux-parametron logic using a superconducting resonator," *Appl. Phys. Lett.*, vol. 102, no. 5, p. 052602, 2013.

7. N. Takeuchi, K. Ehara, K. Inoue, Y. Yamanashi, and N. Yoshikawa, "Margin and Energy Dissipation of Adiabatic Quantum-Flux-Parametron Logic at Finite Temperature," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, p. 1700304, Jun. 2013.

8. N. Takeuchi, D. Ozawa, Y. Yamanashi, and N. Yoshikawa, "An adiabatic quantum flux parametron as an ultra-low-power logic device," *Supercond. Sci. Tech.*, vol. 26, no. 3, p. 035010, Mar. 2013.

9. T. Mukaiyama, N. Takeuchi, K. Ehara, K. Inoue, Y. Yamanashi, and N. Yoshikawa, "Operation of an Adiabatic Quantum-Flux-Parametron Gate Using an On-Chip AC Power Source," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 4, p. 1301605, Aug. 2013.

10. T. Mukaiyama, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Design and demonstration of an on-chip AC power source for adiabatic quantum-flux-parametron logic," *Supercond. Sci. Tech.*, vol. 26, no. 3, p. 035018, Mar. 2013.

11. K. Inoue, N. Takeuchi, K. Ehara, Y. Yamanashi, and N. Yoshikawa, "Simulation and Experimental Demonstration of Logic Circuits Using an Ultra-Low-Power Adiabatic Quantum-Flux-Parametron," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, p. 1301105, Jun. 2013.

12. S. Miura, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Implementation of SFQ Microwave Choppers for Controlling Quantum Bits," *Phys. Proc.*, vol. 36, pp. 250-255, Jan. 2012.

13. N. Takeuchi, D. Ozawa, Y. Yamanashi, and N. Yoshikawa, "On-chip RSFQ microwave pulse generator using a multi-flux-quantum driver for controlling superconducting qubits," *Phys. C*, vol. 470, no. 20, pp. 1550-1554, Nov. 2010.

14. N. TAKEUCHI, Y. YAMANASHI, and N. YOSHIKAWA, "Design and Implementation of RSFQ Microwave Choppers for the Superconducting Quantum-Computing System," *IEICE Trans. Electron.*, vol. E93-C, no. 4, pp. 458-462, 2010.

15. N. Takeuchi, Y. Yamanashi, Y. Saito, and N. Yoshikawa, "3D simulation of superconducting microwave devices with an electromagnetic-field simulator," *Phys. C*, vol. 469, no. 15-20, pp. 1662-1665, Oct. 2009.

International conferences

1. N. Takeuchi, T. Ortlepp, Y. Yamanashi, and N. Yoshikawa, "Several Applications Using Quantum-Flux-Latch," *The 6th Superconducting SFQ VLSI Workshop (SSV 2013)*, Ibaraki, Japan, Nov. 2013 (Oral).

2. K. Inoue, N. Takeuchi, Y. Yamanashi, N. Yoshikawa, "Design and Test of Basic Cells for Adiabatic Quantum-Flux-Parametron Logic With Magnetic-Shielding Structures," *The 6th Superconducting SFQ VLSI Workshop (SSV 2013)*, Ibaraki, Japan, Nov. 2013 (Poster).

3. D. Si, N. Takeuchi, K. Inoue, X. Peng, Y. Yamanashi, and N. Yoshikawa, "Yield analysis of Large-scale Adiabatic Quantum Flux Parametron Logic: the Effect of the Deviation of the Inductance Parameter," *The 6th Superconducting SFQ VLSI Workshop (SSV 2013)*, Ibaraki, Japan, Nov. 2013 (Poster).

4. N. Takeuchi, T. Ortlepp, K. Inoue, Y. Yamanashi, and N. Yoshikawa, "Proposal and Implementation of High-Speed Test Circuits for Adiabatic Quantum-Flux-Parametron Gates," *The 26th International Symposium on Superconductivity (ISS 2013)*, Tokyo, Japan, Nov. 2013 (Poster).

5. D. Si, N. Takeuchi, K. Inoue, Y. Yamanashi, and N. Yoshikawa, "Yield Analysis of Large-Scale Adiabatic-Quantum-Flux-Parametron Logic: The Effect of the Distribution of the Critical Current," *The 26th International Symposium on Superconductivity (ISS 2013)*, Tokyo, Japan, Nov. 2013 (Poster).

6. N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Design and Implementation of a Reversible Quantum-Flux-Parametron Gate," *The 7th East Asia Symposium on Superconductive Electronics (EASSE 2013)*, Taipei, Taiwan, Oct. 2013 (Poster).

7. N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Purely Reversible Quantum-Flux-Parametron Logic," *The 11th European Conference on Applied Superconductivity (EUCAS 2013)*, Genova, Italy, Sept. 2013 (Oral).

8. N. Takeuchi, T. Ortlepp, Y. Yamanashi, and N. Yoshikawa, "Novel Latch for Adiabatic Quantum-Flux-Parametron Logic," *The 14th International Superconductive Electronics Conference (ISEC 2013)*, Boston, USA, July 2013 (Oral).

9. N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Energy Dissipation and Bit-Error-Rate of Adiabatic Quantum-Flux-Parametron Logic with Under-Damped Junctions," *The 14th International Superconductive Electronics Conference (ISEC 2013)*, Boston, USA, July 2013 (Poster).

10. K. Inoue, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Simulation and Implementation of an 8-bit Carry Look-Ahead Adder Using Adiabatic Quantum-Flux-Parametron," *The 14th International Superconductive Electronics Conference (ISEC 2013)*, Boston, USA, July 2013 (Poster).

11. K. Inoue, N. Takeuchi, K. Ehara, Y. Yamanashi, N. Yoshikawa, "Cell-Base Design of a 1-bit Arithmetic Logic Unit Using Ultra-Low-Power Adiabatic Quantum-Flux-Parametron," *The 5th Superconducting SFQ VLSI Workshop (SSV 2012)*, Nagoya, Japan, Dec. 2012 (Poster).

12. N. Takeuchi, K. Ehara, K. Inoue, Y. Yamanashi, and N. Yoshikawa, "Measurement of 40-zJ energy dissipation of adiabatic quantum-flux-parametron logic

using a superconducting resonator," *The Applied Superconductivity Conference 2012 (ASC 2012)*, Portland, USA, Oct. 2012 (Oral).

13. N. Takeuchi, K. Ehara, K. Inoue, Y. Yamanashi, and N. Yoshikawa, "Margins and energy dissipation of adiabatic quantum-flux-parametron logic at finite temperature," *The Applied Superconductivity Conference 2012 (ASC 2012)*, Portland, USA, Oct. 2012 (Poster).

14. K. Inoue, K. Ehara, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Simulation and experimental demonstration of logic circuits using an ultra-low-power adiabatic quantum-flux-parametron," *The Applied Superconductivity Conference 2012 (ASC 2012)*, Portland, USA, Oct. 2012 (Oral).

15. S. Miura, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Implementation of SFQ Microwave Choppers for Controlling Quantum Bits", *The 13th International Superconductive Electronics Conference (ISEC 2011)*, Den Hague, Netherlands, Sept. 2011 (Poster).

16. N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Comparison of 3D-Electromagnetic Simulation Methods for Designing Superconductor Microwave Devices," *The 6th East Asia Symposium on Superconductor Electronics (EASSE 2011)*, Yamagata, Japan, Oct. 2011 (Poster).

17. S. Miura, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Improvement of SFQ Circuit Systems for Measuring Escape Rates of Josephson Junctions," *The 3rd Superconducting SFQ VLSI Workshop (SSV 2010)*, Yokohama, Japan, Jan. 2010 (Poster).

18. N. Takeuchi, D. Ozawa, S. Miura, Y. Yamanashi and N. Yoshikawa, "Design of RSFQ Circuits for Controlling Superconducting Quantum Bits," *The 3rd Superconducting SFQ VLSI Workshop (SSV 2010)*, Yokohama, Japan, Jan. 2010 (Poster).

19. N. Takeuchi, D. Ozawa, Y. Yamanashi, and N. Yoshikawa, "On-chip RSFQ microwave pulse generator for controlling superconducting qubits," *The 22nd International Symposium on Superconductivity (ISS 2009)*, Tsukuba, Japan, Nov. 2009 (Poster).

20. N. Takeuchi, Y. Saito, Y. Yamanashi, and N. Yoshikawa, "Design and implementation of RSFQ microwave choppers for controlling Josephson junction qubits," *The 12th International Superconductive Electronics Conference (ISEC 2009)*, Fukuoka, Japan, June 2009 (Poster).

21. N. Takeuchi, H. Suzuki, Y. Yamanashi, and N. Yoshikawa, “Design of miniaturized superconducting passive delay lines for RSFQ circuits,” *The 2nd Superconductive SFQ VLSI Workshop (SSV 2009)*, Fukuoka, Japan, June 2009 (Poster).

22. N. Takeuchi, Y. Yamanashi, Y. Saito, and N. Yoshikawa, “3D simulation of superconducting microwave devices with an electromagnetic-field simulator,” *The 21st International Symposium on Superconductivity (ISS2008)*, Tsukuba, Japan, Nov. 2008 (Poster).

23. Y. Saitoh, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, “Implementation and low temperature tests of RSFQ microwave choppers for controlling Josephson junction qubits,” *The International Symposium on Physics of Quantum Technology 2008*, Nara, Japan, Nov. 2008 (Poster).

24. N. Takeuchi, Y. Saitoh, Y. Yamanashi, and N. Yoshikawa, “Design of RSFQ microwave choppers for controlling Josephson junction qubits,” *The International Symposium on Physics of Quantum Technology 2008*, Nara, Japan, Nov. 2008 (Poster).

Domestic conferences

1. 井上健太，竹内尚輝，山梨裕希，吉川信行，“磁気シールド構造を持つ論理セルを用いた断熱型磁束量子パラメトロン論理回路の設計と測定，”2014 年電子情報通信学会総合大会，新潟大学，新潟県，2014 年 3 月.

2. 井上健太，竹内尚輝，山梨裕希，吉川信行，“磁気シールド構造を用いた断熱型磁束量子パラメトロンによる 8-bit Carry Look-ahead Adder の設計と測定結果，”2013 年度秋季低温工学・超電導学会，ウィンクあいち，愛知県，2013 年 12 月.

3. 竹内尚輝，井上健太，山梨裕希，吉川信行，“アンダーダンプ接合を用いた断熱型 QFP 回路の有限温度におけるビットエネルギー，”第 74 回応用物理学会秋季学術講演会，同志社大学，京都府，2013 年 9 月（注目講演）.

4. 司徳永，竹内尚輝，井上健太，山梨裕希，吉川信行，“断熱型磁束量子パラメトロンのパラメータばらつき及び配線インダクタンスが回路動作に及ぼす影響の研究，”第 74 回応用物理学会秋季学術講演会，同志社大学，京都府，2013 年 9 月.

5. 井上健太，竹内尚輝，山梨裕希，吉川信行，“断熱型 QFP 回路の安定動作に向けたシールド構造の研究，”2013 年電子情報通信学会ソサイエティ大会，福岡工業大学，福岡県，2013 年 9 月.

6. 竹内尚輝，山梨裕希，吉川信行，“アンダーダンプ接合を用いた断熱型 QFP 回路の消費エネルギーとビットエラーレートの評価，”電子情報通信学会超伝導エレクトロニクス研究会 SCE2013, 機械振興会館，東京都，2013 年 7 月．

7. 竹内尚輝，井上健太，山梨裕希，吉川信行，“ 断熱型 QFP ゲートに基づいたラッチ回路の提案，”2013 年電子情報通信学会総合大会，岐阜大学，岐阜県，2013 年 3 月．

8. 井上健太，竹内尚輝，江原康平，山梨裕希，吉川信行，“ 超低消費電力断熱型磁束量子パラメトロン回路を用いた 8 ビット全加算器の設計，”2013 年電子情報通信学会総合大会，岐阜大学，岐阜県，2013 年 3 月．

9. 向山隆志，竹内尚輝，山梨裕希，吉川信行，“ 断熱型 QFP 回路駆動用オンチップ交流電源の最大発振周波数の改善，”第 60 回応用物理学会春季学術講演会，神奈川工科大学，神奈川県，2013 年 3 月．

10. 司徳永，竹内尚輝，井上健太，山梨裕希，吉川信行，“ 断熱型量子磁束パラメトロンのパラメータばらつきと動作マージンの関係，” 第 60 回応用物理学会春季学術講演会，神奈川工科大学，神奈川県，2013 年 3 月．

11. 井上健太，竹内尚輝，江原康平，山梨裕希，吉川信行，“ 超低消費電力断熱モード磁束量子パラメトロンを用いた論理回路のシミュレーションと動作実証，”電子情報通信学会超伝導エレクトロニクス研究会 SCE2013，岡山大学，岡山県，2013 年 1 月．

12. 竹内尚輝，江原康平，井上健太，吉川信行，“ 断熱型 QFP 回路の最小ビットエネルギーに関する検討，”第 73 回応用物理学会学術講演会，松山大学，愛媛県，2012 年 9 月．

13. 井上健太，竹内尚輝，江原康平，山梨裕希，吉川信行，“ 超低消費電力断熱モード磁束量子パラメトロン回路を用いた全加算器の設計と動作実証，”2012 年電子情報通信学会ソサイエティ大会，富山大学，富山県，2012 年 9 月．

14. 竹内尚輝，山梨裕希，吉川信行，“ 超伝導共振器を用いた微小消費エネルギーの測定方法の提案，”電子情報通信学会超伝導エレクトロニクス研究会 SCE2012, 機械振興会館，東京都，2012 年 4 月．

15. 竹内尚輝，江原康平，井上健太，吉川信行，“ 超伝導共振器を用いた微小消費エネルギーの測定方法の提案，”第 59 回応用物理学関係連合講演会，早稲田大学，東京都，2012 年 3 月．

16. 井上健太，竹内尚輝，江原康平，山梨裕希，吉川信行，“超低消費電力断熱モード QFP を用いた論理回路の設計及び性能評価，”2012 年電子情報通信学会総合大会，岡山大学，2012 年 3 月．

17. 三浦翔吾，竹内尚輝，山梨裕希，吉川信行，“ SFQ Escape Rate 測定回路のインダクタンス構造の検討，”第 57 回応用物理学関係連合講演会，東海大学，神奈川県，2010 年 3 月．

18. 竹内尚輝，小澤暖，山梨裕希，吉川信行，“超伝導量子ビット操作に向けたオンチップ RSFQ マイクロ波パルスジェネレータの提案，”第 70 回応用物理学会学術講演会，富山大学，富山県，2009 年 9 月．

19. 竹内尚輝，山梨裕希，吉川信行，“ RSFQ 回路のタイミング調整に向けた超伝導小型受動遅延素子の提案，” 2009 年電子情報通信学会総合大会，愛媛大学，愛媛県，2009 年 3 月．

20. 竹内尚輝，斉藤裕一郎，山梨裕希，吉川信行，“三次元電磁界シミュレータを用いた超伝導マイクロ波デバイスのシミュレーション方法，”電子情報通信学会超伝導エレクトロニクス研究会 SCE2008, 機械振興会館，東京都，2009 年 1 月．

21. 斉藤裕一郎，竹内尚輝，山梨裕希，吉川信行，“超伝導量子ビット操作に向けた SFQ マイクロ波チョッパの試作と実装，”第 69 回応用物理学会学術講演会，中部大学，愛知県，2008 年 9 月．

22. 竹内尚輝，山梨裕希，吉川信行，“電磁界シミュレータを用いた超伝導伝送路の三次元シミュレーション，”第 55 回応用物理学関係連合講演会，日本大学，千葉県，2008 年 3 月．

Awards

1. 工学府学生表彰，横浜国立大学大学院工学府，2014 年 3 月．

2. エレクトロニクスソサイエティ学生奨励賞，2013 年電子情報通信学会総合大会，2013 年 9 月．

3. 注目講演，第 74 回応用物理学会秋季学術講演会，2013 年 9 月．

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