Implementation and Experimental Evaluation of a Cryocooled System Prototype for High-Throughput SFQ Digital Applications

Yoshihito Hashimoto, Shinichi Yorozu, Toshiyuki Miyazaki, Yoshio Kameda, Hideo Suzuki, and Nobuyuki Yoshikawa

***Abstract*—We report on development of a cryocooled system prototype for high-throughput single flux quantum (SFQ) digital applications. The system was designed to have 32 I/O links with a bandwidth of 10 Gbps/port. An SFQ multi-chip module (MCM), double mu-metal magnetic shields, a 40-K radiation shield, customized GaAs cryogenic amplifiers, a 32-pin wide-bandwidth cryo-probe, and 32 I/O cables were packaged in a vacuum chamber together with a two-stage 4-K 1-W Gifford-McMahon (G-M) cryocooler. S-parameter measurements showed that the analog bandwidth of the I/O link was 23 GHz. We demonstrated high-speed cryocooled operation of a test module, in which a 5 mm $\times$ 5 mm SFQ circuit chip was flip-chip bonded on a 16 mm $\times$ 16 mm MCM carrier with $\phi 30$ μm InSn bump bonds, at bit rates up to 12.5 Gbps. Measured bit error rate (BER) was less than 10^{-12} for a $10^{23} - 1$ pseudorandom bit sequence (PRBS) at 10 Gbps.**

***Index Terms*—Cryocooler, cryopackaging, integrated circuit, multi-chip module, SFQ, superconductor.**

I. Introduction

CRYOPACKAGING is necessary to utilize ultra-high-speed single flux quantum (SFQ) circuits [1] in practical systems. The high-speed operation with extremely low power dissipation of SFQ digital or mixed-signal circuits, such as analog-to-digital converters [2], network switches [3], [4], and microprocessors [5], have been demonstrated at clock frequencies over 10 GHz, and DC measurements of simple flip-flops have demonstrated the potential of SFQ circuits to operate at over 100 GHz [6]. Additionally, recent progress in chip-to-chip SFQ pulse transmission [7]–[9] has raised the possibility of ultra-high-speed multi-chip modules (MCMs) that can operate at the speed of single chips. Most of these high-speed demonstrations, however, were done by using low-speed input/output (I/O) testing method or DC measurements in liquid helium.

For practical use, SFQ circuits need cryocoolers with high-speed I/O links to room temperature (RT) systems [10]–[12]. Cryocooled systems are successfully being developed for small-scale applications such as digital receivers [10], [11], which require relatively narrow digital bandwidth (hundreds Mbps/port to Gbps/port). However, for large-scale, high-throughput applications such as network switches, which require many (100 to 1000) I/O links with wider digital bandwidth (tens Gbps/port), cryocooled systems are much more difficult to develop. In fact, although a 4 $\times$ 4 switch was demonstrated in a closed cycle refrigerator with 24 high-speed electric I/O links and two optical fiber inputs, the operation frequency was limited at 4 Gbps, which was well below its target frequency of 10 Gbps [12]. Operation of SFQ circuits in cryocooled systems with multi I/O links with a bandwidth of the order of 10 Gbps/port has yet to be reported, so further effort is required to develop cryopackaging technology for high-throughput SFQ digital systems.

Two years ago, we began a study on cryopackaging technology. The primary purpose was to develop a cryocooled system prototype to demonstrate our switch circuits [3], [4] at the system level. The prototype was designed to have 32 I/O links between the SFQ MCM and the RT systems with a bandwidth of 10 Gbps/port for our first system demonstration [13]. We developed elemental cryopackaging technologies and components including MCM [8], [9], semiconductor cryogenic amplifier [13], wide-bandwidth multi-pin cryo-probe [13], and superconductor voltage driver. Last year, we developed the cryocooled system prototype by integrating these elemental cryogenic components, I/O cables, magnetic and thermal shields, and a cryocooler. In this paper, we report on the design, implementation, and experimental results of the system.

II. System Integration

A. System Design

Fig. 1 shows the general scheme of our cryocooled system. The cryocooler has two temperature stages, namely, 4 K and 40 K stages. The SFQ MCM is located on the 4 K stage. The MCM consists of SFQ logic circuit chips, voltage driver chips, and an MCM carrier. The chips are flip-chip bonded on the carrier using solder bumps. The MCM allows one to choose a suitable fabrication process for each chip. In our usual case, logic circuit chips are designed with well-established standard library cells [14] so that they are fabricated with NEC's standard Nb process [15] in which the junction critical current density J_C is 2.5 $\mathrm{kA/cm^2}$, while the driver chips are fabricated using a higher-J_C process (typically $J_C = 10\,\mathrm{kA/cm^2}$) to generate enough output voltage for low bit-error-rate (BER) operation at high speed.

Chip-to-chip communications use SFQ pulses. Both the pulse driver and receiver are single-junction circuits [8], [9].

Manuscript received August 24, 2006. This work was supported in part by the New Energy and Industrial Technology Development Organization (NEDO) as Superconductors Network Device Project, and by the Japan Science and Technology Agency (JST) under the CREST Research Grant.

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Digital Object Identifier 10.1109/TASC.2007.898126

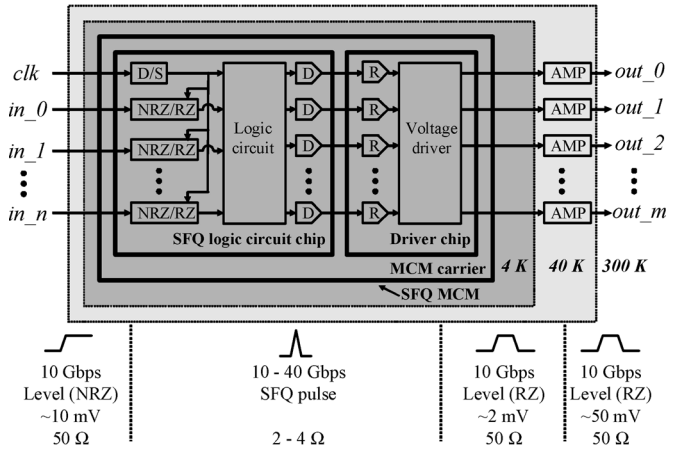

Fig. 1. General scheme of our cryocooled system. D/S, NRZ/RZ, D, and R denote DC to SFQ converter, NRZ to RZ converter, pulse driver, and pulse receiver, respectively. More than one SFQ logic circuit chip and driver chip may be used.

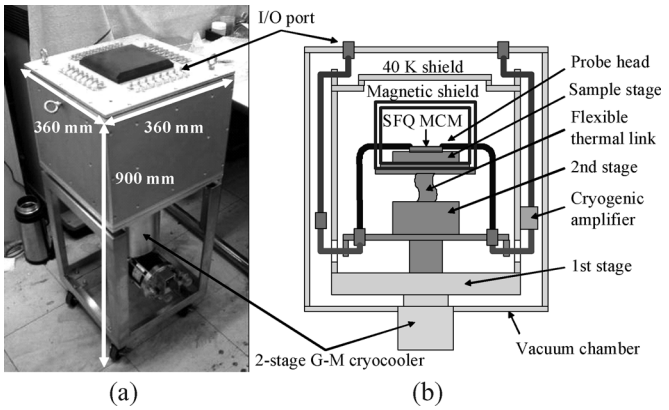

Fig. 2. (a) Photograph and (b) cross-sectional view of system. Compressor is eliminated in photograph.

The transmission line impedance for on-chip and chip-to-chip communication is 2 to 4 Ω for J_C of 2.5 to 10 $\mathrm{kA/cm^2}$. We already demonstrated high-speed chip-to-chip communications up to 60 Gbps with $J_C = 2.5\ \mathrm{kA/cm^2}$ and up to 117 Gbps with $J_C = 10\ \mathrm{kA/cm^2}$ by using ring-shaped circuits [8], [9].

The outputs of the SFQ logic circuit chips are transferred to the voltage driver chips, and are converted into 2-mV level signals on a 50-Ω line. The outputs of the driver chips are amplified to about 50 mV by semiconductor cryogenic amplifiers at 40 K.

The I/O link between the MCM and RT system is electrical, and its data rate was designed to be 10 Gbps/port. For the first demonstration of our switches, number of the I/O link was designed to be 32. Thus the system bandwidth is 320 Gbps.

B. Implementation

Fig. 2 shows a photograph and a cross-sectional view of our system. The system occupies $360\ \mathrm{mm} \times 360\ \mathrm{mm} \times 900\ \mathrm{mm}$ without a compressor. Every component is packaged in a vacuum chamber measuring $360\ \mathrm{mm} \times 360\ \mathrm{mm} \times 304\ \mathrm{mm}$.

The system is cooled by using a two-stage Gifford-McMahon (G-M) cryocooler. Tables I and II show the on-catalog specifications of the cryocooler and compressor. Both of them were manufactured by Sumitomo Heavy Industries Ltd. [16]. The actual temperature and cooling capacity depend on the heat loads

TABLE I
SPECIFICATIONS OF CRYOCOOLER [16]

	Cryocooler RDK-408D
Cooling method	G-M (2-stage)
Cooling capacity	1W at 4.2 K (first stage) 31 W at 40 K (second stage)
Weight [kg]	18
Size [mm]	H 557 × W 180 × L 294
Maintenance [hour]	10,000

TABLE II
SPECIFICATIONS OF COMPRESSOR [16]

	Compressor CSA-71A
Cooling method	air
Power consumption [kW]	6.5
Weight [kg]	140
Size [mm]	H 885 × W 550 × L 550
Maintenance [hour]	20,000

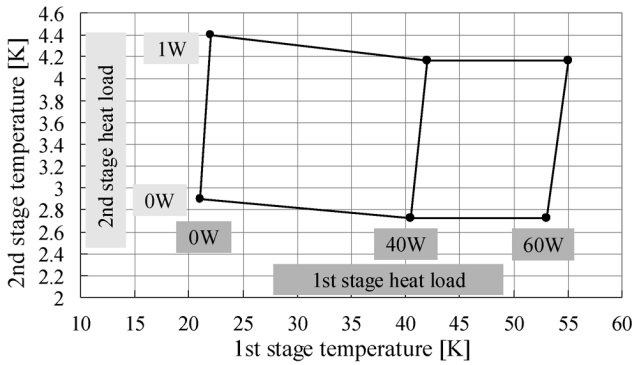

Fig. 3. Measured load map.

on the first and second stages. Hence, we measured the load map of our cryocooler. The measured load map (Fig. 3) shows, for example, if the heat loads are 40 W and 1 W on the first and second stage, respectively, the temperature is 42 K on the first stage while it is 4.2 K on the second stage.

The SFQ MCM is packaged on the 4-K sample stage (Fig. 2b). The MCM and the sample stage are 16 mm × 16 mm and 60 mm × 60 mm, respectively. A flexible thermal link is used to connect the sample stage to the second stage in order to damp mechanical oscillations of the cryocooler. The MCM is surrounded by double mu-metal magnetic shields and a 40 K radiation shield, as shown in Fig. 2b.

On the first stage, GaAs cryogenic amplifiers [13], which were customized for operation in cryogenic environments, are installed to amplify the output of the SFQ MCM. By placing the amplifiers on the first stage, the length, and hence the electrical loss, of the cables between the SFQ MCM and the amplifier can be reduced, resulting in a higher signal to noise ratio and lower BER. The gain of the amplifier is about 30 dB in a frequency range of 60 kHz to 25 GHz at 40 K. Note that the gain is about 9 dB higher than the gain at RT. The amplifier consumes 1 W and measures $35\ \mathrm{mm} \times 58.5\ \mathrm{mm} \times 13.5\ \mathrm{mm}$.

One of the challenges of cryocooled system integration is how to reduce heat load while keeping electric loss as small as possible, because these requirements conflict with each other [10]. Additionally, the system should be easy to handle and robust

TABLE III
I/O CABLE

Part	Cable	Length [mm]
300 K - 1st stage	ϕ2.2 mm Cu, co-ax, flexible	300
1st - 2nd stage	ϕ1.19 mm PB[a], co-ax, semi-rigid	300
2nd stage – MCM	ϕ1.19 mm Cu, co-ax, flexible	100

[a] Phosphor Bronze.

TABLE IV
ESTIMATED HEAT LOAD

Stage	Thermal path or heat source	Heat [W]
1st stage	Radiation	8
	Co-ax cable	43.2
	Other cable	0.1
	Cryogenic amplifier[a]	6
	Support rod	0.1
	1st stage total	*57.4*
2nd stage	Radiation	0.1
	Co-ax cable	0.8
	Other cable	0.1
	2nd stage total	*1.0*
Sample stage	Radiation	-
	SFQ MCM[b]	0.01
	Sample stage total	*0.01*

[a] Six amplifiers are assumed.

[b] MCM with 25,000 junctions is assumed.

against thermal cycles. To solve these problems, we used three different cables for each I/O link (Table III). From RT to the first stage, we used relatively thick (ϕ2.2 mm) Cu co-axial cables to make the electrical loss low. Although such thick Cu cable is also a good thermal conductor, sufficient cooling capacity of the first stage allowed us to use it. These Cu cables were thermally anchored at the first stage. On the other hand, the cooling capacity of the second stage is only 1 W. Hence, we used relatively thin (ϕ1.19 mm) co-axial cables made of Phosphor Bronze (PB), whose thermal conductivity is much less than that of Cu, between the first and second stages to make the heat insertion low. The PB cables were thermally anchored at the second stage. From the second stage to the SFQ MCM, we again used Cu co-axial cable to make the electrical loss low. Although the Cu cables are good thermal conductor, heat insertion through the cable is negligible because the temperature of the sample stage is almost the same as that of the second stage. Here we used thin (ϕ1.19 mm) flexible cable to make it easy to attach/detach the cryo-probe (Fig. 2b) to/from the SFQ MCM. To improve electrical conductance for high-frequency signals, silver plating was made on the surfaces of the inner and outer conductors of all the cable. Additionally, porous poly-tetra-fluoro-ethylene (PTFE), instead of normal PTFE, was used as insulator for all the cable. The reason is that porous PTFE is not as thermally expandable as normal PTFE, so that it makes the I/O cables mechanically robust against thermal cycles. The total length of an I/O link from the RT I/O port to the SFQ MCM is 700 mm. The length from the SFQ MCM to the cryogenic amplifier is 400 mm. Total heat load to the sample stage was estimated to be 1.01 W (Table IV).

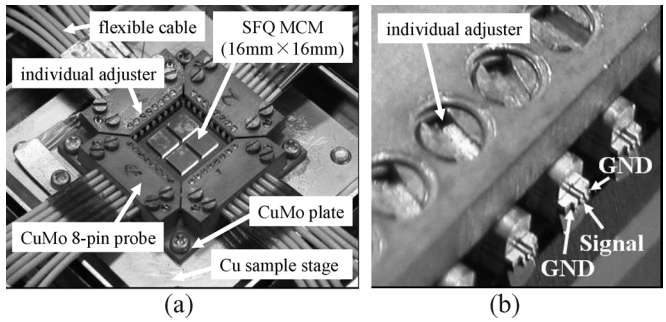

Fig. 4. Photographs of (a) 32-pin cryo-probe and (b) its probe head.

Another challenge was to develop a reliable, wide-bandwidth, multi-pin cryo-probe. The probe had to be detachable in order to be repeatedly used, so we employed mechanical pressure to establish electrical contact. After several improvements, we developed a reliable probe (Fig. 4). The 32-pin probe consists of four 8-pin probes. The body of the 8-pin probe is made of CuMo. Eight probe heads are inserted into the probe body. The probe head is made of BeCu to ensure reliable contact at 4 K, and it has a signal finger and two ground (GND) fingers to form a coplanar waveguide. As shown in Fig. 4a, the SFQ MCM is set on a CuMo plate on the Cu sample stage. Then, four 8-pin probes are aligned and fixed on the CuMo plate with screws. The height of each probe head can be adjusted using individual adjusters, if needed. The reason why we used CuMo for the plate and probe body is that its expansion coefficient $(7.7 \times 10^{-6}/\mathrm{K})$ is closer to that of Si $(4.2 \times 10^{-6}/K)$ in comparison to that of Cu $(17.0 \times 10^{-6}/K)$. Thus, the reliability of the electrical contact at 4 K is higher. Additionally, CuMo is hard material so that the probe body resists abrasion. Note that the probe is scalable: one can easily package larger MCMs that have more than 32 pins by using more 8-pin probes.

After the compressor is turned on, the system reaches 4 K in four to five hours. Achievable minimum sample stage temperature is 3.85 K, which means the actual heat load is less than the estimation (Table IV). The second stage's temperature oscillates with an amplitude of several hundreds mK. It was pointed out that such a temperature oscillation may result in fluctuations of temperature-dependent circuit parameters [10]. In our system, however, the thermal resistance and the thermal capacitance between the second and the sample stages act as a thermal filter so that the oscillation amplitude at the sample stage is significantly damped to mK order.

III. EXPERIMENTAL RESULTS

A. Frequency Characteristics

We designed and fabricated a test chip for S parameter measurements of our system (Fig. 5a). The chip size was 16 mm × 16 mm, and it contained sixteen 50-Ω microstrip lines (MLSs). As shown in Fig. 5b, the probing pad was coplanar in order to match the probe head (Fig. 4b). The probing pad was designed to be 50 Ω. Note that we took into account the dielectric constant ε_r of the Si wafer $(\varepsilon_r \sim 12)$ in designing the probing pad. We cooled the test chip with our cryocooled system and measured the S parameters with a vector network analyser. Fig. 6 plots the measured S21. S21 was measured for an electrical path from one RT I/O port to another RT I/O port through an MSL on the test

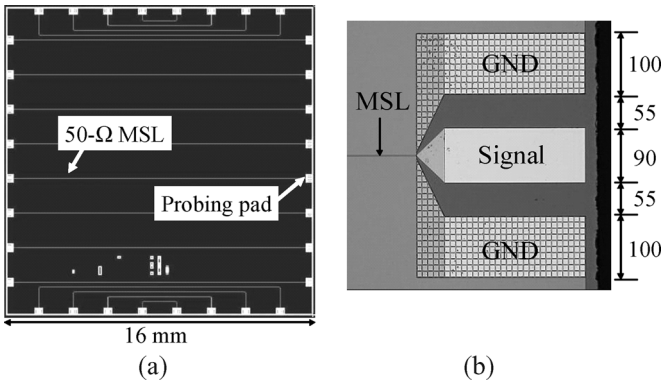

Fig. 5. (a) Layout of 16 mm × 16 mm test chip for S-parameter measurements; (b) photograph of its probing pad. In (b), sizes are in μm.

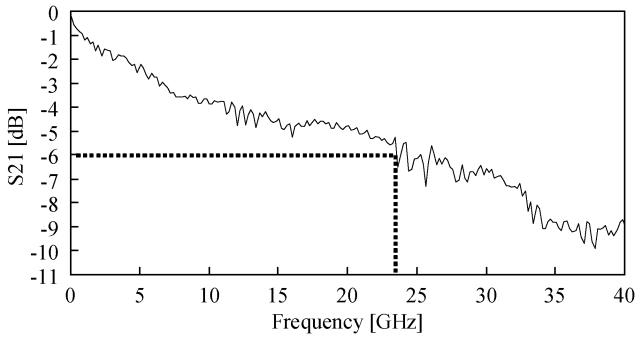

Fig. 6. S21 measured for the test chip shown in Fig. 5. Dashed line indicates analog bandwidth of 23 GHz.

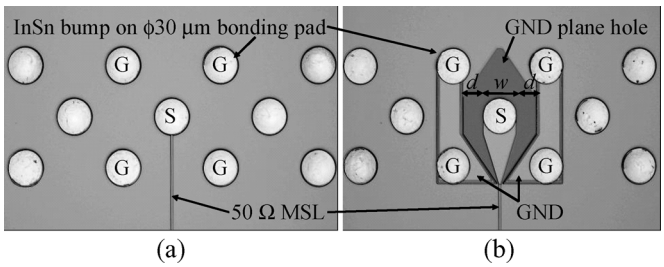

Fig. 7. Microphotographs of (a) ordinary bonding pad and (b) coplanar waveguide (CPW) bonding pad. InSn solder bumps are formed on the $\phi 30$ μm bonding pads. S and G denote signal and GND bumps, respectively. In (b), $w = 30$ μm, $d = 18.3$ μm.

chip that was packaged on the 4-K sample stage so that insertion loss of the system was a half of the S21. Therefore, analog bandwidth (BW), which is defined as a frequency at which the insertion loss is 3 dB, was 23 GHz. The obtained analog BW was much wider than 10 GHz.

In designing MCM, the bonding pad for the I/O signals has to be carefully designed to ensure good impedance matching. Fig. 7a shows an ordinary $\phi 30$ μm bonding pad connected to a 50-Ω MSL, whose width is 1.5 μm. This type of bonding pad has parasitic capacitance between the pad and the ground plane, which causes impedance mismatch. Hence, we also tried a coplanar waveguide (CPW) bonding pad (Fig. 7b). The CPW pad was designed to be 50 Ω by taking into account ε_r of the Si wafer. To compare these two bonding pad types, we fabricated a test module (Fig. 8), in which a 5 mm × 5 mm MSL

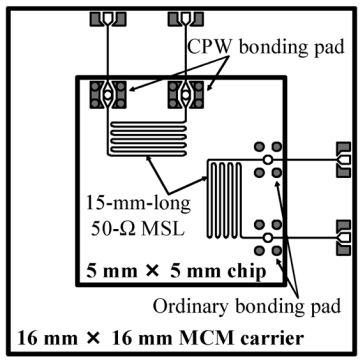

Fig. 8. Schematic of test module to compare two types of bonding pad; one is ordinary type and the other is CPW type.

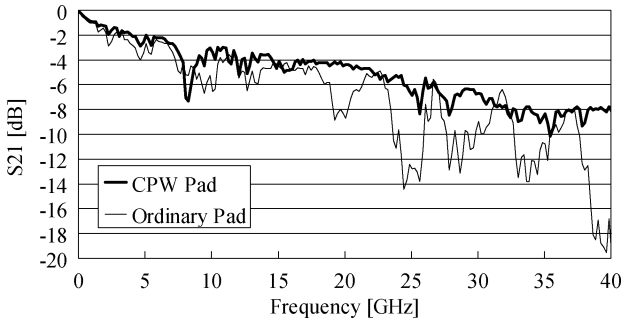

Fig. 9. S21 measured for ordinary bonding pad and CPW bonding pad.

chip was flip-chip bonded on a 16 mm × 16 mm MCM carrier using $\phi 30$ μm InSn solder bumps. The chip contained two 15-mm-long 50-Ω MSLs. One of the MSLs was connected to ordinary bonding pads while the other was connected to CPW bonding pads (Fig. 8). We cooled the test module with our cryocooled system and measured the S parameters. As shown in Fig. 9, the MSL with the ordinary bonding pad exhibited resonance at about 5 GHz and its harmonics. The resonance frequency corresponds to the MSL length, which means the mismatch at the ordinary pad is significant. On the other hand, the MSL with the CPW pad did not exhibit severe resonance. Compared with the S21 for the ordinary pad, the S21 for the CPW pad was 2 to 10 dB higher at the resonance frequencies, which proves that the CPW pad is effective.

B. Cryocooled Operation of SFQ Module

To demonstrate stable cryocooled operation of SFQ circuits at high speed, we designed an SFQ test module that consisted of a 5 mm × 5 mm SFQ chip and a 16 mm × 16 mm MCM carrier (Fig. 10). The chip was flip-chip bonded on the carrier with $\phi 30$ μm InSn solder bumps. The chip contained a test circuit consisting of an NRZ/RZ converter, JTLs, splitters, and a 16-stage SQUID-stack voltage driver (Fig. 11). In the voltage driver, each SQUID was coupled to an RS flip-flop (RSFF), which is the same as the circuit proposed in [12]. The test circuit comprised 591 junctions and its bias current was 90 mA.

The test circuit operates as follows. If the data *dat_in*, which is in non-return-to-zero (NRZ) format, and clock *clk_in* are applied to the circuit, the NRZ/RZ converter converts *dat_in* into an SFQ pulse that is in return-to-zero (RZ) format. Then, the pulse is divided into two: one is used as a *set* pulse while the other is used as a *reset* pulse for the RSFF. A delay of 50 ps is

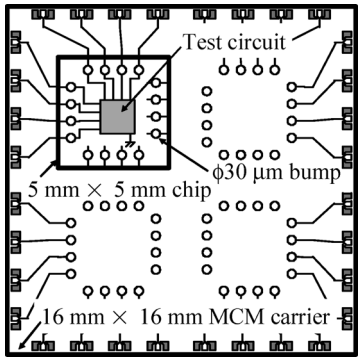

Fig. 10. Schematic of SFQ test module for BER measurement.

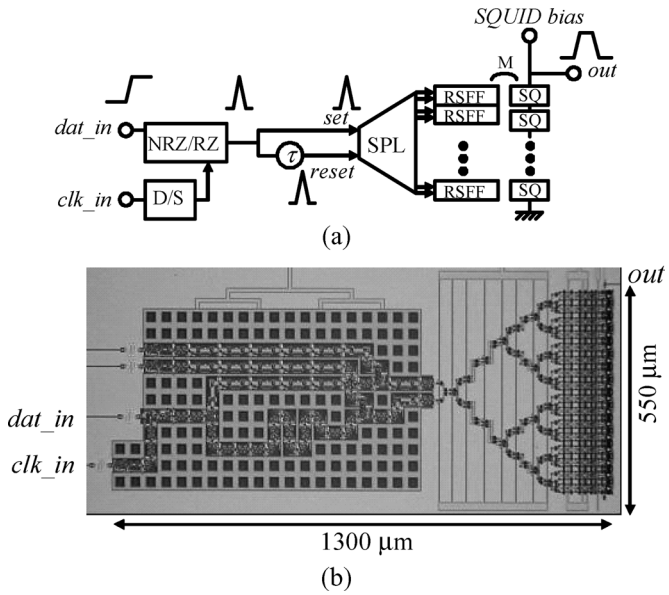

Fig. 11. (a) Circuit diagram and (b) microphotograph of test circuit. D/S, NRZ/RZ, SPL, RSFF, and SQ denote DC to SFQ converter, NRZ to RZ converter, splitter, RS flip-flop, and SQUID, respectively.

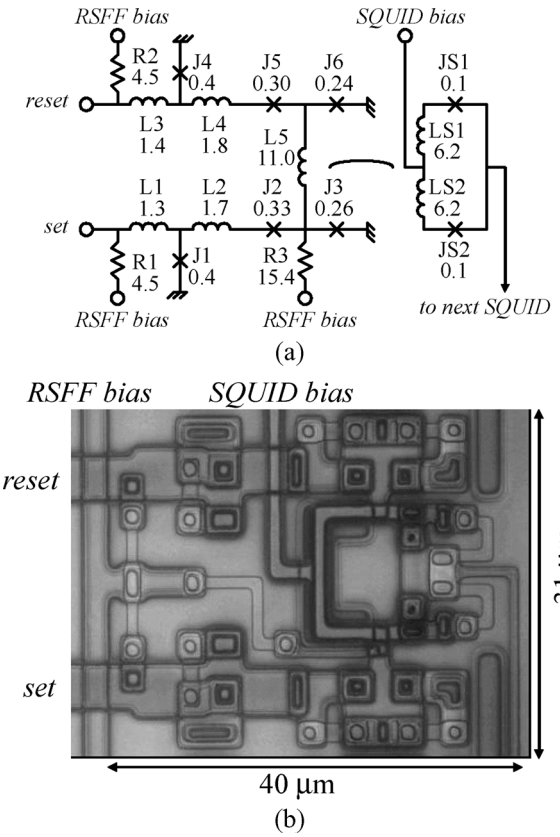

Fig. 12. (a) Optimized equivalent circuit and (b) microphotograph of single stage of voltage driver. Currents, inductances, and resistances are in mA, pH, and Ω, respectively. Bias voltage for RSFF is 2.5 mV.

added to the *reset* pulse. The *set* pulse is split into 16 pulses and each pulse is applied to each RSFF. The *reset* pulse is also split into 16 pulses and applied to each RSFF. Thus, when data "1" comes to the circuit, the RSFFs store the data for 50 ps. While the RSFFs store the data, the 16 SQUIDs generate voltage.

The voltage driver is a key circuit for high-speed, low-BER cryocooled operation of SFQ circuits. In principle, to make the driver operate with a wide bias margin and high output voltage, the critical current I_C of the SQUID should be increased, because by doing so, one can reduce the impact of the bias-current reduction that occurs because part of the SQUID bias current flows to the 50-Ω load while the SQUIDs are generating voltage. Nevertheless, we used the smallest available junction whose size was $1\ \mu\mathrm{m} \times 1\ \mu\mathrm{m}$ ($I_C = 0.1$ mA) to minimize the circuit size and power, and optimized the driver (Fig. 12). Additionally, an aggressive design rule, in which the minimum line width, minimum space, and alignment margin were $1\ \mu\mathrm{m}$, $1\ \mu\mathrm{m}$, and $0.3\ \mu\mathrm{m}$, respectively, was used in the layout of the driver to minimize the circuit size. The test chip was fabricated using the same process as NEC's standard Nb process [15] except that J_C was increased to $10\ \mathrm{kA/cm^2}$ to generate enough voltage (∼2 mV for our cryogenic amplifier [13]) for low BER operation at 10 Gbps. The shunt resistance R was designed to be $I_C R = 0.88$ mV. GND plane holes were made below the coupling inductances $L5$, $LS1$, and $LS2$ (Fig. 12) to increase the coupling constant. The coupling constant was measured to be 0.46. The output voltage of the driver was 2 to 2.5 mV during low-speed measurement.

The MCM carrier was fabricated using the same process as that for chips except that it did not contain any junction. The carrier had an Nb GND plane and two Nb wiring layers. InSn solder bumps were formed with a simple emersion process [17] on Au/Pd/Ti/Nb bonding pads of the chip and carrier. The thicknesses were 50 nm, 100 nm, and 200 nm for Ti, Pd, and Au, respectively. The CPW bonding pads (Fig. 7b) were used for I/O signals, while ordinary bonding pads (Fig. 7a) were used for biases.

We packaged and cooled the test module in our cryocooled system. First, we performed high-speed function tests. We applied a test pattern and a clock from a pulse pattern generator (PPG) at RT to the test module and observed the output of the module on a digital sampling oscilloscope. We confirmed correct operation: the test pattern *dat_in* (in NRZ format) was converted into RZ format by the on-chip NRZ/RZ converter, and the output of the module was amplified by the GaAs cryogenic amplifier at 40 K (Fig. 13). A maximum output voltage of about 50 mV was obtained at the optimum driver bias at 10 Gbps. We confirmed correct operation up to 12.5 Gbps. The maximum throughput was limited by the PPG.

We also measured BER by applying a 10-Gbps $10^{23}-1$ pseudorandom bit sequence (PRBS) and a clock from the PPG to the test module. Errors were counted with an error detector at

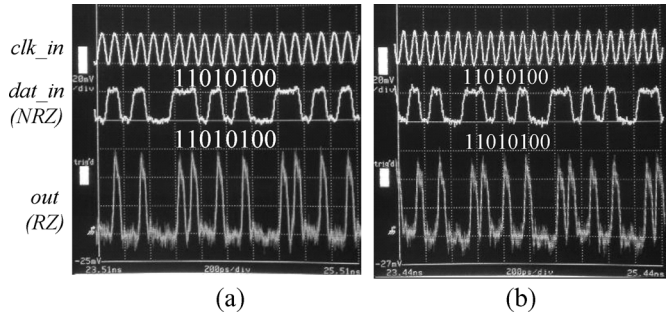

Fig. 13. High-speed cryocooled operation of SFQ test module at (a) 10 Gbps and (b) 12.5 Gbps. Horizontal axis is 200 ps/div and vertical axis is 20 mV/div.

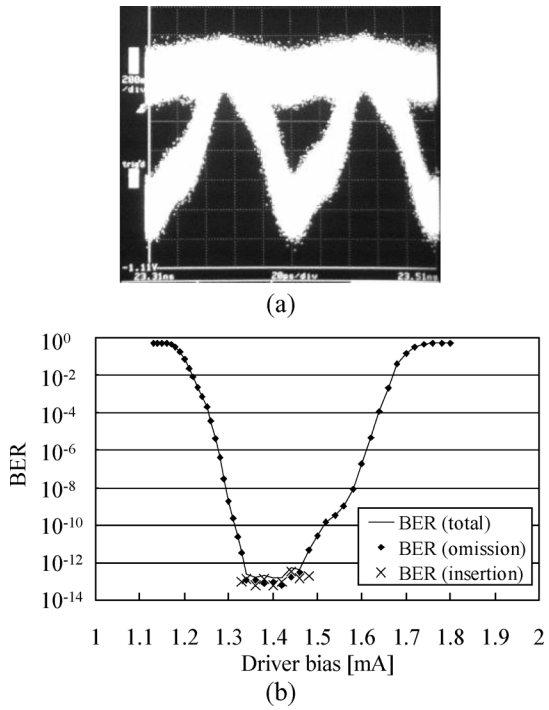

Fig. 14. (a) Eye diagram and (b) BER measured at 10 Gbps for $10^{23}-1$ PRBS pattern. In (a), horizontal axis is 20 ps/div and vertical axis is 200 mV/div.

RT. The output of the system was amplified again to about 1 V by using a semiconductor amplifier at RT to make the output voltage higher than the threshold of the error detector. Fig. 14 shows the measured eye diagram and BER curve. The BER was less than 10^{-12} in a driver bias margin of 1.4 mA $\pm$ 4.3%.

IV. Conclusion

We have developed a cryocooled system prototype. The system has 32 high-speed I/O links between an SFQ MCM and RT systems. S-parameter measurements showed that the analog BW of the I/O link was 23 GHz. The cryocooled system including 32 I/O cables, a 32-pin cryo-probe, an SFQ MCM with a superconductor voltage driver, and a customized GaAs cryogenic amplifier stably operated at bit rates up to 12.5 Gbps. The BER for a $2^{23}-1$ PRBS was less than 10^{-12} at 10 Gbps, which showed that the prototype has enough performance for high-speed system demonstrations of not only our switches but also other SFQ digital circuits. Our cryopackaging technology and cryogenic components such as MCM, cryo-probe, cryogenic amplifier, and voltage driver can be generally used to integrate high-throughput cryocooled SFQ digital systems.

Acknowledgment

The authorswould like to thank S. Akasaka, T. Kagawa, and M. Machida of Kawashima Manufacturing Co., Ltd. and K. Fujioka of Cryoware Inc. and S. Sasai of TOTOKU Electric Co., Ltd. for their significant contributions to development of the system. They would also like to thank the members of SRL-ISTEC for their discussion and assistance.

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