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Direct measurements of propagation delay of single-flux-quantum circuits by time-to-digital converters

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Abstract: Direct measurements of propagation delay of single-flux-quantum (SFQ) circuits were performed using SFQ double-oscillator time-to-digital converters. The propagation delay of several SFQ logic gates in our cell library named CONNECT were measured in picosecond resolution. Small discrepancy in the propagation delay of picosecond level was observed between measurement and circuit simulation results. The discrepancy is well explained assuming the parasitic inductance around shunt resistors of Josephson junctions.

Keywords: SFQ circuits, superconducting devices, TDC, Josephson junctions, superconducting integrated circuits, propagation delay
Classification: Superconductivity

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1 Introduction

Single-flux-quantum (SFQ) circuits have a potentiality to become a basic technology for next-generation high-end computing systems because of their extremely low-power and high-speed operation [1]. Recently high-speed operations of microprocessors [2] and network switches [3] beyond 20-GHz clock frequency were successfully demonstrated. One of important issues in fabricating SFQ circuits is the requirement of precise timing design in picosecond resolution. Because SFQ logic gates are basically a clocked gate, they need globally synchronous high-speed clocks in a gate level. Current design of SFQ circuits is carried out based on timing parameters extracted by using circuit simulators [4]. It is strongly demanded to verify the timing parameters of each logic gate in picosecond resolution experimentally to ensure the timing design and to increase the maximum clock frequency. It was reported recently that the measured propagation delay of the Josephson transmission line (JTL) is about 20% faster than circuit simulation results [5]. The discrepancy was attributed to the parasitic inductance at shunt resistors of Josephson junctions.

We have been developing SFQ time-to-digital converters (TDC), which directly convert a small time difference between two signals into a binary code. Our SFQ TDC is a double-oscillator type and has time resolution of about 2.5 ps [6, 7]. In this study, we investigated the propagation delay of SFQ logic gates using the SFQ TDC. The propagation delay of several logic gates in our cell library named CONNECT [8] was measured in picosecond resolution.

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2 Experiment

We measured the propagation delay of a two-junction JTL, a confluence buffer (CB) and several clocked SFQ logic gates, such as a delay flip-flop (DFF), a flip-flop with non-destructive readout (NDRO), a NDRO with complementary outputs (NDROC), a delay flip-flop with complementary clock inputs and data outputs (D2FF) and a resettable toggle flip-flop (RTFF) in the CONNECT cell library. In experiments the propagation delay of clocked gates is defined as a time interval between clock input and data output. In order to improve the time resolution in the delay measurement, the propagation delay of several stages of gates, which are connected in series, was measured by SFQ TDC. The SFQ logic gates and the SFQ TDC was fabricated on the same chip by using the CONNECT cell library and the SRL 2.5 kA/cm^{2}Nb process [9]. In the delay measurement, the frequencies of the ring-oscillators of the TDC were evaluated by monitoring their average voltage. We repeated delay measurements 1000 times to obtain one data point, though the acquired data were very stable and their distribution is within the time resolution of the TDC, *i.e.* 2.5 ps.

3 Results and Discussions

Measured bias-current dependence of the propagation delay of a two-junction JTL is plotted by closed circles in Fig. 1 (a). Circuit simulation results based on a circuit diagram shown in Fig. 2 (a) are also plotted by a solid curve in the figure. One can see that the discrepancy of about two ps is seen between measurement and simulation results. Similar discrepancy in the propagation delay of the JTL was reported in the experiment using ring oscillators made up with JTLs, where the discrepancy was attributed to the parasitic inductance around shunt resistors of Josephson junctions [5]. In order to examine the effect of the parasitic inductance, we performed the circuit simulation taking into account the parasitic inductance around the shunt resistor. Fig. 2 (b) shows an equivalent circuit diagram of the Josephson junction in the JTL with parasitic inductances L_p around the shunt resistor, where the value was extracted from the structure of the layout. The simulation results taking into account the parasitic inductance is shown in Fig. 1 (a) by a dashed curve. Fairly good agreement between measurement and simulation results can be seen in the figure.

Measured bias-current dependences of the propagation delay of the NDROC and the NDRO for several samples are plotted in Fig. 1 (b) and (c) by dots, where the delay from "clk" to "dout1" for the NDROC and the delay from "clk" to "dout" for the NDRO are measured. Circuit simulation results with and without the parasitic inductance around the shunt resistor are also shown by dashed and solid curves in the figure, respectively, where the parasitic inductances in the Josephson junction similar to Fig. 2 (b) was assumed in each gate. One can see that the simulation results taking into account the parasitic inductance agree quite well with the experimental results, except that some discrepancy appears at low bias-current condition in the NDRO. Sim-

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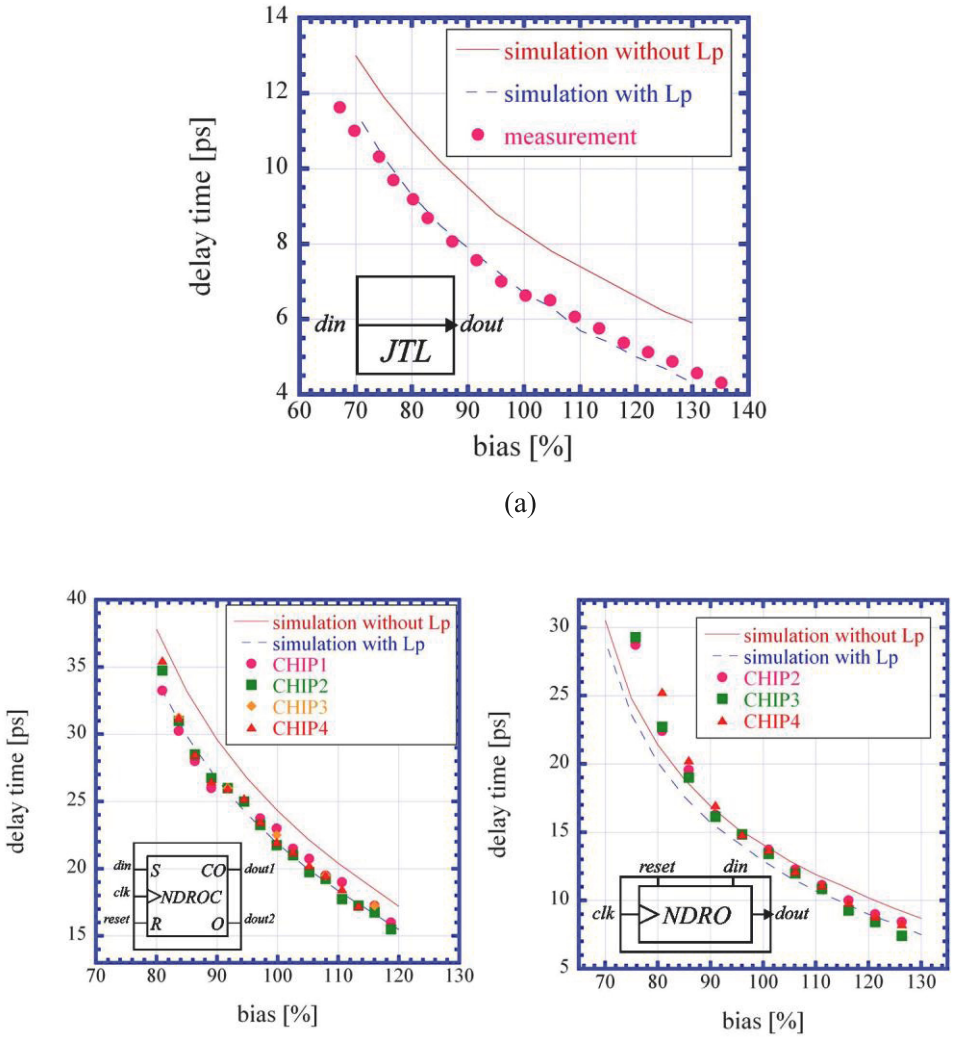

Fig. 1. Propagation delay of SFQ logic gates as a function of their bias current. (a) JTL (from din to dout), (b) NDROC (from clk to dout1), (c) NDRO (from clk to dout). Dots indicate the measured results. Dashed and solid curves show simulation results with and without the parasitic inductance L_p around shunt resistors of Josephson junctions. Inserts in the figures represent symbols of each logic gate.

ilar agreements between the experimental results and the simulation results with parasitic inductance at high bias condition and some discrepancy at low bias condition were also observed in the CB and the RTFF. The discrepancy at low bias current is thought to arise from the fact that the propagation delay of SFQ circuits depends sensitively on circuit parameters at lower bias condition.

Measured bias-current dependences of the propagation delay of D2FFs and DFFs are also plotted in Fig. 3 (a) and (b) by dots with circuit simulation results with and without the parasitic inductance around the shunt resistor.

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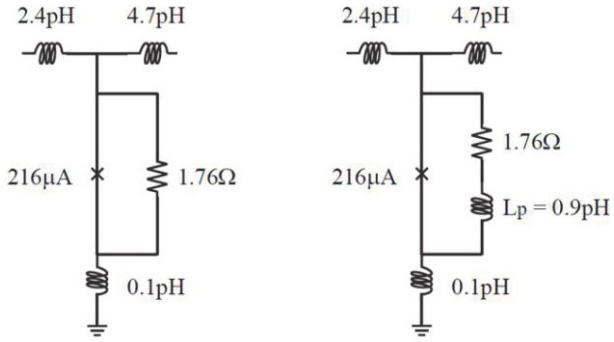
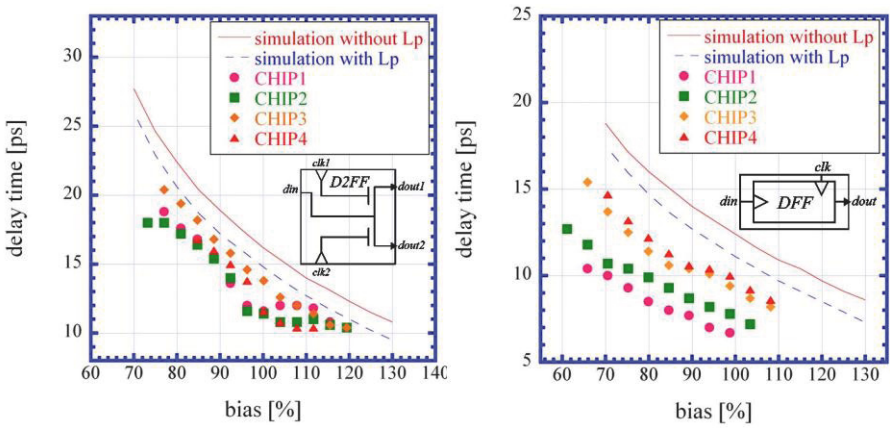


(a) (b)

Fig. 2. Equivalent circuit diagrams of the Josephson junction in the JTL (a) without and (b) with parasitic inductances L_p around the shunt resistor.



(a) (b)

Fig. 3. Propagation delay of SFQ logic gates as a function of their bias current. (a) D2FF (from clk1 to dout1), (b) DFF (from clk to dout). Dots indicate measured results. Dashed and solid curves show simulation results with and without the parasitic inductance L_p around shunt resistors of Josephson junctions. Inserts in the figures represent symbols of each logic gate.

In contrast to the previous results, the measured results are much smaller than the simulation results in all bias-current conditions. In addition, the measured data vary widely depending on the samples. Though we don't figure out the reasonable reason for the disagreement yet, the extraction of the circuit parameters from the physical circuit structure has to be reconsidered carefully in these logic gates.

4 Conclusion

We directly measured the propagation delay of SFQ logic gates using double-oscillator SFQ TDCs. The propagation delay of several basic SFQ logic

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gates in the CONNECT cell library were measured in picosecond resolution. It was shown that the measured propagation delay of almost SFQ logic gates coincided well with the simulation results taking into account the parasitic inductance at shunt resistors in Josephson junctions. However the measured propagation delay was much smaller and varied depending on the samples in some logic gates, such as the D2FF and the DFF.

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