

Design and Investigation of Gate-to-Gate Passive Interconnections for SFQ Logic Circuits

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Abstract—We have developed a method of designing single-flux-quantum (SFQ) logic circuits with passive gate-to-gate interconnections. Based on our method, we designed a 2×2 switch in which all the interconnections are implemented with passive transmission lines (PTLs) while short Josephson transmission line (JTL) segments are used only to adjust the signal timings. Compared with an identical switch using JTL interconnections, the switch using PTL interconnections has 45% fewer wiring junctions and requires 48% less wiring power current. The switch operated at 40 GHz with a bias margin of $\pm 9.5\%$.

Index Terms—Integrated circuit, interconnection, passive transmission line, single-flux-quantum (SFQ), superconductor.

I. INTRODUCTION

SINGLE-FLUX-QUANTUM (SFQ) logic circuits [1] can use two kinds of devices for interconnection: Josephson transmission lines (JTLs) and passive transmission lines (PTLs) such as microstrip lines. JTLs are generally used because they easily propagate SFQ pulses without reflections and they facilitate signal timing adjustment. However, since JTLs use Josephson junctions (JJs), they have a large propagation delay, and the powering current increases with the length. Moreover, the probability of timing errors due to process variations and thermal noise increases with the length. It is thus problematic to develop larger scale and/or higher speed SFQ circuits using only JTLs for interconnection.

These problems can be reduced by replacing JTLs with PTLs because PTLs do not use JJs except for the drivers and receivers [2]–[12]. PTLs support signal transmission at the speed of light, which is an order of magnitude faster than that of typical JTLs. Moreover, the powering current is independent of the length and is much lower than that of JTLs. The timing error probability is also expected to be much smaller than in JTLs. Thus, PTLs will be a key component in high-performance SFQ circuits.

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Since the advantages of PTLs over JTLs become more visible with longer interconnections, one promising PTL application is the interconnection between SFQ circuit blocks separated by a long distance relative to the single-stage-JTL length. Considering this, we used PTLs in a 4×4 switch to connect greatly separated 2×2 switch blocks [11], [12]. However, the PTLs' contribution is generally very limited in such applications. In fact, we used only six PTLs; we still used JTLs within each 2×2 switch block.

To better utilize their advantages, we need to use PTLs more extensively. To do so, we developed a method of designing SFQ logic circuits using gate-to-gate passive interconnections. We also investigated basic properties of our driver and receiver when they were connected with very short PTLs. Using our method, we designed and demonstrated a 2×2 switch. We also compared the PTL-version 2×2 switch with a JTL version to examine the effectiveness of PTL interconnection. Circuits were fabricated using NEC's standard Nb process [13]. The critical current density of the junction was 2.5 kA/cm^2 .

II. DESIGN METHOD

A. PTL-Connectable Logic Cell and Circuit Design Method

To enable us to use PTLs for gate-to-gate interconnections, we developed PTL-connectable logic cells that enable PTLs to be directly connected to the I/O ports. The main feature of our cell is that it has not only an input port but also an output port for the clock signal [Fig. 1(a)]. This feature is suitable for SFQ logic circuits in which clock-splitting is frequently used. An implementation of the PTL-connectable logic cell is shown in Fig. 1(b). The cell consists of a logic cell, PTL receivers, PTL drivers [9], and a splitter. The logic cell and splitter are elements of our standard cell library "CONNECT" [14]. We designed five PTL-connectable logic cells: D-flip-flop (DFF), AND, NOT, NDRO, and confluence buffer (CB). The CB is used as an asynchronous OR gate. Fig. 2 shows the PTL-connectable DFF as an example. We extracted the timing parameters of the designed cells by simulations (Table I). The cells were tested at low speed. The worst performing cell was the AND cell, which had a bias margin of $\pm 21.6\%$. The best performing cell was the DFF cell, which had a bias margin of $\pm 29.6\%$. The bias margin for correct operation for all cells was $\pm 17.0\%$. Although further optimization may increase the bias margin, this level is acceptable as the first versions.

In actual circuit design, signal timing adjustments are needed. In our design method, the signal timings are adjusted by inserting JTL segments immediately after the receivers (Fig. 3). The receiver consists of a receiver stage followed by a buffer

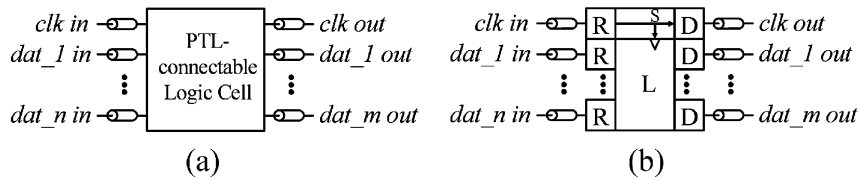


Fig. 1. (a) General scheme of PTL-connectable logic cell and (b) its implementation. L, S, R, and D are logic cell, splitter, receiver, and driver, respectively.

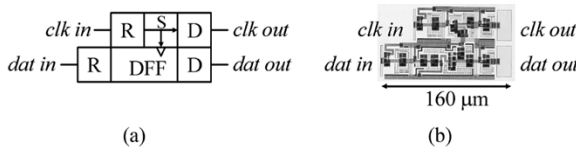


Fig. 2. (a) Configuration and (b) layout of PTL-connectable DFF.

TABLE I
TIMING PARAMETERS OF PTL-CONNECTABLE LOGIC CELLS

PTL-connectable Logic Cell	$clk\ in-clk\ out$ [ps]	delay ^a [ps]	Setup [ps]	Hold [ps]
DFF	20.2	31.7	-8.1	8.1
AND (ain)	20.5	39.2	-16.1	16.8
(bin)	-	-	-15.0	15.5
NOT	20.5	36.0	6.2	10.9
NDRO (set)	20.3	33.5	-11.4	11.6
(reset)	-	-	0.4	-0.3
CB	N/A	29.4	N/A	N/A

^aDuration between $clk\ in$ and $dat\ out$, for clocked cells. For CB, delay is the duration between $dat\ in$ and $dat\ out$.

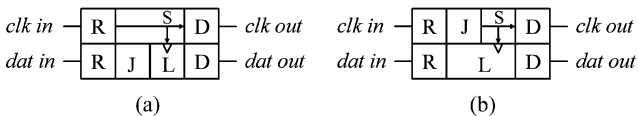


Fig. 3. Signal timing adjustment: (a) add delay to data and (b) add delay to clock. J denotes JTL segment.

stage [9]. Since the timing adjustment procedure is simply extending the receiver's buffer stage, it does not disturb the PTL-connectable logic cell's operation.

We also developed multiple-fanout PTL-connectable cells that have multiple data output ports or/and multiple clock output ports. These cells are implemented by inserting splitters in the PTL-connectable cells (Fig. 4).

Our method uses splitters within the PTL-connectable logic cells (Figs. 1 and 4) in contrast to the design methods reported in [5] and [6]. By doing so, we avoid using explicit PTL-connectable splitters which would add three more JJs (corresponding to a driver-receiver pair) for each signal splitting. Therefore, we can significantly reduce the number of JJs in SFQ logic circuits.

B. PTL

Our standard fabrication process [13] has three Nb layers. The lowest Nb layer is used as the ground plane and the other two Nb layers are used for wiring. The PTL is formed with the lower wiring layer (Fig. 5). The PTL impedance is $2\ \Omega$ and the width is

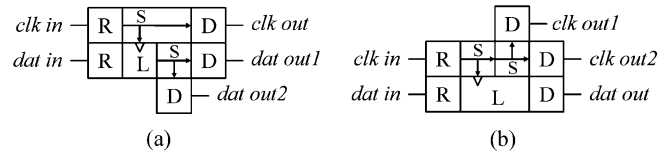


Fig. 4. Multiple-fanout cells. Cell having (a) two data output ports and (b) two clock output ports.

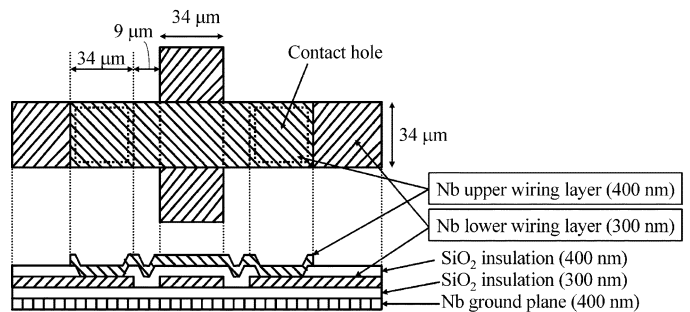


Fig. 5. Cross-section of PTL crossing. Numbers in parentheses denote thicknesses.

$34\ \mu\text{m}$. At the PTL crossing, one of the PTLs is formed with the upper wiring layer (Fig. 5). The parasitic capacitance between crossing PTLs was estimated to be about $0.1\ \text{pF}$. Crosstalk between the crossing PTLs reduces the receiver's bias margin [10]. However, our recent measurements showed no serious degradation of the driver and receiver bias margins for up to four PTL crossings.

III. INVESTIGATION OF DRIVER AND RECEIVER CONNECTED WITH SHORT PTLs

To investigate our drivers and receivers connected with short PTLs, we designed six PTL ring oscillators with 4-mm-, 2-mm-, 1-mm-, 400- μm -, 200- μm -, and 20- μm -long PTLs. The circuit diagram and measurement procedure are described in [9]. We measured the bias margins of the driver-receiver pairs over a frequency range of 10–40 GHz. Fig. 6 shows the test results. The resonance frequency reasonably increased as the PTL length was decreased, and no degradation due to resonance was observed for PTLs shorter than 1 mm. These results demonstrated that our driver and receiver worked well even with very short “PTLs” that can be considered lumped elements.

We also numerically investigated dependence of propagation delay t_W on PTL length. The propagation delay t_W was defined as duration between driver's switching and receiver's switching (Fig. 7). Fig. 8 is the simulation result. For relatively short PTL lengths, t_W nonlinearly depended on the PTL length. This is because the reflection at the receiver went back to the driver before the driver finished switching. The nonlinearity is clearer

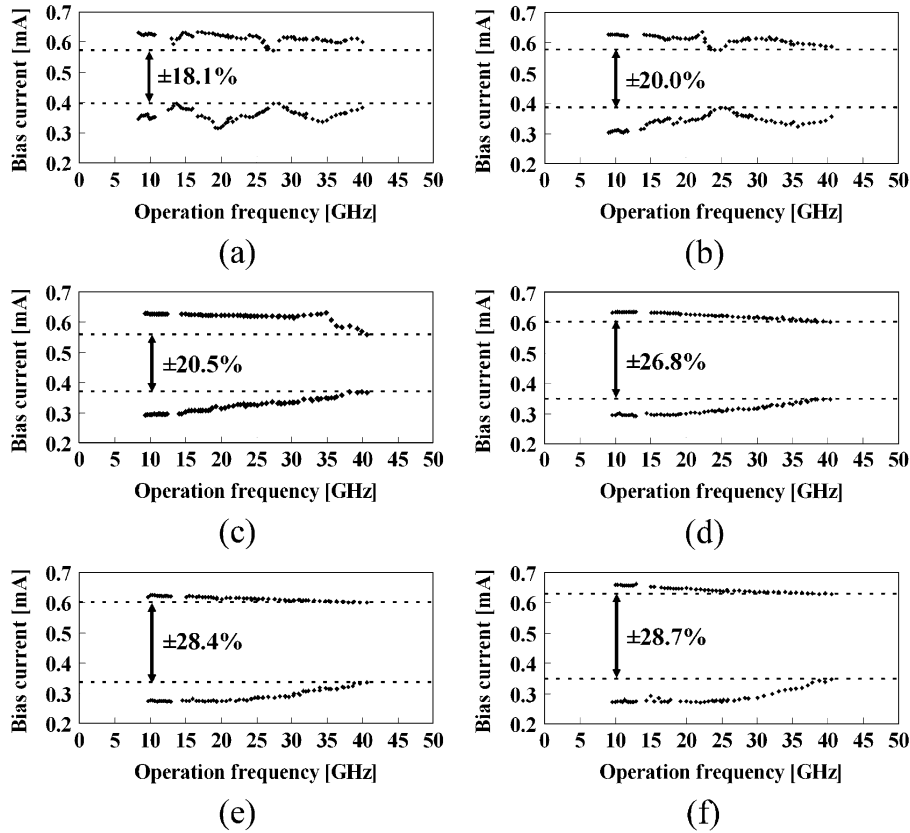


Fig. 6. Measured bias margins for driver-receiver pairs. PTL lengths were (a) 4 mm, (b) 2 mm, (c) 1 mm, (d) 400 μm , (e) 200 μm , and (f) 20 μm . Narrowest bias margin from 10 to 40 GHz is shown in each plot.

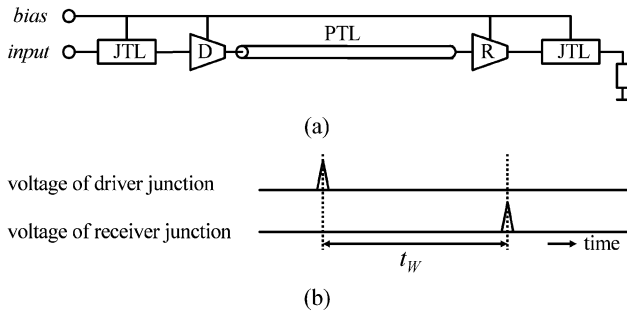


Fig. 7. Circuit simulated: (a) circuit diagram and (b) definition of propagation delay t_W . D and R are driver and receiver, respectively.

for lower bias currents, because the driver's switching delay increases as the bias current decreases. However, for bias currents equal to or larger than -20% of the designed value, the linear fitting of t_W approximates the simulation results with better than 0.42-ps accuracy over the PTL length range of 0 to 3 mm. This means that for these bias values, we can use the following convenient approximation for the timing design in actual logic circuits, without significant errors even for very short "PTLs":

$$t_W \approx t_0(I_B) + l_P \tau_P \quad (1)$$

where τ_P , l_P , t_0 , and I_B are PTL delay per unit length, PTL length, the driver-receiver pair's switching delay when PTL length is zero, and bias current, respectively. In (1), only t_0 is dependent on bias current. t_0 extracted by the simulation is shown in Table II.

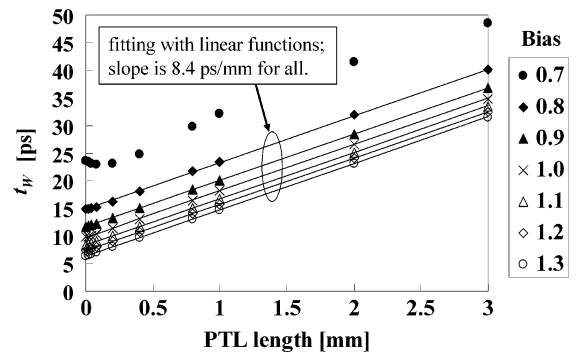


Fig. 8. Simulation result of PTL-length dependence of t_W for various bias values. Linear fitting functions having slope of 8.4 ps/mm are also shown for bias values from -20 to $+30\%$ of the designed value.

TABLE II
DEPENDENCE OF T_0 ON BIAS CURRENT

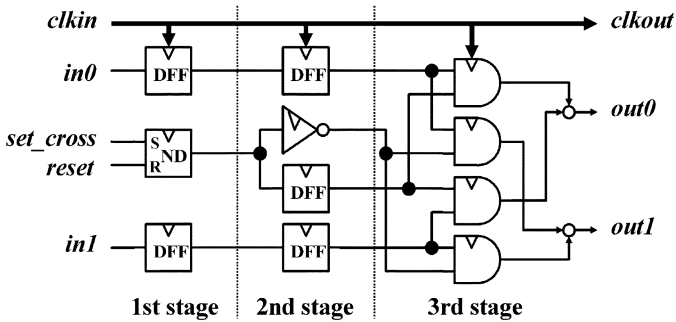
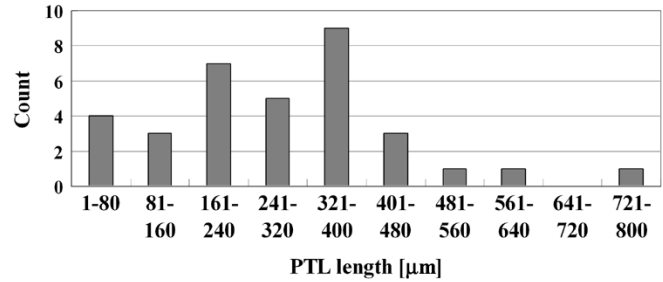
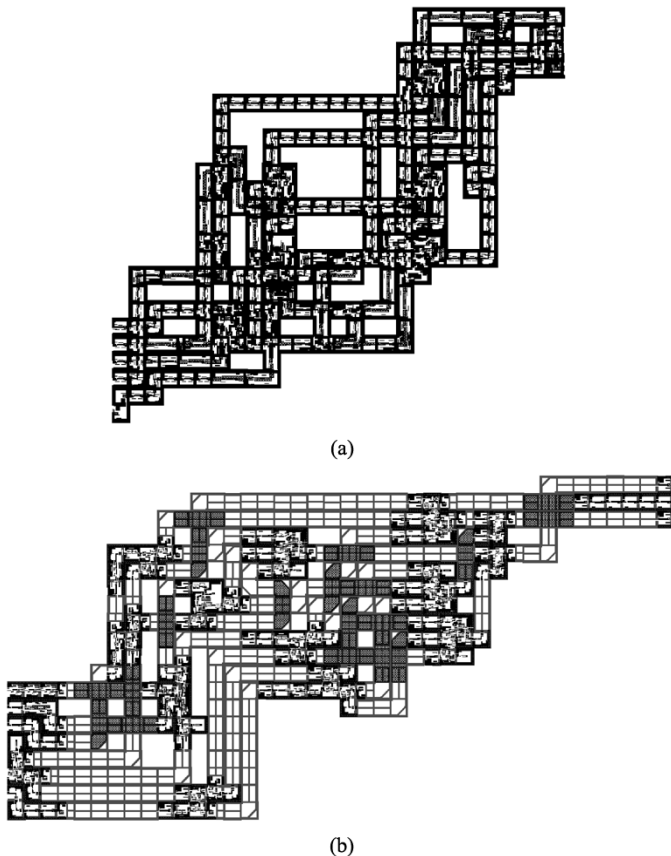
Bias current ^a	0.8	0.9	1.0	1.1	1.2	1.3
t_0 [ps]	14.9	11.6	9.8	8.3	7.3	6.4

^aNormalized by the designed value.

IV. 2×2 SWITCH USING PTLs

A. Design of the Switch

As an example, we applied our design method to a 2×2 switch circuit. The switch has two data inputs $in0$ and $in1$ and

Fig. 9. Circuit diagram of 2×2 switch circuit.Fig. 11. Distribution of lengths of PTLs used in 2×2 switch.Fig. 10. Layout of 2×2 switch circuit designed using (a) JTL gate-to-gate interconnection and (b) PTL gate-to-gate interconnection. Circuit sizes were (a) $1080 \mu\text{m} \times 960 \mu\text{m}$ and (b) $1600 \mu\text{m} \times 800 \mu\text{m}$.

two data outputs $out0$ and $out1$ (Fig. 9). The connection between the data inputs and data outputs is controlled by two control inputs set_cross and $reset$. If set_cross is input, the switch's function is set to "cross" and $in0$ and $in1$ are routed to $out1$ and $out0$, respectively. If $reset$ is input, the switch's function is set to "bar" and $in0$ and $in1$ are routed to $out0$ and $out1$, respectively. The switch circuit has 13 logic cells and three pipeline stages. Fig. 10(a) shows the layout of this switch designed using JTL interconnection [15]. The switch uses the concurrent-flow clocking scheme, and its correct operation was already demonstrated up to 40 GHz [15]. In this design, we set an interconnection constraint: the JTL interconnection from a logic cell to the

TABLE III
COMPARISON OF PTL-VERSION 2×2 SWITCH
WITH JTL-VERSION 2×2 SWITCH

	Logic	JTL	Splitter	D&R ^a	Inter-connection ^b	Total ^c
JJ Number						
JTL version	126	381	52	0	433	559
PTL version	126	70	63	106	239	365
Current [mA]						
JTL version	12.9	57.2	5.4	0	62.6	75.5
PTL version	12.9	10.7	6.3	15.6	32.6	45.5

^aNumber of JJs or current of driver-receiver pair.^bNumber of JJs or current of JTL, splitter, and driver-receiver pair.^cTotal number of JJs or total current of entire circuit.

next-stage logic cell can only go to the right or up. Under this constraint, any JTL interconnection between two points had approximately the same length regardless of how it was routed. This simplified timing adjustment, enabling us to reduce the number of JJs needed for timing adjustments.

Fig. 10(b) shows the layout of the switch designed with PTL gate-to-gate interconnections. In this design, we imposed the same interconnection constraint as that used in the JTL version [Fig. 10(a)]. We used 34 PTLs with a maximum PTL length of $728 \mu\text{m}$ and a minimum one of $20 \mu\text{m}$. There were 37 PTL crossings with a maximum of three crossings per PTL. Fig. 11 shows the distribution of the length of PTLs used in the switch.

We compared the PTL-version switch [Fig. 10(b)] with the JTL-version [Fig. 10(a)] to examine the effectiveness of PTL interconnection. For interconnection of which the length is comparable to or shorter than the single-stage-JTL length (40 or $80 \mu\text{m}$ in our cell library), PTLs have disadvantages because of the driver/receiver overhead. In our switch, about 12% of the interconnection uses such short PTLs (Fig. 11). However, in the PTL version, the number of JJs and current used for interconnection were reduced to 55% and 52% of those of the JTL version, respectively, in spite of the driver/receiver overhead (Table III). Using PTLs is thus a promising way to reduce the powering current, which may induce magnetic fields that cause large-scale circuit errors [16], and to reduce the timing error probability due to process variation.

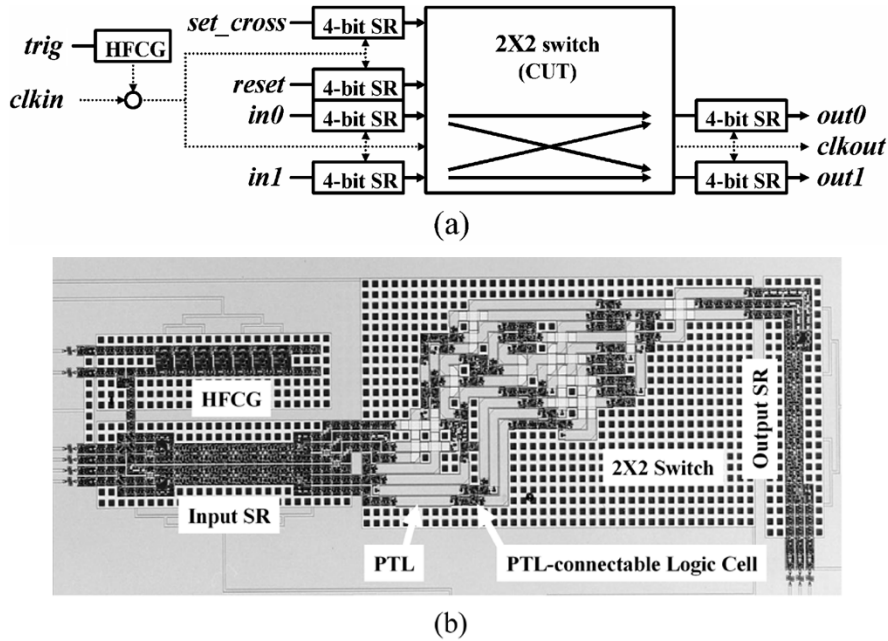


Fig. 12. (a) Circuit diagram and (b) microphotograph of fabricated test circuit for PTL-version 2×2 switch.

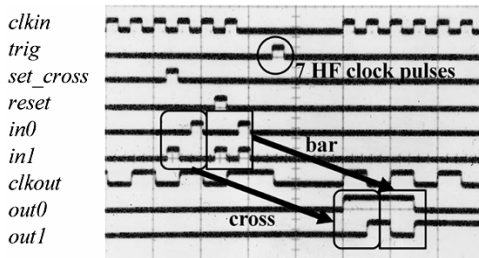


Fig. 13. Waveform of on-chip test for PTL-version 2×2 switch.

B. Experimentation With the Switch

We carried out an on-chip test [17], [18] for the 2×2 switch. The test circuit (Fig. 12) consisted of the 2×2 switch (the circuit under test), 4-bit input shift registers (SRs), 4-bit output SRs, and a high-frequency clock generator (HFCG). Fig. 13 shows the waveform of the test. A test pattern $in0 = (0101)$, $in1 = (1011)$, $set_cross = (1000)$, and $reset = (0010)$ was written into the input SRs at low speed. Then, seven high-frequency clock pulses were generated by applying $trig$ to the HFCG. With the seven clock pulses, the switch operated according to the test pattern, and the output of the switch was stored in the output SRs at high speed. Finally, the output data stored in the output SRs were read out at low speed. The test result was $out0 = (1001)$ and $out1 = (0111)$, which meant that the switch correctly routed the data inputs based on the control inputs. Note that in the output traces, either the rising edge or the falling edge corresponds to an observation of an SFQ pulse because we used T-flip-flop-based SFQ/dc converters to detect SFQ pulses. This correct routing was observed up to 50 GHz. The clock frequency was estimated by simulating the HFCG with the bias current applied in the experiment. The measured bias margin was $\pm 9.5\%$ at 40 GHz. The bias margin was limited by the NOT cell, which

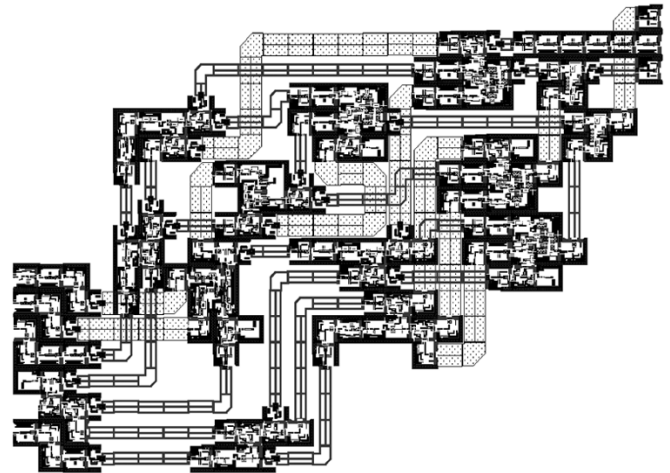


Fig. 14. Layout of PTL-version 2×2 switch assuming our advanced multilayer fabrication process. Circuit size was $1040 \mu\text{m} \times 720 \mu\text{m}$.

had the narrowest timing margin: ± 4 ps at 40 GHz. This test demonstrated the validity of our design.

V. DISCUSSION

The use of PTLs significantly reduces the number of JJs in SFQ logic circuits as explained in the previous section. However, this does not immediately mean that the use of PTLs will reduce the circuit area. In fact, the circuit area of the PTL-version 2×2 switch [Fig. 10(b)] was about 1.6 times that of the JTL version [Fig. 10(a)]. One reason for this drawback is the overhead of the driver and receiver. To reduce the overhead, we should reduce the number of JJs and the area of PTL-connectable logic cells. Another reason is the large area occupied by the PTL crossings. The crossing structure requires contact holes between the lower wiring layer and the upper wiring layer as shown in Fig. 5. As a result, the size of the PTL crossing became three times that of JTL crossing in our cell-based design. This

problem can be overcome, however, by increasing the number of Nb layers. Considering this, we have started developing an advanced multilayer fabrication process that has six Nb layers [19]. In this process, two Nb layers are available for PTLs and one Nb layer is available for the shield between PTLs. With this advanced process, we will be able to reduce the area for PTL crossing because contact holes will not be needed. Moreover, it will become possible to place PTLs above logic cells because we can place a shield between them. These improvements will significantly reduce the circuit area. Fig. 14 shows the layout of a PTL-version 2×2 switch designed with our advanced fabrication process. The circuit area is significantly reduced to 56% of that of the same circuit designed with our standard process [Fig. 10(b)]. The circuit area is about 72% of that of the JTL version [Fig. 10(a)]. Note that the PTL-connectable logic cells in Fig. 14 are the same as those in Fig. 10(b). By reducing the number of JJs and the area of these cells, we will be able to reduce the circuit area even further.

VI. CONCLUSION

We developed a method of designing SFQ logic circuits with gate-to-gate passive interconnections. We determined the basic properties, such as bias margins and timing parameters, for the PTL-connectable logic cells and the driver–receiver pair. The validity of our design method was demonstrated through an on-chip test of a 2×2 switch. The use of gate-to-gate passive interconnection significantly reduces the number of JJs and current of SFQ logic circuits. A drawback of gate-to-gate passive interconnection is the larger area in comparison to that of JTL interconnection. However, the problem can be overcome by increasing the number of Nb layers.

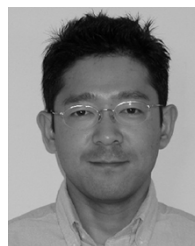
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