20 GHz Operation of Bit-Serial Handshaking Systems Using Asynchronous SFQ Logic Circuits

Maki Ito, Kenji Kawasaki, Nobuyuki Yoshikawa, Akira Fujimaki, Hirotaka Terai, and Shinich Yorozu

***Abstract*—Synchronous design is generally used in SFQ digital systems at present. In large-scale SFQ digital systems, however, the introduction of asynchronous design is required due to the large clock skew in the clock distribution network and complexity in the timing design at high clock rate. We have proposed a hierarchical design approach using asynchronous SFQ circuits with handshaking protocol for asynchronous data transfer. In our asynchronous approach, each circuit module is designed based on a data driven self-timed (DDST) architecture. A handshaking protocol is also used to ensure the logical ordering in data communication between the modules, where we have adopted bit-serial architecture to reduce the communication costs in handshaking. One issues in the bit-serial handshaking (BSHS) system is the synchronization of the input data when the module has multiple input ports. In this study, we have designed an SFQ BSHS system with multiple input ports, where Muller C-elements is used to synchronize the multiple input data. We have designed and implemented a BSHS half adder using NEC 2.5 $\mathrm{kA/cm^2}$ Nb standard process to demonstrate asynchronous addition of two input data at high speed. We have successfully confirmed its correct operation at about 20 GHz.**

***Index Terms*—Adder, asynchronous system, bit-serial architecture, data-driven self-timing, handshaking, SFQ circuit.**

I. Introduction

At present time, a synchronous approach is generally used in designing SFQ digital systems, although an asynchronous approach can also be used [1]. In large-scale SFQ digital systems, the distribution of globally synchronous clock signals at high frequency becomes an awkward task due to large clock skew in the clock distribution network. In order to solve the timing issues, we have been developing the asynchronous SFQ circuit systems based on data-driven self-timing (DDST) [2].

In the DDST architecture, conventional synchronous clocking is used just inside the circuit module. Between the modules, dual-rail lines are used to transfer complementary data, from which the local clock is reproduced by using a logical OR function. In our asynchronous design hierarchy, handshaking protocol is also used to prevent the data collision between the DDST modules and to ensure logical ordering [2]. However, large cost in the handshaking is commonly a disadvantage in handshaking system. A large overhead in the circuit size and the delay make it not so popular in present CMOS circuit design. However in the SFQ circuits the situation is somewhat different. Due to the self-resetting nature of the SFQ pulse, request and acknowledgment signals are simply produced in the SFQ circuits. A large overhead is also relatively reduced by adopting the bit-serial architecture, where the data transfer is performed in the unit of bit-serial data during a single handshaking procedure. In this case high-throughput nature

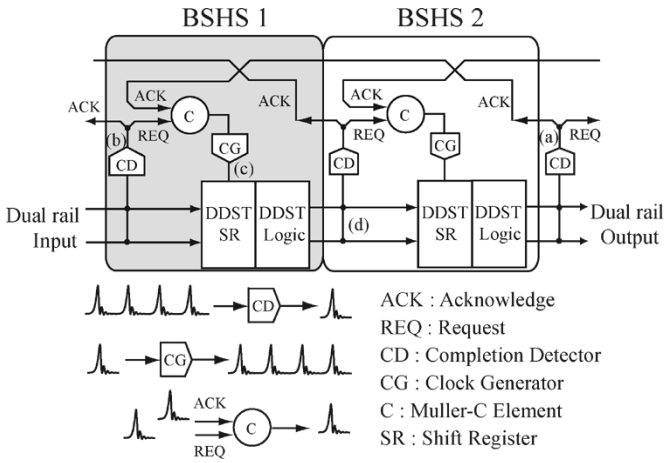

Fig. 1. A block diagram of the BSHS pipelined system.

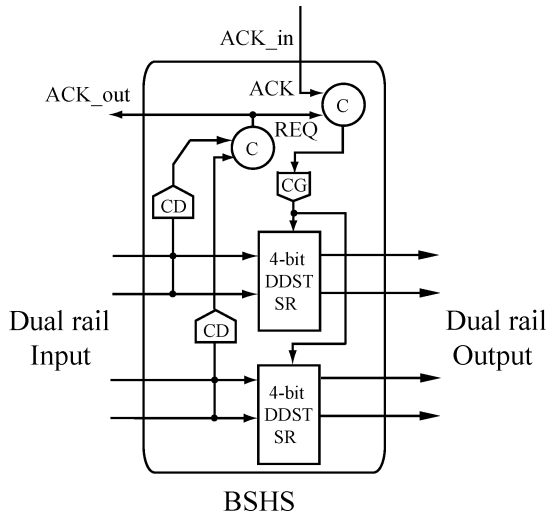

Fig. 2. A block diagram of a two-input BSHS module.

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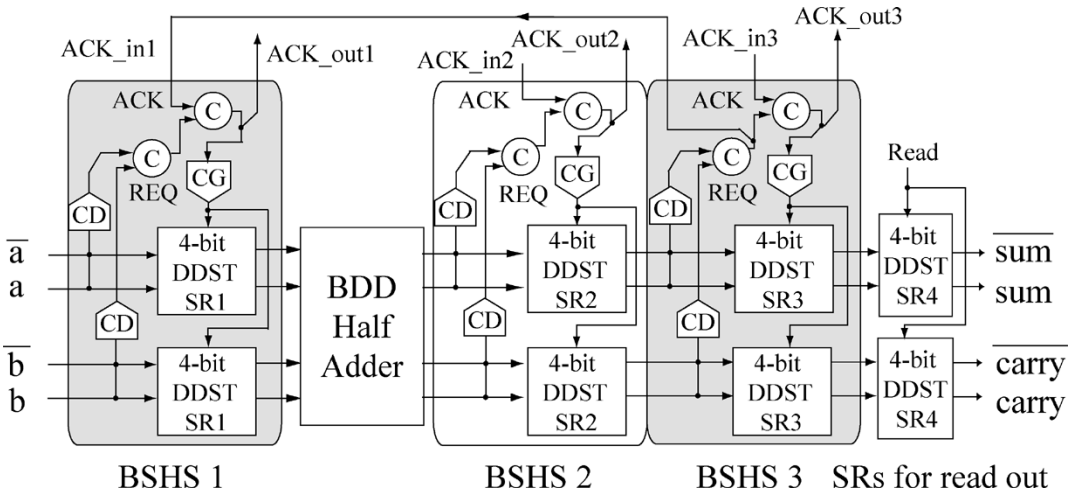

Fig. 3. A test system for a two-input bit-serial hand shaking system, which is composed of three stages of the BSHS modules, one BDD half adder and two shift registers for read out.

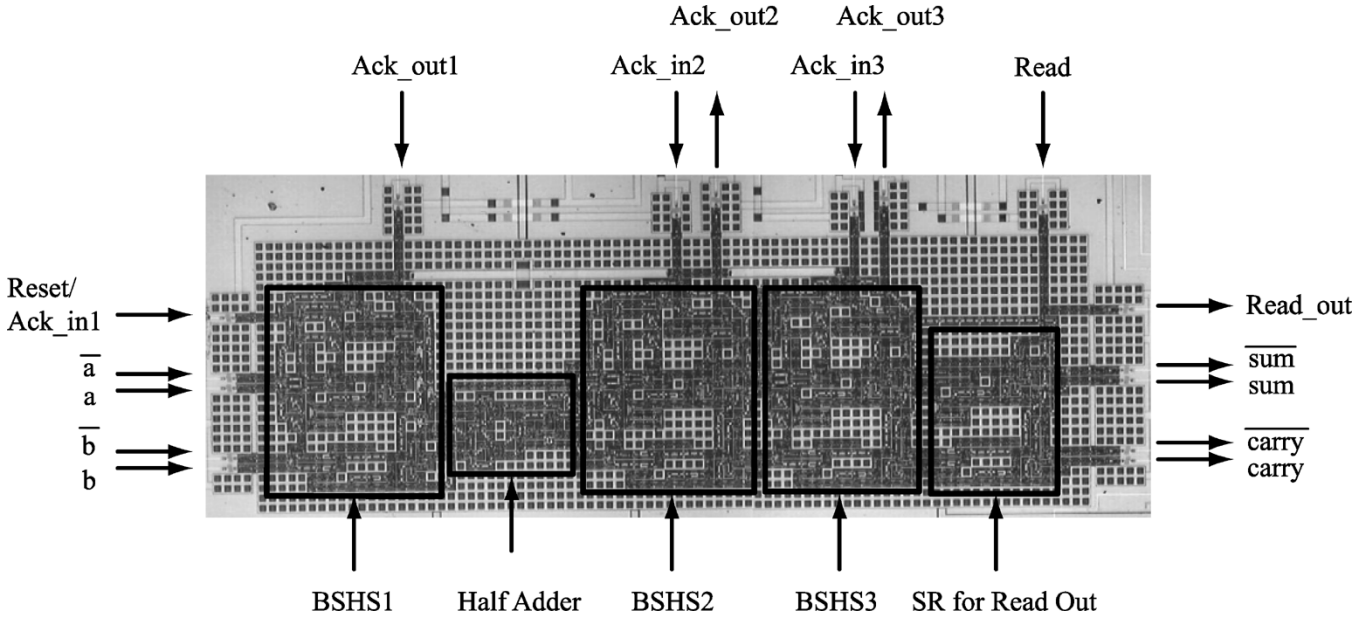

Fig. 4. A photomicrograph of the test system.

of the SFQ circuits is effectively utilized in the handshaking system. In our previous study, we have designed a bit-serial handshaking (BSHS) pipelined system and demonstrated the asynchronous transfer of bit-serial data at high speed [3].

When we make a large bit-serial handshaking (BSHS) system, the module sometimes has multiple input ports. In this case synchronization of multiple data inputs has to be ensured even at high clock rate. In this study, we have investigated the BSHS system with multiple input ports. We have designed and implemented a BSHS half-adder, which is composed of a 1-bit DDST half adder and BSHS modules to demonstrate high-speed addition of two data inputs at high speed.

II. Bit Serial Hand Shaking Systems

Fig. 1 shows a block diagram of the BSHS pipelined system, which was proposed earlier [2]. The module is composed of a DDST shift register (DDST SR), a completion detector (CD), a clock generator (CG), a Muller C-element (C) and a DDST logic block. The DDST SR keeps input bit-serial data and outputs them when high-speed clock pulses are applied from the CG. The CG generates high-speed clock pulses of the finite length when a trigger pulse is applied. The CD is composed of several stages of T flip-flops, which counts the input pulses and detects the completion of the data input. The Muller C-element generates an SFQ pulse if SFQ pulses are applied to its both input nodes. In this pipelined system, the transfer of the data between the modules is carried out as follows.

In the initial state, both BSHS modules (BSHS 1 and BSHS 2) are supposed to be empty. Because the CD at the output of the BSHS 2 has already detected a data output event ((a) in Fig. 1), ACK (acknowledge) of the Muller C-element in the BSHS 1 is enabled. If bit-serial data is applied to the system, the end of the data causes the generation of REQ (request) pulse ((b) in Fig. 1). The Muller C-element sends a trigger pulse to the CG. Then, the data in the DDST SR are pushed out by the high-speed

TABLE I
TIMING PARAMETERS OF THE BSHS MODULE

Timing Parameters	Times (ps)
ACK_in to Data_out	348
Data_in to Data_out	682
Data_in to ACK_out	333

clock from the CG ((c) in Fig. 1). These data are computed in the DDST logic block and sent to the next BSHS module ((d) in Fig. 1).

III. BIT SERIAL HAND SHAKING SYSTEM WITH MULTIPLE INPUTS

The above-mentioned BSHS pipelined system is a simple chain of BSHS models and there are no branch and confluence of the data flow. In the past we developed a circuit with one-bit hand-shaking channel. Fig. 2 shows a straightforward generalization of this circuit for two-input hand-shaking protocol, where a Muller C-element is used to make synchronization of two data inputs. A REQ signal is issued if both inputs arrive to the BSHS module. The BSHS module with multiple data inputs is constructed in the same way by simply adding the Muller C-element. The asynchronous transfer of the data to multiple outputs is also possible by receiving all ACK signals from the following BSHS modules and synchronizing them using the Muller C-elements.

IV. IMPLEMENTATION AND HIGH-SPEED TEST OF A BIT SERIAL HAND SHAKING SYSTEM

We have designed a 4-bit BSHS system with two asynchronous inputs, in which one-bit half adder is used as a DDST logic block. The circuit is implemented by using the CONNECT cell library [4] and the NEC 2.5 $\mathrm{kA/cm^2}$ Nb standard process [5]. Fig. 3 shows a block diagram of the system, which is composed of three stages of BSHS modules and a dual rail one-bit DDST half adder. In this demonstration we used the DDST half adder based on a binary decision diagram (BDD) [6], which is one way to realize DDST SFQ circuits. Passive transmission lines (PTLs) [7], [8] are used for the transfer of ACK signals from the module BSHS 3 to the BSHS 1 in order to reduce the handshaking delay. Two shift registers (SRs) are added to the output of the system to read out the high-speed output data at low speed.

The DC bias margin of the system is estimated to be $-20\% \sim +30\%$ by using the Verilog logic simulator, which has been developed to estimate the DC bias margins of SFQ circuits [9]. The target frequency is 20 GHz. Table I lists the some important timing parameters of the BSHS module shown in Fig. 2. Fig. 4 shows a photograph of the test system. Its size and total junction count is $1,300\,\mu\mathrm{m} \times 4,760\,\mu\mathrm{m}$ and 2,565, respectively.

Fig. 5 shows the test results of the BSHS half adder system. The test sequence is as follows. Initially, ACK_in1 is applied and the dual-rail serial data a(0011), b(0101) are loaded into the BSHS 1. These data are immediately added by the BDD half adder and the results of the addition is moved to the BSHS 2. Then the next dual-rail serial data a(1001), b(1010) are loaded into the BSHS 1. In this situation if ACK_in2 is applied, the data on the BSHS 2 is moved to the BSHS 3. At the same time, a ACK_in1 signal, which acknowledges the completion of the data output on the BSHS 2, is sent from the BSHS 3 to the BSHS 1. Because the data has already stored in the BSHS 1 this time, the data on the BSHS 1 is moved to the BSHS 2 automatically. These data transfer caused by the handshaking is performed at about 20 GHz, which is determined by the frequency of the clock generator. Finally by applying ACK_in3,

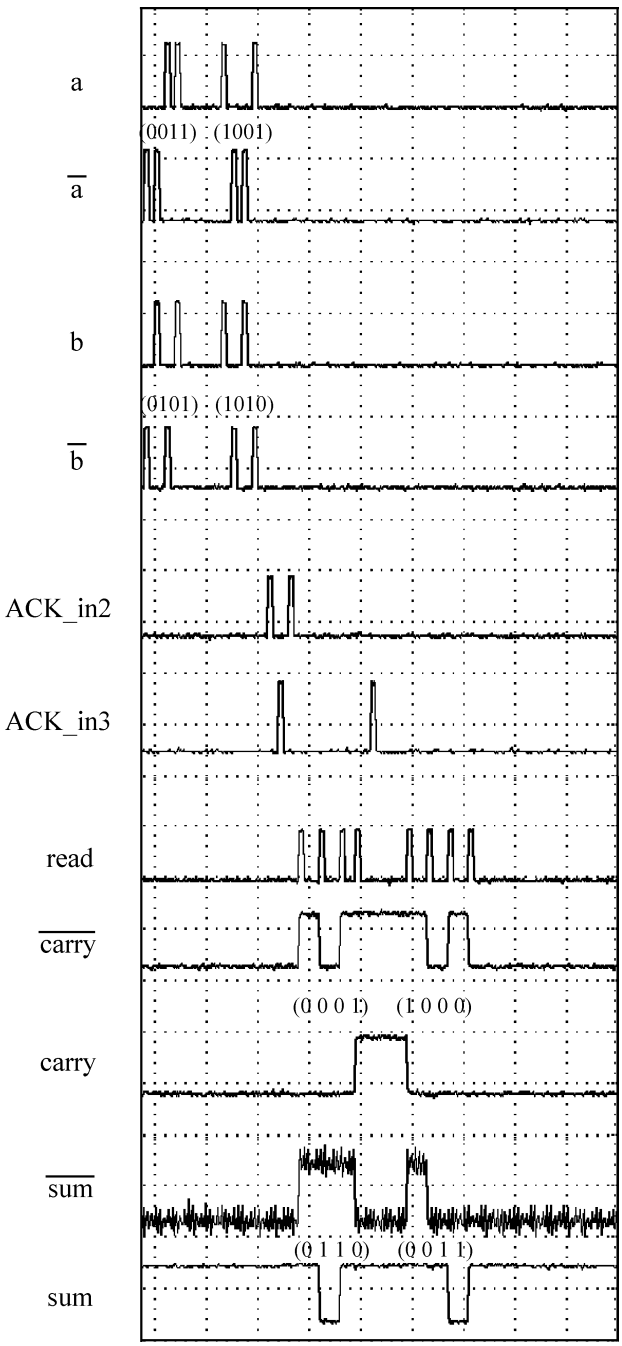

Fig. 5. Test results of the BSHS half adder system shown in Fig. 3. The scales of y-axis for the input (a, a_bar, b, b_bar, ACK_in2, ACK_in3, and read) is 20 mV/div and the scales for the output (carry_bar, carry, sum_bar, and sum) is 200 $\mu\mathrm{V/div}$. The rising edges in the input signals correspond to the inputs of SFQ pulses, and the transitions in the output signals are the output of SFQ pulses. The scale of x-axis is 10 ms/div.

the data on the BSHS 3 is moved to the output SRs. By applying the Read signal, the data on the SRs is outputted, which is expected to be sum(0110) and carry(0001). Successive inputs of ACK_in2, ACK_in3 and Read signals, also result in the read out of sum(0011) and carry(1000).

Fig. 5 illustrates our experiments with asynchronous summation of 4-bit data at about 20 GHz using the bit-serial hand shaking. The DC bias margin was found to be $+-$ 5.5% from the test.

V. Conclusion

We have investigated an SFQ bit-serial handshaking (BSHS) system with multiple inputs. The synchronization of asynchronous multiple inputs is performed by using Muller C-elements. In order to demonstrate the validity of the proposed asynchronous design approach, we have designed and implemented a BSHS half adder using Nb 2.5 $\mathrm{kA/cm^2}$ standard process and CONNECT cell library. The number of Josephson junction in the system is about 2500, and its bias current is about 333 mA. Passive transmission lines (PTLs) are used for sending acknowledgment signals. This results in the reduction of about 16% of the handshaking delay. The high-speed addition of asynchronous 4-bit data is successfully demonstrated at the data transfer rate of about 20 GHz. The chip yield for the successful operation was found to be about 30%. It was also found from the experiment that the initialization of the system is important to ensure the correct operation of the asynchronous system.

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