Title of article:

Access-Time Measurements of the Josephson-CMOS Hybrid Memory using Single Flux Quantum Circuits

Authors and addresses:

N. Yoshikawa[1], M. Tokuda[1], T. Tomida[1], H. Kojima[1], K. Fujiwara[2], Q. Liu[2] and T. Van Duzer[2]

[1]Department of Electrical and Computer Engineering, Yokohama National University, Yokohama, 240-8501, Japan

[2]Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA

Corresponding author:

Nobuyuki Yoshikawa

Department of Electrical and Computer Engineering, Yokohama National University, 79-5 Tokiwadai, Yokohama, 240-8501, Japan

Phone: +81-45-339-4259

Fax: +81-45-338-1157

E-mail: yoshi@yoshilab.dnj.ynu.ac.jp

Short title:

Access-Time Measurements of the Josephson-CMOS Hybrid Memory using SFQ Circuits

Classification numbers:

PACS: 85.25.Hv

Abstract

We have measured access time of a 16-kbit Josephson-CMOS hybrid memory by using an SFQ delay measurement system. The delay measurement system is composed of a Josephson latching driver to generate input signals for the memory, an SFQ clock generator and counter to measure the time interval, and a current sense circuit to detect the current output from the memory. The time resolution of the system corresponds to a clock period of the clock generator, which is 50 ps in our design. In these preliminary measurements, we have observed a memory access time of about 4 ns, where the parasitic capacitance of the bonding pad of the Josephson chip limits the access time at present. This is the first demonstration of the access time measurement of a complete Josephson-CMOS hybrid memory.

1. Introduction

Hybridization of high-speed, low-power single-flux-quantum (SFQ) circuits [1] and high-density CMOS circuits is a promising technology for realizing future high-performance digital systems. One application is a Josephson-CMOS hybrid memory [2], which is composed of a high-density CMOS memory cell array and high-speed Josephson current sense circuits. Due to low driving ability and low integration density of SFQ circuits, it is not easy to achieve a large-scale memory by using pure SFQ circuits at present. The hybrid memory is, thus, a potential candidate to overcome a memory bottleneck in high-performance SFQ digital systems. Furthermore, we can expect improvement in CMOS device characteristics in terms of the speed and the current leakage when cooling CMOS circuits down to cryogenic temperatures.

In the previous study, we have developed a 4.2 K CMOS device model and reported near-infinite retention time of the memory cell at low temperatures [3]. We have also demonstrated the complete operation of the hybrid memory system by low-speed tests [4]. In this study, we have implemented a delay measurement system using SFQ circuits and measured the access time of the hybrid memory with high time resolution.

2. Josephson-CMOS Hybrid Memory

Figure 1(a) shows the architecture of the 16-kb Josephson-CMOS hybrid memory examined in this study. It consists of an SFQ-CMOS interface, a CMOS decoder, a CMOS memory cell array and a Josephson current-sense circuit. A circuit schematic of the memory cell is shown in Fig. 1(b). It is a conventional three-transistor DRAM cell, but operates as an SRAM cell at low temperature due to its near-infinite retention time. The Josephson current-sense circuit, which is a Josephson balanced comparator, detects the output current from RBL through the CMOS bit select decoder at high speed [4]. The SFQ-CMOS interface consists of a Josephson latching driver, which is a parallel connection of double 15-junction stacks [5], and CMOS differential amplifiers. The latching drivers amplify submillivolt-level SFQ pulses to 40 mV-level signals, which are further amplified by CMOS differential amplifiers to volt-level signals [3]. In addition to the CMOS differential amplifier, we have a more complex option, a Josephson-CMOS hybrid amplifier [4], which is faster and dissipates less power than the CMOS differential amplifier.

The main features of the hybrid memory are small access time due to high-speed operations of the Josephson current-sense circuit and the low-temperature CMOS devices, and the nonvolatile and nondestructive operations owing to the three-transistor memory cell operating at low temperatures. The access time of the 16 kb memory is estimated to be 700 ps and 1.2 ns assuming Hitachi 0.18 μm and Rohm 0.35 μm CMOS processes, respectively, by circuit simulation using our 4 K modification of the BSIM3 model [6].

3. Test System

A block diagram of the access time measurement system is shown in Fig. 2. The system consists of a 20 GHz SFQ clock generator (CG) and an SFQ counter. In operation, an SFQ "Start" signal is applied first to the CG; it is simultaneously amplified by the latching driver and sent to the CMOS part of the hybrid memory as an address signal. Then, an output signal from the memory is detected by the Josephson current-sense circuit, and converted to an SFQ pulse, which stops the operation of the CG. In the meantime, a number of SFQ pulses generated from the CG is counted by the SFQ counter. This number corresponds to the access time of the hybrid memory. The time resolution of the delay measurement system corresponds to the clock period, which is designed to be 50 ps in this system.

Fig. 3 is a photograph of the CMOS and Josephson chips mounted on a chip carrier. Wire bonding is used to connect the chips each other in this preliminary test. The CMOS chip was fabricated using the Rohm 0.35 μm CMOS process. The Josephson chip was designed using the CONNECT cell library [7] and fabricated using the NEC 2.5 kA/cm^2 Nb standard process [8].

4. Results and Discussion

A low-speed test result of the 16-kbit hybrid memory is shown in Fig. 4. In the measurement, a datum "1" is read out from the memory system by applying the row address data [10000000] to the memory, where only a datum "1" of the MSB is generated by SFQ circuits while keeping the other bits to be zero. In the test the "Start" signal, which is not shown in the figure, is first applied to the measurement system, which induces the upward transitions in the "Address" signal, and also in the "Output" signal of the memory. One can see that upward transition appears in the waveform of the "Stop" signal, which corresponds to the output of an SFQ pulse from the memory system. The following downward transition in the "Stop" signal arises from the input of the "External clock", which is applied to stop the clock generator completely. Finally the "Address" and "Output" signals return to zero by removing the AC bias to the Josephson latching driver. Note that successive inputs of the "External clock" are carried out to check the complete operation of the current-sense circuit in the measurement.

A result of the access time measurement is shown in Fig. 5, where the data stored in the counter is read out by applying the "Read" signal to the counter. One can see that the data "000000001000101" are obtained. Because the clock period of the clock generator is calculated to be about 60 ps in the bias condition of this measurement, the access time is estimated to be 4.1 ns. In the access time measurement, we have observed a distribution of the value of the access time when we repeat the measurement many times. In order to examine the distribution of the access time, we have made a histogram of the access time as shown in Fig. 6, where measurements are repeated 10000 times. It is found from the histogram that a sharp peak, which is followed by a broad peak,

appears at 4.2 ps. These double peaks are thought to be arising form the discrete amplitude fluctuation in the output voltage of the Josephson latching driver. The measurement of the output waveform of the latching driver indicated that there were two stable states whose amplitudes were about 30 mV and 40 mV in this sample due to the imperfect switching of junctions in the stack. This voltage fluctuation may cause large variations in the delay of the CMOS amplifier because its delay is extremely increased when the input voltage becomes smaller. The circuit simulation shows that the delay of CMOS amplifier becomes larger than 2 ns when the input voltage amplitude is less 20 mV for example.

The measured access time of 4.2 ns is, however, still much larger than the value, ~ 1.2 ns, obtained from the circuit simulation assuming the Rohm 0.35 μm CMOS process. We believe that this large delay is caused by the large parasitic capacitance at the bonding pad of the Josephson chip because we did not remove the ground plane underneath the bonding pad. The circuit simulation taking account of the parasitic capacitance at the bonding pad, which is estimated to be about 15 pF for our 300μm-square pads, shows that the access time is increased up to 3.6 ns, which coincides well with the test results.

5. Conclusion

We have measured the access time of the Josephson-CMOS hybrid memory by the SFQ delay measurement system. The measured access time was about 4 ns. Though the obtained value is larger than the theoretical access time due to the large parasitic capacitance at the bonding pad, This is the first demonstration of the access time measurement of the Josephson-CMOS hybrid memory system using SFQ circuits.

Acknowledgement

The part of the work at Yokohama was supported by VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with Cadence Design Systems, Inc. and Synopsis, Inc., and also supported by the NEDO through ISTEC as Collaborative Research and Superconductors Network Device Project. The VLSI chip in this study has been fabricated in the chip fabrication program of VDEC in collaboration with Rohm Corporation and Toppan Printing Corporation, and Hitachi Ltd. and Dai Nippon Printing Corporation.

The work at Berkeley was supported by the Office of Naval Research under Grant No. N00014-03-1-0065.

References

[1] Likharev K K and Semenov V K 1991 *IEEE Trans. Appl. Superconduct.,* **1** 3-28

[2] Ghoshal U, Hebert D and Van Duzer T 1993 *1993 ISSCC Digest of Technical Papers* **33** 54-55

[3] Yoshikawa N, Tomida T, Tokuda M, Liu Q, Meng X, Whiteley S R and Van Duzer T 2005 *IEEE Trans. Appl Supercond* **15** 267-271

[4] Liu Q, Van Duzer T, Meng, X, Whiteley S R, Fujiwara K, Tomida T, Tokuda K and Yoshikawa N 2005 *IEEE Trans. Appl Supercond* **15** 415-418

[5] Suzuki H and Imamura T 1990 *IEEE Trans on electron device*, **37**, 2399-2405

[6] BSIM3v3.2 MOSFET Model User's Manual, Department of Electrical Engineering and Computer Science, University of California, Berkeley, 1998

[7] Nagasawa S, Hashimoto Y, Numata H and Tahara S 1995 *IEEE Trans. Appl. Supercond* **5** 2447-2452

[8] Yorozu S, Kameda Y, Terai H, Fujimaki A, Yamada T and Tahara S 2002 Physica C **378-381** 1471-1474

Figure Captions

Fig. 1. (a) Architecture and (b) memory cell structure of the Josephson- CMOS hybrid memory.

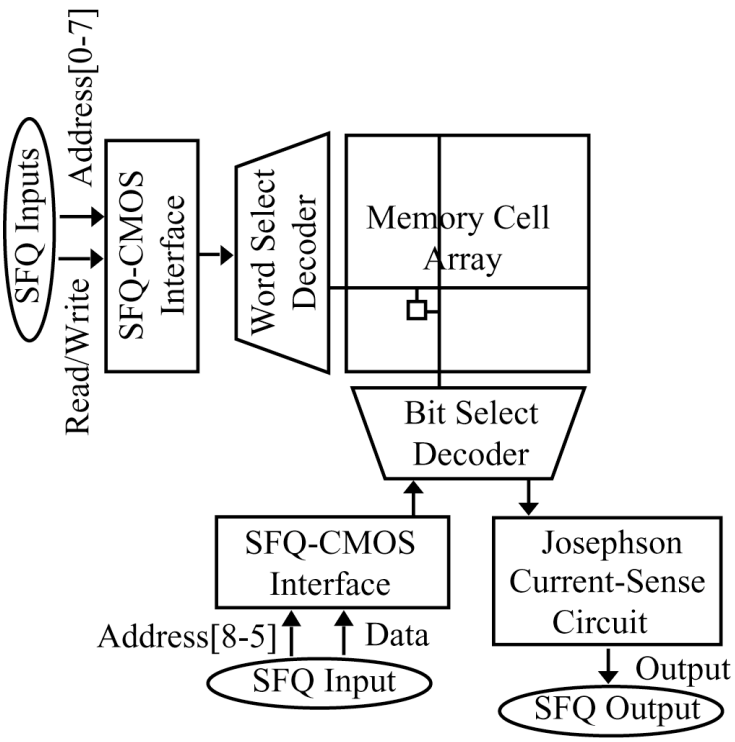
Fig. 2. A block diagram of an access time measurement system.

Fig. 3 The photograph of the CMOS chip and the Josephson chip. Die size of the CMOS and Josephson chips are 3 mm x 3 mm and 5 mm x 5 mm, respectively.

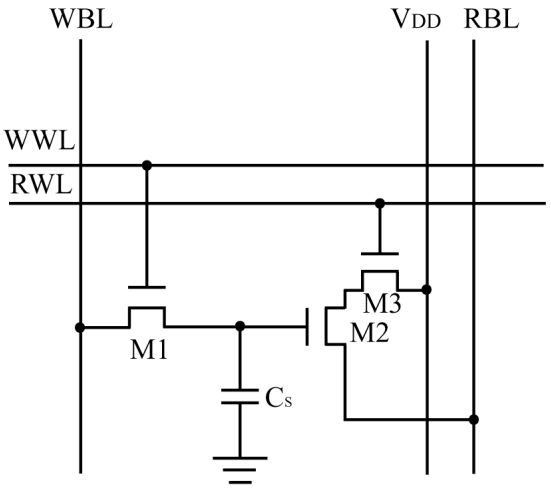
Fig. 4. A low-speed test result of 16-kbit hybrid memory system at 4.2K. Transitions in the “Stop” signal correspond to the output of the SFQ pulses.

Fig. 5. A result of the access time measurement, where the data stored in the counter is read out bit-serially from the most significant bit (MSB) by applying the “Read” signal to the counter. Transitions in the “Stop” and “Counter_out” signals correspond to the output of the SFQ pulses.

Fig. 6. The histogram of the access time measured by the SFQ delay measurement system.


SFQ Inputs
Address[0-7]
Read/Write
SFQ-CMOS Interface
Word Select Decoder
Memory Cell Array
Bit Select Decoder
SFQ-CMOS Interface
Josephson Current-Sense Circuit
Address[8-5]
Data
SFQ Input
Output
SFQ Output

(a)


WBL
VDD
RBL
WWL
RWL
M1
M2
M3
Cs

(b)

Fig. 1

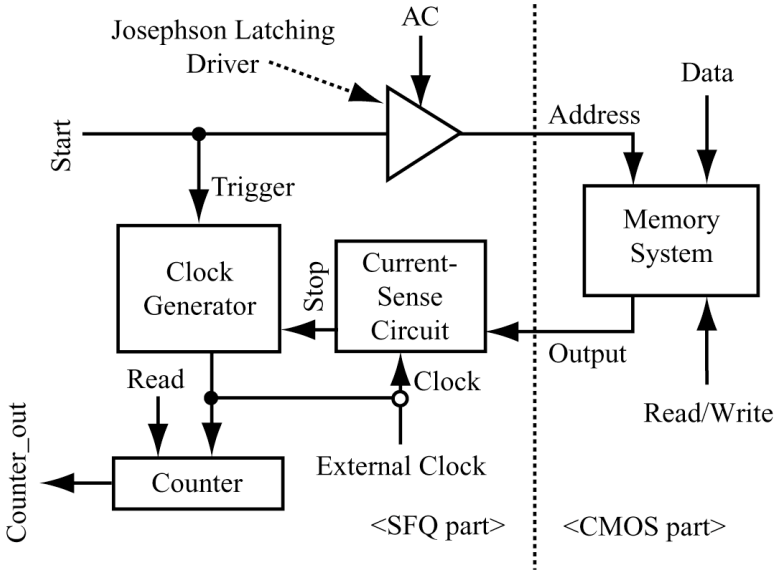

Josephson Latching
Driver
AC
Data
Address
Start
Trigger
Memory
System
Clock
Generator
Stop
Current-
Sense
Circuit
Output
Read
Clock
Read/Write
Counter_out
Counter
External Clock
<SFQ part>
<CMOS part>

Fig. 2

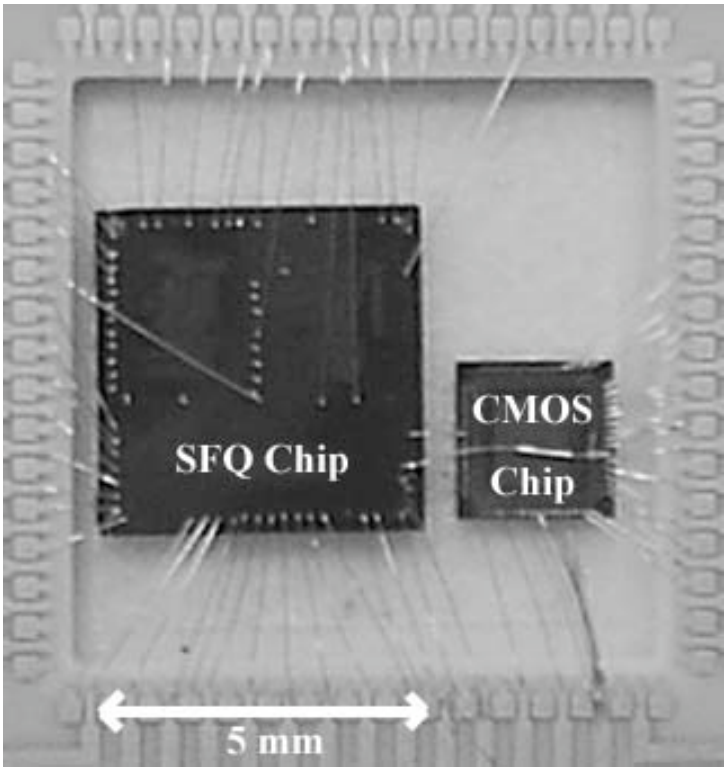


Fig. 3

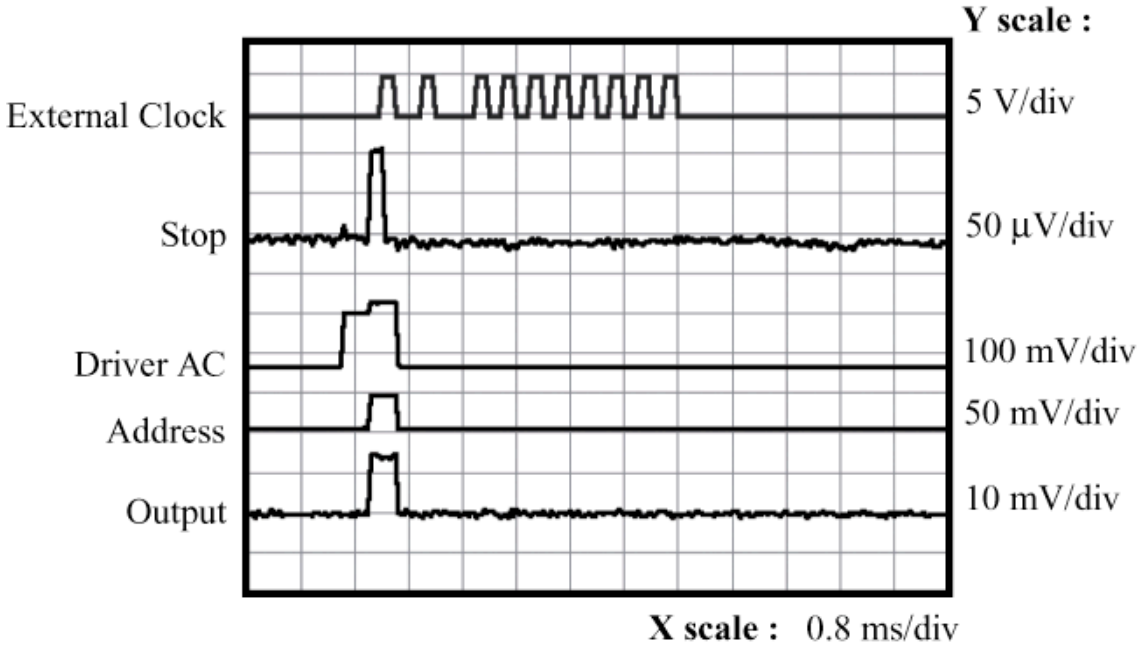

Y scale :
External Clock
5 V/div
Stop
50 µV/div
Driver AC
100 mV/div
Address
50 mV/div
Output
10 mV/div
X scale : 0.8 ms/div

Fig. 4

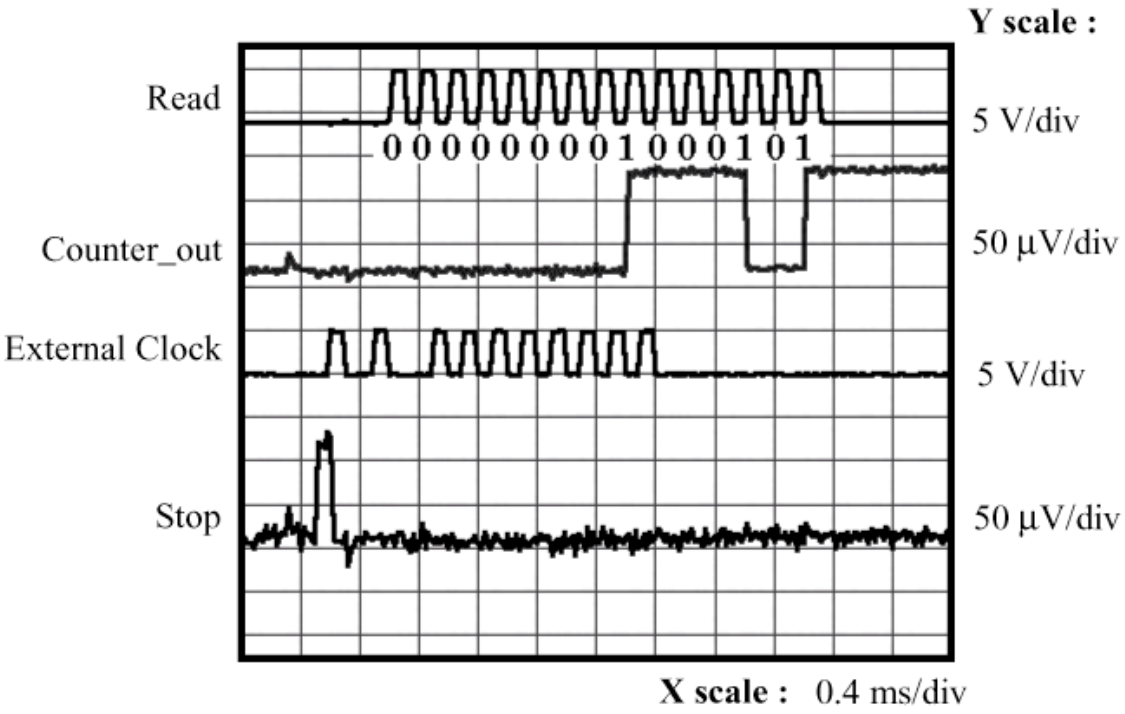

Y scale :
Read
0 0 0 0 0 0 0 0 1 0 0 0 1 0 1
5 V/div
Counter_out
50 µV/div
External Clock
5 V/div
Stop
50 µV/div
X scale : 0.4 ms/div

Fig. 5

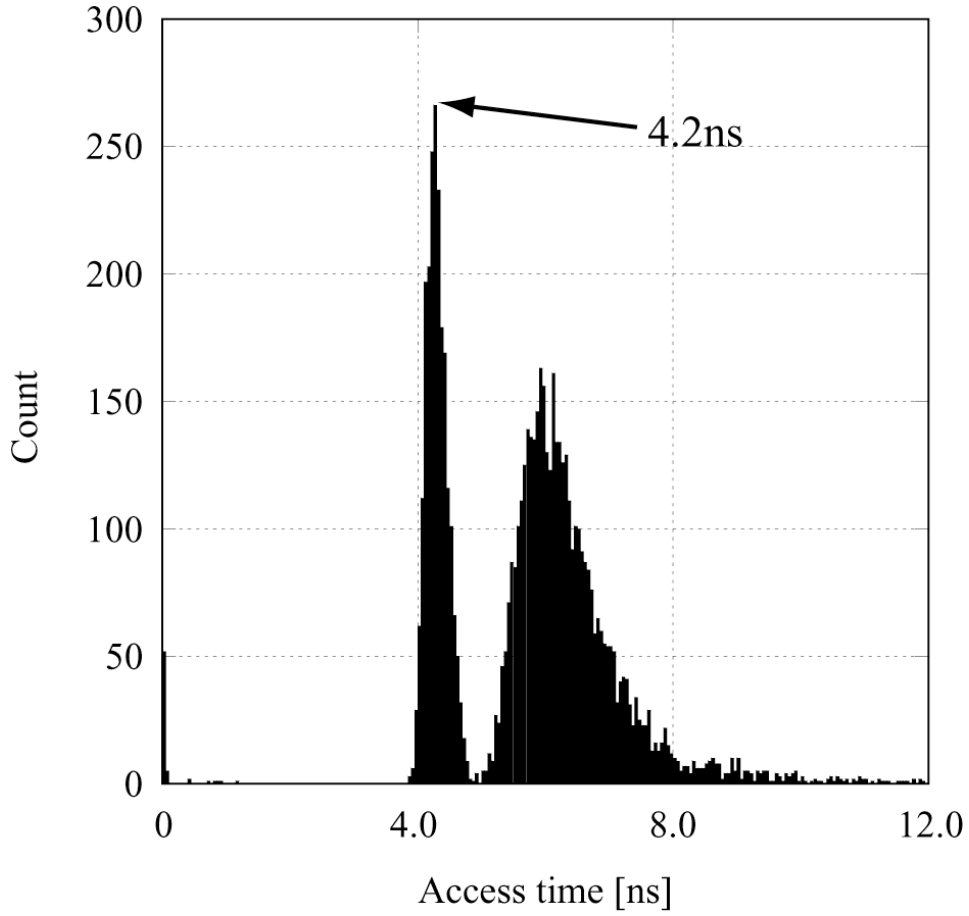


Fig. 6