ACS APPLIED ELECTRONIC MATERIALS

pubs.acs.org/acsaelm
Article

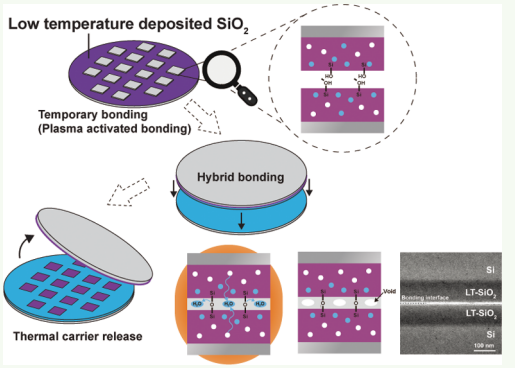
Temporary Direct Bonding by Low Temperature Deposited SiO_2 for Chiplet Applications

Koki Onishi, Hayato Kitagawa, Shunsuke Teranishi, Akira Uedono, and Fumihiro Inoue*

Cite This: ACS Appl. Electron. Mater. 2024, 6, 2449−2456
Read Online

ACCESS | Metrics & More | Article Recommendations

ABSTRACT: Die-to-wafer hybrid bonding is a crucial technology in advanced chiplet integration systems. Temporary die bonding on wafers and subsequent debonding are key aspects of this process. However, conventional polymer-based temporary bonding techniques involve several challenges such as issues related to the accurate placement of the die. Although direct bonding is a promising technology, such processes normally involve permanent bonds. The present study demonstrates an innovative temporary bonding method based on plasma-activated direct bonding and examines the associated bonding/debonding mechanisms. In this work, a dielectric bonding film was deposited at a relatively low temperature by chemical vapor deposition. This method offers several advantages, including high alignment accuracy, limited risk of die shift, and cost reduction based on removal of the carrier wafer grinding process. Wafer bonding was performed with SiO_2 films deposited at low temperatures, and voids were formed at the bonding interfaces during postbond annealing. The bonding energy was sufficiently low even after annealing to allow wafer pairs to be released as a consequence of voids serving as initiation points for debonding. Desorption gas analysis established that the SiO_2 films absorbed significant moisture from ambient air, which was the root cause of void formation. Die-to-wafer bonding tests confirmed the formation of voids at the bonding interfaces. This dielectric is likely to have applications as a temporary bonding material in chiplet integration systems.



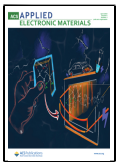
KEYWORDS: *Thermal releasable dielectric film, Temporary bonding, Plasma activated bonding, Hybrid bonding, chiplet*

INTRODUCTION

High-performance semiconductor devices are a necessary component of systems such as artificial intelligence, cloud networks (that is, data centers), and edge devices. The concept of chiplets has received a great deal of attention as a means of reducing production costs while improving yield, power efficiency and performance.[1−5] Compared with systems on a chip and so-called monolithic chip devices, chiplet integration can provide improved yields by selecting known-good die (KGD) and can also adopt dies fabricated using different technical nodes in the system. These factors can lead to cost reduction and reduce the time from research and development to the marketing stage. Furthermore, because the chiplet concept allows more design flexibility, such systems can result in increased integration density, shorter interconnections, and lower power consumption.

Chiplet integration typically requires a reduction of the vertical interconnection pitch.[1−5] Although the flip-chip micro bump technique has commonly been employed during die-to-wafer (D2W) bonding, this technology cannot ensure the alignment tolerance required for a pitch of less than 2 μm during thermal compression. In the case of D2W interactions involving finer pitches, hybrid bonding, in which dielectric layers are bonded with Cu pads in the absence of adhesive, can be employed. In fact, this approach is currently used to fabricate devices such as CMOS image sensors along with NAND and high bandwidth memory units based on wafer-to-wafer (W2W) bonding.[2−10] Hybrid bonding is also expected to have applications in D2W integration, although D2W hybrid bonding involves technological challenges. Examples of such challenges include die-level cleaning, activation, die handling, and balancing high alignment accuracy with throughput. At present, D2W hybrid bonders, which can perform the direct placement of hybrid bonding, have insufficient levels of particle, throughput, and Q-time control. These tools are surprisingly improving performance; therefore, the straightforward integration of direct placement might be a major technique in the future. Nevertheless, the mitigation method for the integration would be the mainstream for a while until

Received: January 18, 2024
Revised: March 20, 2024
Accepted: March 21, 2024
Published: April 1, 2024



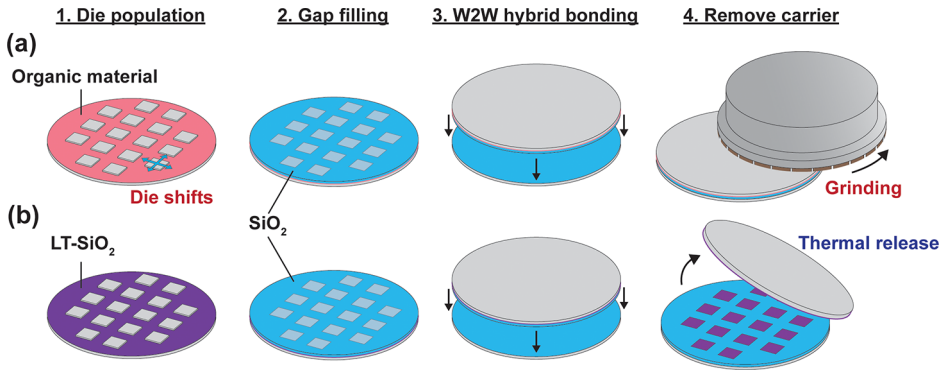


Figure 1. D2W integration processes using (a) an organic material and (b) LT-SiO_2 as the temporary bonding interface.

the bonders and other processes become matured. In recent years, processes with a temporary die placement on the carrier wafer have been proposed as the mitigation method.[1,5−9] The advantage of such processes is that well-developed wafer-level tools can be used for die cleaning, activation, and bonding. These methods include a temporary bonding step during die placement on the carrier wafer. Although organic materials (typically spin-coated polymers) are often used as temporary adhesives, issues such as die shifts during die placement, thermal budget limitations, and difficulty in maintaining nanolevel total thickness variations due to the low elastic modulus of the polymer remain. In the case that plasma activated bonding is employed to permanently attach dies to the carrier wafer in conjunction with a standard bonding dielectric, backside grinding is required to later remove the carrier wafer. These steps can result in greater costs by increasing the processing time and leading to the loss of silicon wafers. It should also be noted that the removal of bulk silicon by grinding is not a sustainable practice.

On this basis, the present work proposes a new temporary bonding method based on low-temperature-deposited SiO_2 (LT-SiO_2).[1] The process flow during D2W bonding with LT-SiO_2 is summarized in Figure 1. The LT-SiO_2 used in this technique is a dielectric film deposited by plasma enhanced chemical vapor deposition (PE-CVD) at a relatively low temperature of 150 °C. Temporary bonding during die placement is accomplished by direct bonding with LT-SiO_2 as the bonding dielectric material (Figure 1a). This process reduces the risk of die shifts because the bonding interface is both thin and solid. Additionally, because SiO_2-based direct bonding is typically used in the fabrication of such devices, this technology is compatible with most front-end processes. As noted, D2W bonding tools have not yet matured, but a small degree of bonding failure can be accepted in the case of temporary bonding. Furthermore, LT-SiO_2 forms voids at the bonding interface during annealing that allow the carrier wafer to later be removed using a thermal release technique (Figure 1b).

The present work demonstrates a temporary bonding process involving LT-SiO_2 and also characterizes the LT-SiO_2, in particular the void formation mechanism associated with this material.

EXPERIMENTAL SECTION

A number of p-type 200 mm Si(100) wafers were employed for the W2W bonding trials. A 150 nm LT-SiO_2 layer was deposited on each wafer by PE-CVD at 150 °C, using liquid tetraethyl orthosilicate (TEOS) mixed with gaseous O_2 as precursors, at a deposition pressure of 50 Pa and radio frequency power of 1000 W. Following deposition, the dielectric surface was planarized using an ACuPLANE LK393C4 slurry. Following this, a 50 nm portion of the LT-SiO_2 layer was removed by chemical and mechanical polishing, leaving a 100 nm-thick layer. Each specimen was subsequently subjected to postdeposition annealing (PDA) under N_2 at different temperatures. The wafer pairs were then activated by exposure to a N_2 plasma for 60 s, after which the wafer surfaces were rinsed with deionized water. Wafer bonding was performed at room temperature in clean ambient air. The initial contact was carried out while applying a low pressure at the center of the wafer pairs, after which postbond annealing (PBA) was performed.

In contrast, D2W bonding experiments were performed using p-type 300 mm Si(100) wafers. Exactly the same process was applied to the 300 mm wafers as had been employed with the 200 mm wafers up to the PDA step. At this point, the backside of the top wafer was thinned to 200 μm. After grinding, the wafer was singulated into dies with a size of 10 × 10 mm.[11] Following this, the wafer surface was cleaned and activated using the same process as that applied during the W2W bonding. After wet cleaning, die bonding was performed using a particle-less, noncontact-type D2W bonder.

The composition of the LT-SiO_2 and thermal SiO_2 films was determined by Rutherford backscattering spectrometry (RBS) and elastic recoil detection analysis (ERDA, HRBS500, Kobelco) while a nanoindenter (Bruker TS 77) was used to ascertain the elastic modulus of each film, and roughness values were obtained using atomic force microscopy (AFM, SPA-400/SPI3800N). Scanning acoustic microscopy (SAM, Insight IS-350) was employed to examine voids at the interfaces of each bonded wafer pair and cross-sectional images were acquired using transmission electron microscopy (TEM, JEOL JEM-2100F). Bonding energy values were obtained by the double cantilever beam (DCB) method[12,13] performed under dry N_2. During these trials, a blade was automatically inserted by an actuator at a point 4 mm from the wafer edge. Thermal desorption spectroscopy (TDS, ESCO TDS1200II) was used to assess gases released from the films. TDS was able to detect compounds released from the samples during annealing, and trials were performed at a rate of 60 °C/min. Meanwhile, open spaces in the films were characterized by positron annihilation spectroscopy (PAS).[14−17] A positron implanted into a solid will undergo annihilation with an electron and emit γ rays. The energy distribution of these γ rays (511 keV) is broadened by the momentum component of the annihilating electron-positron pair. Freely diffusing positrons can potentially be trapped by open spaces because of Coulomb repulsion resulting from the ion cores. Because the momentum distribution of electrons at these defect sites will differ from that of electrons in the bulk, defects can be detected by assessing the Doppler broadening spectra of the annihilation radiation. In the present work, spectra were acquired based on the S parameter, defined as the proportion of annihilation events in the energy range between 510.22 and 511.78 keV. For TDS and PAS, the samples cut into 10 × 10 mm were used.

https://doi.org/10.1021/acsaelm.4c00114
ACS Appl. Electron. Mater. 2024, 6, 2449−2456

RESULTS AND DISCUSSION

Table 1 shows the compositions and elastic moduli for an LT-SiO_2 film and a thermal SiO_2 reference film. These compositions were determined using ERDA at depths of 30 to 50 nm from the surface. Although thermal SiO_2 contained only silicon and oxygen, LT-SiO_2 also included hydrogen. Because the latter film was deposited at a relatively low temperature, some residual unreacted TEOS likely remained in SiO_2, which may have been responsible for the hydrogen in the film. In addition, analysis by X-ray photoelectron spectroscopy indicated a high proportion of carbon in the LT-SiO_2 film, providing further evidence that the unreacted precursor remained in the film. The elastic modulus for each specimen was measured by nanoindentation, and the modulus for the LT-SiO_2 was found to be lower than that for the thermal SiO_2. This result can be attributed to the presence of impurities such as hydrogen and carbon in the former material and indicates that a dense Si−O network was not formed.

Table 1. Composition and Elastic Moduli for Oxide Films

	Si	O	H	elastic modulus [GPa]
LT-SiO_2	27.5	59.7	12.8	65.1
thermal SiO_2	34.0	66.0		74.6

Figure 2 presents AFM images of the LT-SiO_2 surfaces. The root-mean-square surface roughness values for this material after CMP, exposure to a 100 W N_2 plasma, and exposure to a 250 W N_2 plasma were 0.15, 0.21, and 0.85 nm, respectively. The CMP process evidently generated atomic-level flatness on the LT-SiO_2 surface (Figure 2a). Although this smooth surface was maintained after treatment with 100 W plasma (Figure 2b), some defects were formed after treatment with 250 W plasma (Figure 2c). It should be noted that 250 W is not an overly high power setting for plasma activation. The LT-SiO_2 was evidently more sensitive to ion bombardment than the thermal SiO_2 because of the minimal mesoscopic structure of the former, which caused surface etching and redeposition, leading to defect formation.

To investigate the effect of the plasma power and PDA temperature on the void formation, LT-SiO_2 pairs were bonded and annealed. Figure 3 provides SAM images of the bonding interfaces. In the present article, voids less than 1 mm are defined as microvoids. Immediately after bonding, microvoids were observed only in those pairs made with the higher plasma power of 250 W (Figure 3a). In the case of the bonding pair made using this high plasma power, the microvoids might have been caused by the rough surface (that is, by the presence of micro defects) that limited the contact area between the wafers. The other three pairs were bonded without voids, except for those caused by particles. In the present work, void formation was not undesirable because the goal was to use LT-SiO_2 as a temporary bonding material, and hence the voids served to initiate debonding. However, since wafers must be firmly bonded so that they can withstand subsequent processing until the carrier wafer is removed, void formation immediately after bonding should be avoided. Therefore, plasma activation at 100 W was selected as optimal. It should also be noted that large voids appeared in the wafer pair fabricated without PDA after PBA at 150 °C (Figure 3e). In addition, microvoids were also observed in the case of the pair subjected to PDA at 150 °C while only a few voids were observed on the pair made with PDA at 250 °C.

Bonding pairs fabricated with PDA at 150 and 250 °C were also subjected to PBA at 250 °C. As shown in Figure 4, both pairs exhibited very large voids, suggesting that voids were produced when the PBA temperature was equal to or above the deposition temperature of 150 °C or the PDA temperature.

Figure 5 shows a cross-sectional TEM image of a bonding interface of a sample after PBA at 250 °C. This image was taken from the black area in the SAM image presented in Figure 4. The white line that can be seen at the bonding interface is a gap, which cannot be detected by SAM due to the resolution limitation. This indicates that the wafer pair was partially bonded and that voids appeared at the SiO_2−SiO_2 bonding interface rather than at other interfaces.

To confirm that the wafer pairs could be debonded, the bonding energy of each specimen was ascertained using the DCB method.[12,13] These trials were performed under N_2 to eliminate any effect of water stress corrosion.[13,18] Figure 6 plots the bonding energies for thermal SiO_2 pairs and LT-SiO_2 pairs, with the latter subjected to PDA at 150 or 250 °C. Wafer debonding in conjunction with a low applied force is commonly performed in the mass production of thermal SiO_2 wafers without PBA, such as during alignment qualification of send-ahead wafers. Thus, the goal was to obtain debonding energies below the value for thermal SiO_2 without PBA (2.21 J/m^2). In the case of the thermal SiO_2 samples in the present work, the bonding energy increased as the PBA temperature was increased up to 250 °C, above which it plateaued. Hydrogen bonds between −OH groups and water molecules at the bonding interface play an important role in SiO_2−SiO_2 direct bonding.[19−23] However, these bonds transition to stronger siloxane bonds (Si−O−Si) during annealing. Therefore, it is likely that PBA at 250 °C was sufficient to promote the formation of such bonds in trials with thermal SiO_2. In contrast, the bonding energy for the LT-SiO_2 was lower and, although it also increased with increasing

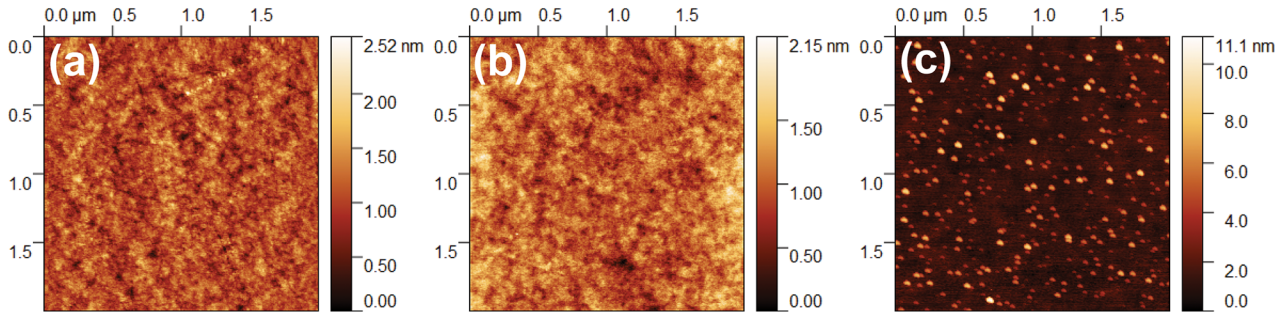


Figure 2. AFM images of LT-SiO_2 specimens (a) after CMP, (b) after exposure to 100 W N_2 plasma, and (c) after exposure to 250 W N_2 plasma.

https://doi.org/10.1021/acsaelm.4c00114
ACS Appl. Electron. Mater. 2024, 6, 2449−2456

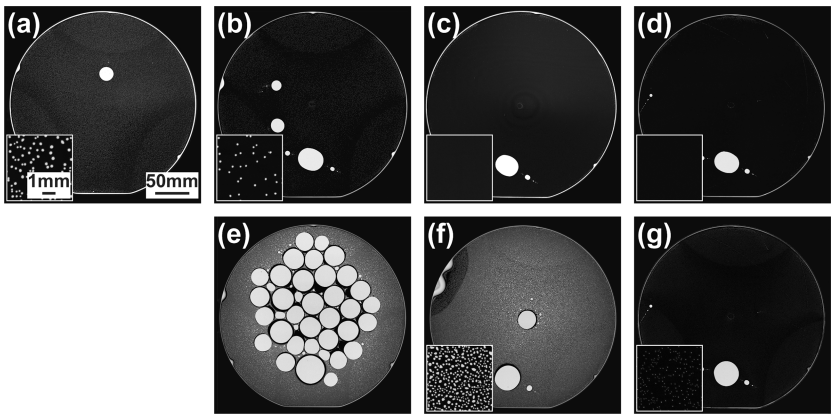


Figure 3. SAM images of LT-SiO_2 specimens (a–d) after bonding and (e,f) after PBA at 150 °C. These treatments were performed (a) with high plasma power, (b,e) without PDA, (c,f) with PDA at 150 °C, and (d,g) with PDA at 250 °C.

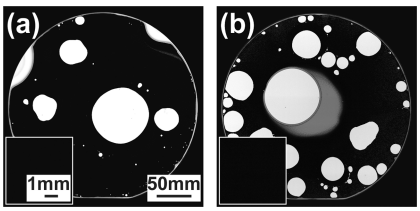


Figure 4. SAM images of LT-SiO_2 specimens after PBA at 250 °C and with PDA at (a) 150 or (b) 250 °C.

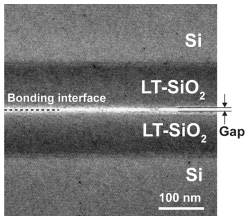


Figure 5. Cross-sectional TEM image of the LT-SiO_2 bonding interface following PDA at 250 °C after PBA at 250 °C.

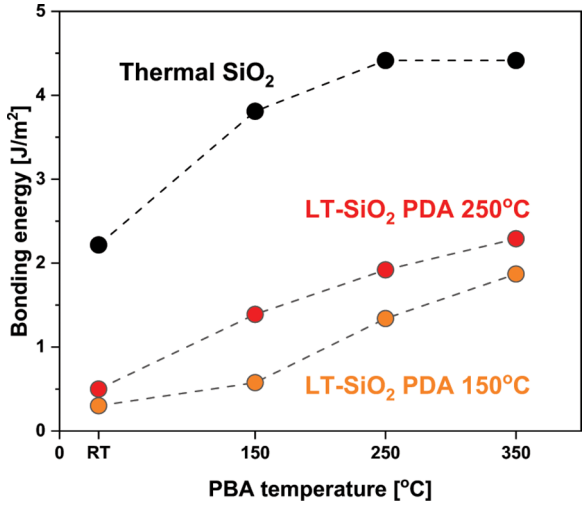


Figure 6. Bonding energy for thermal SiO_2 and LT-SiO_2 specimens as a function of PBA temperature.

temperature, it did not plateau above 250 °C. Because a gap was present at the bonding interface, as shown in Figure 5, a higher temperature was required to promote closing of this gap and the formation of siloxane bonds. In addition, the bonding energy for the LT-SiO_2 remained lower than, or almost the same as, that for the thermal SiO_2 above 350 °C. It is worth noting that there were no voids at the bonding interfaces of the thermal SiO_2 pairs whereas the LT-SiO_2 pairs exhibited numerous voids, which is normally considered to indicate bonding failure. However, in the present application, these voids served to initiate debonding and to adjust the bonding energy, suggesting new applications for LT-SiO_2.

It is apparent from the above data that LT-SiO_2 can be used as a temporary interface bonding material. Specifically, LT-SiO_2 bonding pairs seem to form voids at the bonding interface, which is a key requirement for subsequent debonding.

The void formation mechanism was investigated in detail using TDS and PAS. Figure 7 provides the TDS data acquired

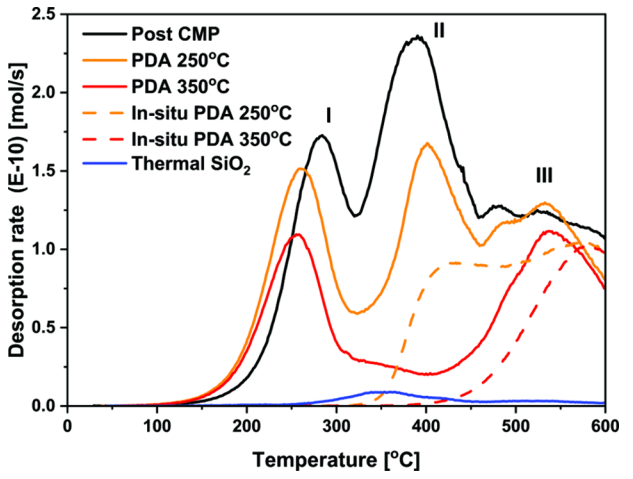


Figure 7. TDS spectra of LT-SiO_2 and thermal SiO_2 based on the monitoring of mass 18 (H_2O). I, II, and III in the figure represent peak positions.

from thermal SiO_2 and LT-SiO_2 specimens based on monitoring mass 18 (H_2O). Larger amounts of desorbed molecules were generated by LT-SiO_2 than by thermal SiO_2. More than 70% of all molecules released from the LT-SiO_2 without PDA up to 600 °C comprised H_2O. Moreover, the LT-SiO_2 spectrum contained three peaks (referred to as I, II, and III herein). Peak III was found to change only minimally with the PDA temperature, likely because the temperature at

https://doi.org/10.1021/acsaelm.4c00114
ACS Appl. Electron. Mater. 2024, 6, 2449–2456

which this peak appeared was above the PDA temperature. Peak II decreased significantly as the PDA temperature increased and was almost completely absent at 350 °C. Although peak I also decreased, it was still observed after PDA at 350 °C. LT-SiO_2 specimens were also subjected to *in situ* PDA in the chamber of the TDS instrument. In prior experiments, an interval of more than 1 day was normally applied between annealing and acquiring TDS data. However, in the case of the *in situ* PDA samples, TDS analysis was performed immediately after PDA without exposure to air. During these trials, peak I disappeared at both 250 and 350 °C and peak II was less intense. These results are similar to those reported by Hirashita et al.,[24] who established that SiO_2 films deposited by PE-CVD absorbed water molecules from the air. Thus, peak I was clearly associated with the desorption of absorbed water. Hirashita also reported that some absorbed water was attached to the −OH groups in the film via hydrogen bonding. As shown in Table 1, a large portion of the hydrogen derived from the TEOS precursor remained in the film. In the case of peak II, the change caused by the use of the *in situ* PDA process is attributed to the desorption of water undergoing hydrogen bonding. This is not the main origin of peak II because water was desorbed from the LT-SiO_2 during *in situ* PDA at 250 °C. The associated reaction is believed to have been

$$Si - OH + HO - Si \rightarrow Si - O - Si + H_2O$$

which occurred in the film between 250 and 350 °C. Conversely, peak III was not associated with absorbed water but was assigned to the reaction of residual TEOS in the film. Specifically, the TEOS is thought to have reacted to produce water above 400 °C[24,25] via the reaction

$$2Si - OC_2H_5 \rightarrow Si - O - Si + 2C_2H_4 + H_2O$$

Based on the TDS results, it is evident that void formation resulted from the desorption of water from the film. As reported by Sabbione et al.,[22] hydrogen, which is generated by silicon oxidation with water, can cause void formation in SiO_2/SiO_2 direct bonding, too. Although we observed hydrogen desorption from LT-SiO_2, the amount of desorption is less than water desorption. In addition, a higher temperature is required to desorb hydrogen. The LT-SiO_2 unavoidably absorbed water from the air even after PDA and this is an important factor that makes this material useful for temporary direct bonding.

Additional evaluations of nanoscale open spaces in the films were performed using PAS, which is a useful means of detecting atomic-scale open spaces.[14−17]

Figure 8 plots *S* as a function of the positron energy, *E*, for both thermal SiO_2 and LT-SiO_2 specimens. The mean positron implantation depth was estimated from the positron energy. The *S* values in the surface region (E = 0−1 keV) were low due to annihilation with electrons, which provided a broadened momentum distribution. In addition, the *S* values near the SiO_2/Si interface were affected by the interface states. This explains why the *S* values in the range E = 1−2 keV reflected the condition of the bulk SiO_2. The *S* values obtained for LT-SiO_2 were lower than those for thermal SiO_2. The *S* values for SiO_2 films deposited by CVD with TEOS are known to decrease when impurities such as unreacted TEOS and water remain in the film.[26] The *S* value for LT-SiO_2 was also found to increase as the PDA temperature was increased.

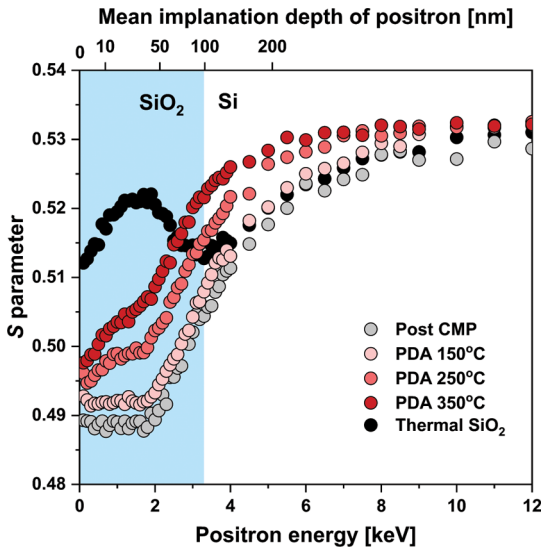


Figure 8. PAS data obtained for LT-SiO_2 and thermal SiO_2 samples: *S* as a function of positron energy.

Sometani et al.[27] reported that evaporation of impurities such as C_2H_4, CO, and H_2O from open spaces in TEOS-SiO_2 films increased the *S* value, which was attributed to the formation and annihilation of parapositronium in empty open spaces. A further increase in the *S* value was observed following annealing at 250−350 °C, and this temperature range agrees with that corresponding to the first desorption peak I shown in Figure 7.

Based on both the TDS and PAS results, a void formation mechanism was developed, as shown in Figure 9. In this

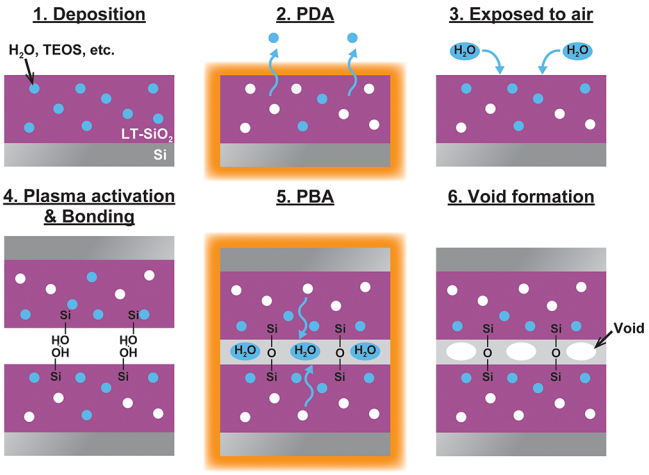


Figure 9. Proposed void formation mechanism.

mechanism, LT-SiO_2 contains significant amounts of water and unreacted TEOS immediately after being deposited. As these compounds evaporate during PDA, open spaces are formed in the film and the quantity that is lost via evaporation increases with increasing PDA temperature. However, when exposed to ambient air, LT-SiO_2 absorbs water molecules that fill the open spaces at the surface and subsurface. These molecules readily form hydrogen bonds with −OH groups in the film. Subsequently, the LT-SiO_2 surface is activated by the plasma to generate terminal −OH groups, after which bonding and PBA are performed. During PBA, water evaporates from the

https://doi.org/10.1021/acsaelm.4c00114
ACS Appl. Electron. Mater. 2024, 6, 2449−2456

film and diffuses to the bonding interface. Water is also generated as siloxane bonds are formed at the bonding interface. However, this water cannot desorb from the bonding interface because the open spaces in the film are already filled with reabsorbed water. As a result, voids are formed at the bonding interface.

Finally, D2W bonding trials were performed by using thermal SiO_2 and LT-SiO_2 with PDA at 250 °C. Figure 10

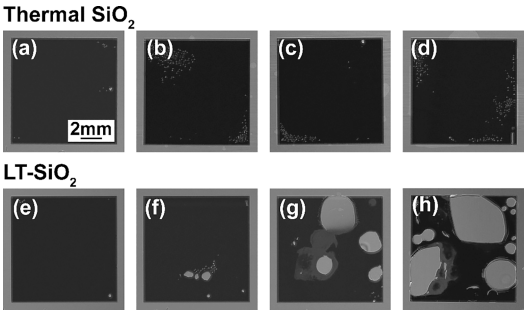


Figure 10. SAM images of (a–d) thermal SiO_2 and (e–h) LT-SiO_2 specimens with the latter subjected to PDA at 250 °C. Samples shown are (a,e) after bonding, (b,f) after PBA at 150 °C, (c,g) after PBA at 250 °C, and (d,h) after PBA at 350 °C.

provides SAM images of the interfaces generated by D2W bonding. These images demonstrate the presence of microvoids around the die edge for the thermal SiO_2 regardless of the application of PBA. Such microvoids can possibly be attributed to the Joule–Thomson effect.[28,29] In these experiments, the air between the top die and bottom wafer was compressed from the center to the edge during bond wave propagation, such that the pressure was higher at the bonding front, and compressed air expanded at the edge into the surrounding atmosphere. At this point, the air rapidly cooled, and condensed water droplets were formed, leading to the generation of microvoids. It is also possible that plasma activation created an edge effect due to the rectangular structure of the Si die.

It should be noted that the proportional void area was not increased after PBA in the case of thermal SiO_2 bonding, as demonstrated in Figure 11. The proportional void area was calculated from the SAM images shown in Figure 10. In

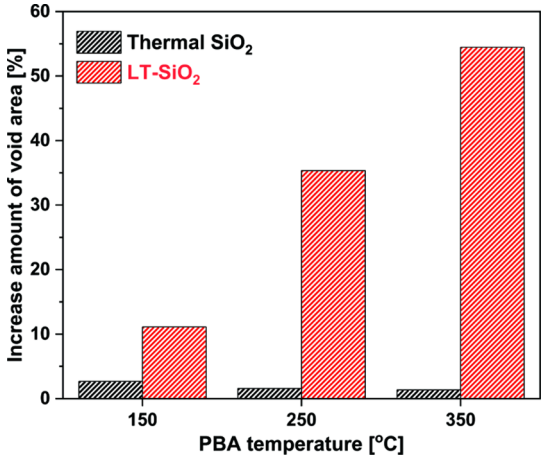


Figure 11. Increase in the void area in thermal and LT-SiO_2 specimens after PBA.

contrast, while the LT-SiO_2 specimen exhibited some voids immediately after bonding, the void proportion was greatly increased by annealing, especially when the PBA temperature equaled the PDA temperature of 250 °C. This result corresponds to the trends observed in the W2W bonding trials and indicates that the LT-SiO_2 bonding interface could undergo delamination during D2W bonding.

Hybrid bonding requires an annealing process to achieve the Cu–Cu connection and enhance the bonding strength. It is one of the advantages of temporary bonding with LT-SiO_2 that debonding can accomplish during annealing of hybrid bonding. In order to realize such an integration flow, the hybrid surface needs to be strongly bonded, as dies are debonded from the carrier. Recently, SiCN has been developed as a dielectric film for the hybrid surface because of its high bonding energy, void-free bonding, and diffusion barrier properties against Cu diffusion. SiCN are able to obtain sufficient bonding energy after PBA at 250 °C.[30,31] Therefore, it is considered that the void formation behavior shown in Figure 10, which forms voids at 250 °C, would be the preferred condition.

We employed nanoindentation to measure the bonding energy of D2W samples and estimate the debonding possibility for D2W samples with LT-SiO_2. As reported in our prior work,[32] nanoindentation method has a potential to measure the bond strength of D2W samples. Although the bonding strength measurement method needs to be improved, it is roughly able to estimate the bonding energy and debonding possibility. The value obtained by nanoindentation method was 1.92 J/m^2 for LT-SiO_2 samples after PBA at 250 °C. These measured values are comparable to those observed in W2W bonding (see Figure 6) and are lower than the debonding criterion for thermal SiO_2 without PBA (2.21 J/m^2). This data suggest that LT-SiO_2 allows for debonding at low forces in D2W configurations, as well.

CONCLUSIONS

This work demonstrated temporary direct bonding with LT-SiO_2 and investigated the characteristics of the resulting films with regard to D2W integration. Voids were formed at the bonding interface during W2W bonding trials in the case in which the PBA temperature exceeded the deposition or PDA temperature. Hence, the bonding energy was sufficiently low to make debonding possible. The TDS results established that the LT-SiO_2 absorbed water from the air but also desorbed a significant quantity of water even after annealing, leading to void formation. The PAS results also suggested that water evaporated from these films, such that open spaces were formed during annealing. Voids were also generated during D2W bonding after annealing as well as during W2W bonding. It is apparent that LT-SiO_2 can be used as a temporary direct bonding interface material in D2W integration.

AUTHOR INFORMATION

Corresponding Author

Fumihiro Inoue – *Yokohama National University, Yokohama 240-8501, Japan*; orcid.org/0000-0003-2292-846X; Email: inoue-fumihiro-ty@ynu.ac.jp

Authors

Koki Onishi – *Yokohama National University, Yokohama 240-8501, Japan*

Hayato Kitagawa – *Yokohama National University, Yokohama 240-8501, Japan*

https://doi.org/10.1021/acsaelm.4c00114
ACS Appl. Electron. Mater. 2024, 6, 2449–2456

Shunsuke Teranishi − *Disco corporation, Tokyo 143-8580, Japan*
Akira Uedono − *University of Tsukuba, Tsukuba, Ibaraki 305-8573, Japan*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsaelm.4c00114

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This work was supported by the "Intensive Support for Young Promising Researchers" project, JPNP20004, from the New Energy and Industrial Technology Development Organization (NEDO) and JST, PRESTO Grant Number JPMJPR22B3, Japan.

■ REFERENCES

(1) Inoue, F.; Teranishi, S.; Iwata, T.; Onishi, K.; Yamamoto, N.; Kawai, A.; Aoki, S.; Hare, T.; Uedono, A. Inorganic Temporary Direct Bonding for Collective Die to Wafer Hybrid Bonding. *2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)*, IEEE, 2023; Publisher: Orlando, FL, USA. DOI: DOI: 10.1109/ECTC51909.2023.00099.

(2) Lau, J. H. Recent Advances and Trends in Advanced Packaging. *IEEE Trans. Compon., Packag. Manuf. Technol.* **2022**, *12*, 228−252, DOI: 10.1109/TCPMT.2022.3144461.

(3) Chen, M. F.; Tsai, C. H.; Ku, T.; Chiou, W. C.; Yu, D. Low Temperature SoIC Bonding and Stacking Technology for 12/16-Hi High Bandwidth Memory (HBM). *IEEE Trans. Electron Devices* **2020**, *67*, 5343−5348.

(4) Elsherbini, A.; Jun, K.; Vreeland, R.; Brezinski, W.; Niazi, H. K.; Shi, Y.; Yu, Q.; Qian, Z.; Xu, J.; Liff, S.; Swan, J.; Yao, J.; Liu, P.; Pelto, C.; Rami, S.; Balankutty, A.; Fischer, P.; Turkot, B. Enabling Hybrid Bonding on Intel Process. *2021 IEEE International Electron devices Meeting (IEDM)*, IEEE, Publisher: San Francisco, CA, USA. DOI: DOI: 10.1109/IEDM19574.2021.9720586.

(5) Elsherbini, A.; Jun, K.; Liff, S.; Talukdar, T.; Bielefeld, J.; Li, W.; Vreeland, R.; Niazi, H.; Rawlings, H.; Ajayi, T.; Tsunoda, N.; Hoff, T.; Woods, C.; Pasdast, G.; Tiagaraj, S.; Kabir, E.; Shi, Y.; Brezinski, W.; Jordan, R.; Ng, J.; Brun, X.; Krisnatreya, B.; Liu, P.; Zhang, B.; Qian, Z.; Goel, M.; Swan, J.; Yin, G.; Pelto, C.; Torres, J.; Fischer, P.; Enabling Next Generation 3D Heterogeneous Integration Architectures on Intel Process. *2022 International Electron Devices Meeting (IEDM)*, IEEE, 2022. Publisher: san Francisco, CA, USA DOI: DOI: 10.1109/IEDM45625.2022.10019499.

(6) Phommahaxay, A.; Suhard, S.; Bex, P.; Iacovo, S.; Slabbekoorn, J.; Inoue, F.; Peng, L.; Kennes, K.; Sleeckx, E.; Beyer, G.; Beyne, E. Enabling Ultra-Thin Die to Wafer Hybrid Bonding for Future Heterogeneous Integrated Systems. *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*, IEEE, 2019. Publisher: Las Vegas, NV, USA. DOI: DOI: 10.1109/ECTC.2019.00097.

(7) Inoue, F.; Phommahaxay, A.; Podpod, A.; Suhard, S.; Hoshino, H.; Moeller, B.; Sleeckx, E.; Rebibis, K. J.; Miller, A.; Beyne, E.. Advanced Dicing Technologies for Combination of Wafer to Wafer and Collective Die to Wafer Direct Bonding. *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, USA, 2019. Publisher: IEEE. DOI: DOI: 10.1109/ECTC.2019.00073.

(8) Inoue, F.; Bertheau, J.; Suhard, S.; Phommahaxay, A.; Ohashi, T.; Kinoshita, T.; Kinoshita, Y.; Beyne, E. Protective layer for collective die to wafer hybrid bonding. *2019 International 3D Systems Integration Conference (3DIC)*, IEEE, 2019. Publisher: Sendai, Japan. DOI: DOI: 10.1109/3DIC48104.2019.9058870.

(9) Uhrmann, T.; Burggraf, J.; Eibelhuber, M. Heterogeneous Integration by Collective Die-To-Wafer Bonding. *2018 International Wafer Level Packaging Conference (IWLPC)*, IEEE, 2018; Publisher: San Jose, CA, USA. DOI: DOI: 10.23919/IWLPC.2018.8573296.

(10) Kagawa, Y.; Fujii, N.; Aoyagi, K.; Nishi, S.; Todaka, N.; Takeshita, S.; Taura, J.; Takahashi, H.; Nishimura, Y.; Tatani, K.; Kawamura, M.; Nakayama, H.; Nagano, T.; Ohno, K.; Iwamoto, H.; Kadomura, S.; Hirayama, T. Novel stacked CMOS image sensor with advanced Cu2Cu hybrid bonding. *2016 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2016; Publisher: San Francisco, CA, USA. DOI: DOI: 10.1109/IEDM.2016.7838375.

(11) Inoue, F.; Podpod, A.; Peng, L.; Phommahaxay, A.; Rebibis, K. J.; Uedono, A.; Beyne, E. Morphological characterization and mechanical behavior by dicing and thinning on direct bonded Si wafer. *Journal of Manufacturing Processes* **2020**, *58*, 811−818.

(12) Maszara, W. P.; Goetz, G.; Caviglia, A.; McKitterick, J. B. Bonding of silicon wafers for silicon-on-insulator. *J. Appl. Phys.* **1988**, *64*, 4943−4950.

(13) Fournel, F.; Continni, L.; Morales, C.; Da Fonseca, J.; Moriceau, H.; Rieutord, F.; Barthelemy, A.; Radu, I. Measurement of bonding energy in an anhydrous nitrogen atmosphere and its application to silicon direct bonding technology. *J. Appl. Phys.* **2012**, *111*, 104907.

(14) Leung, T. C.; Asoka-Kumar, P.; Nielsen, B.; Lynn, K. G. Study of SiO2-Si and metal-oxide-semiconductor structures using positrons. *J. Appl. Phys.* **1993**, *73*, 168−184.

(15) Krause-Rehberg, R.; Leipner, H. S. *Positron Annihilation in Semiconductors: Defect studies*. Springer Series in Solid-State Sciences. Springer Berlin: Heidelberg **1999**, *127*. DOI: 10.1007/978-3-662-03893-2

(16) Uedono, A.; Wei, L.; Tanigawa, S.; Suzuki, R.; Ohgaki, H.; Mikado, T.; Kawano, T.; Ohji, Y. Positronium formation in SiO_2 films grown on Si substrates studied by monoenergetic positron beams. *J. Appl. Phys.* **1994**, *75*, 3822−3828.

(17) Inoue, F.; Jourdain, A.; Peng, L.; Phommahaxay, A.; De Vos, J.; Rebibis, K. J.; Miller, A.; Sleeckx, E.; Beyne, E.; Uedono, A. Influence of Si wafer thinning processes on (sub)surface defects. *Appl. Surf. Sci.* **2017**, *404*, 82−87.

(18) Fuse, J.; Iwata, T.; Ebiko, S.; Inoue, F. Robust Measurement of Bonding Strength for Wafer-to-Wafer 3D Integration. *2023 International Conference on Electronics Packaging (ICEP)*. IEEE, 2023; Publisher: Kumamoto, Japan DOI: DOI: 10.23919/ICEP58572.2023.10129784.

(19) Plach, T.; Hingerl, K.; Tollabimazraehno, S.; Hesser, G.; Dragoi, V.; Wimplinger, M. Mechanisms for room temperature direct wafer bonding. *J. Appl. Phys.* **2013**, *113*, No. 094905.

(20) Stengl, R.; Tan, T.; Gösele, U. A Model for the Silicon Wafer Bonding Process. *Jpn. J. Appl. Phys.* **1989**, *28*, 1735−1741.

(21) Fournel, F.; Martin-Cocher, C.; Radisson, D.; Larrey, V.; Beche, E.; Morales, C.; Delean, P. A.; Rieutord, F.; Moriceau, H. Water Stress Corrosion in Bonded Structures. *ECS J. Solid State Sci. Technol.* **2015**, *4*, 124−130.

(22) Sabbione, C.; Di Cioccio, L.; Vandroux, L.; Nieto, J. P.; Rieutord, F. Low temperature direct bonding mechanisms of tetraethyl orthosilicate based silicon oxide films deposited by plasma enhanced chemical vapor deposition. *J. Appl. Phys.* **2012**, *112*, No. 063501.

(23) Nagano, F.; Inoue, F.; Phommahaxay, A.; Peng, L.; Chancerel, F.; Naser, H.; Beyer, G.; Uedono, A.; Beyne, E.; De Gendt, S.; Iacovo, S. Origin of Voids at the SiO2/SiO2 and SiCN/SiCN Bonding Interface Using Positron Annihilation Spectroscopy and Electron Spin Resonance. *ECS J. Solid State Sci. Technol.* **2023**, *12*, No. 033002.

(24) Hirashita, N.; Tokitoh, S.; Uchida, H. Thermal Desorption and Infrared Studies of Plasma-Enhanced Chemical Vapor Deposited SiO Films with Tetraethylorthosilicate. *Jpn. J. Appl. Phys.* **1993**, *32*, 1787−1793.

(25) Hirashita, N.; Kobayakawa, M.; Arimatsu, A.; Yokoyama, F.; Ajioka, T. Thermal Desorption Studies of Phosphorus-Doped Spin-on-Glass Films. *J. Electrochem. Soc.* **1992**, *139*, 794−799.

(26) Uedono, A.; Wei, L.; Tanigawa, S.; Suzuki, R.; Ohgaki, H.; Mikado, T.; Fujino, K. Characterization of silicon dioxide deposited

by low-temperature CVD using TEOS and ozone by monoenergetic positron beams. *Hyperfine Interact.* **1994**, *84*, 231−236.
(27) Sometani, M.; Hasunuma, R.; Ogino, M.; Kuribayashi, H.; Sugahara, Y.; Uedono, A.; Yamabe, K. Variation of Chemical Vapor Deposited SiO2 Density Due to Generation and Shrinkage of Open Space During Thermal Annealing. *Jpn. J. Appl. Phys.* **2012**, *51*, No. 021101.
(28) Castex, A.; Broekaart, M.; Rieutord, F.; Landry, K.; Lagahe-Blanchard, C. Mechanism of Edge Bonding Void Formation in Hydrophilic Direct Wafer Bonding. *ECS Solid State Lett.* **2013**, *2*, 47−50.
(29) Kim, Y.-S.; Nguyen, T. H.; Choa, S.-H. enhancement of the Bond Strength and Reduction of Wafer Edge Voids in Hybrid Bonding. *Micromachines.* **2022**, *13*, 537.
(30) Inoue, F.; Peng, L.; Iacovo, S.; Phommahaxay, A.; Verdonck, P.; Meersschaut, J.; Dara, P.; Sleeckx, E.; Miller, A.; Beyer, G.; Beyne, E. Influence of Composition of SiCN as Interfacial Layer on Plasma Activated Direct Bonding. *ECS J. Solid State Sci. Technol.* **2019**, *8*, 346−350, DOI: 10.1149/2.0241906jss.
(31) Iacovo, S.; Nagano, F.; Kumar, V. S.; Walsby, E.; Crook, K.; Buchanan, K.; Jourdain, A.; Vanstreels, K.; Phommahaxay, A.; Beyne, E. Direct Bonding Using Low Temperature SiCN Dielectrics. *2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)*, IEEE, 2022; Publisher: San Diego, CA, USA. DOI: DOI: 10.1109/ECTC51906.2022.00101.
(32) Fuse, J.; Iwata, T.; Yoshihara, Y.; Sano, M.; Inoue, F. Exploring bond strength for an advanced chiplet with hybrid bonding. *Chip Scale Rev.* **2024**, *28* (1), 39−45.

https://doi.org/10.1021/acsaelm.4c00114
ACS Appl. Electron. Mater. 2024, 6, 2449−2456