YOKOHAMA NATIONAL UNIVERSITY

DOCTOR'S THESIS

Research on qubit control and readout systems using superconductor and cryo-CMOS circuits
(超伝導回路と低温CMOSを用いた量子ビット制御・読出し回路の研究)

Author:
Hongxiang SHEN

Supervisor:
Prof. Nobuyuki YOSHIKAWA

A thesis submitted in fulfillment of the requirements for the degree of Doctor of Engineering

in the

Department of Mathematics, Physics, Electrical Engineering and Computer Science
Graduate school of engineering science

February 2, 2023

YOKOHAMA NATIONAL UNIVERSITY

Abstract

Department of Mathematics, Physics, Electrical Engineering and Computer Science

Doctor of Engineering

Research on qubit control and readout systems using superconductor and cryo-CMOS circuits (CMOS)

by Hongxiang SHEN

Nowadays, semiconductor technology has developed at a rapid pace because of high integration and stable performance. Moore's law even has been confirmed that the number of transistors in a dense integrated circuit (IC) doubles about every two years. Traditional computer become smaller and faster. However, with the reduction in size of transistors, Moore's law seems to be broken down soon. Besides, the problem of power consumption should be paid attention caused mainly by accumulation of data in the future. For low power consumption society, people start to focus on the superconducting circuits which owns the potential to relieve this problem. On the other hand, quantum computers appear to be capable, at least in principle, of solving certain problems far faster than any conceivable classical computer. This may reveals a new way to achieve quantum computer using superconductor circuits where both of them works within cryogenic temperature.

In this thesis we introduce the research process on quantum bit control and readout system using cryogenic circuits. We suggest a feed back schematic within the cryogenic temperature so that it save lots of cables. THe schematic contains the SFQ,AQFP,and Cryogenic CMOS circuits. Microwave generator as core part designed with SFQ is applied to control qubit. AQFP and cryogenic CMOS circuits is applied to control the generator. The measurement result confirm this circuits operation. Detail data of each circuits is in each chapters. Besides, we present suggestion to improve the characteristic of microwave generator. The SNR is higher than before and initial phase of microwave is controllable.It has been shown that quantum error correction (QEC) can be realized with cryogenic temperature, where it enables the possibility of performing fault-tolerant quantum computing in future.

Acknowledgements

This thesis resulted from my study at Yoshikawa laboratory, I'd like to express my appreciation to everyone who has supported me during my doctor studies in Japan. My advisor Professor Nobuyuki Yoshikawa is who I want to thank the most. Due to my original major is not superconducting circuits, he help me a lot with great patience during my student period. It is his patience and kindness that give me confidence and courage to overcome the bottleneck on the research. Moreover, he provide the chance to attend the many projects, such as qubit controlling and cold flux where I can learn lot knowledge. Besides, I'd like to thank Prof. Yuki Yamanashi. He give me lots suggestions on my research. I'd like to thank Prof. Naoki Takeuchi that I learned a researcher should have a rigorous attitude. I'd like to thank Dr. Hideo Suzuki that I obtained the help and suggestion both in my life and study. I wish to thank the prof.Yuxing He who teach me the designed method of RF circuits. I'd like to thank the prof.Christopher Ayala and prof.Olivia Chen who provide me the chance to learn more about design tools of synopsy.

Expect for the professors, I want to express my gratitude to the students in the Yoshikawa laboratory and yamanashi laboratory. The past member of QC group, such as Shiori Michibayashi and Yoshihiro Takagawa, they do lots of previous research about qubit controlling system. What's more, current group member Shu Sasaki and Nagamatsu Yoshiaki do lots of improvement which brings us closer to achieve quantum computer. Thanks to the unremitting efforts of my QC members, I can achieve my present achievement. I'd like to thank Yuki Hironaka,Taiki Yamae and Tomoyuki Tanaka that they help me in my research and daily life.

Finally, I would like to thank my parents for their full support for my study in Japan.

Contents

Chapter 1

Background

1.1 Introduction

Quantum computer owns the advantage of parallel calculation so that the it can solve the development potential problem in the future[1]. It will play an ever more important part in the behaviour of many emerging forms of artificial nano-technology, and in our understanding of the nano-machinery of biological molecules [2]. The engineering of the ultra small will continue to advance and change our world in coming decades, and as this happens we might use quantum computers to understand and engineer such technology at the atomic level[3]. The context for the development of quantum computers may be explained by a more familiar quantum technology: the laser[4]. Laser' advent reveals a phenomenon: light was always 'incoherent',which means that the many electro-magentic waves generated by source was emitted at completely random times with respect to each other. Quantum mechanical effects allow these waves to be generated in phase, and the light source engineered to exploit this concept was the laser [2]. Based on that, quantum computer,which is engineered to control coherent quantum mechanical waves for different applications, will be quite different with ordinary computer.

The example task for quantum computers which has provided the foremost motivation for their development is Shor's quantum algorithm for factoring large numbers[5]. For example, Shor's algorithm addresses the computational challenge of factoring by exploiting quantum interference to measure the periodicity of arithmetic objects[5][6]. This is one among several quantum algorithms that would allow modestly sized quantum computers to outperform the largest classical supercomputers in solving some specific problems important for data encryption[2]. On the other hand, another application should be paid attention which brings a high impact: Feynman's 1980s proposal of using quantum computers for the efficient simulation of quantum systems[7].

Such as quantum computing 'software' is under research nowadays. Quantum computing 'hardware' is worth to be discussed as well. There are many possible materials for lasers — crystals, organic dye molecules, semiconductors, free electrons — and likewise there are many materials under consideration for quantum computers[2]. Quantum bit is usually recognized to be constructed from the smallest form of matter and an isolated system or unit, such as in ion traps and optical lattices[8].. Besides,they may likewise be made far larger than routine electronic components, as in some superconducting systems[9]. Based on the study of superconductors, we will mainly discuss the control of superconducting qubit in this thesis.

1.2 Requirements For Quantum Computing

To quantum computing, the most strict requirement is the 'closed box'. That means a quantum computer's internal operation, while under the programmer's control, must otherwise be isolated from the environment[10]. There is a phenomenon called decoherence excited in quantum computer. It is caused by small amounts of information leakage form the 'closed box'. Then it can disturb the fragile quantum mechanical waves where the quantum computer depends on. Decoherence comes in several forms. At first state, the quantum mechanical waves, or the oscillations of the constituents in quantum computers will reveal the interference phenomena. Because the constituents process in experiments, the phase of the waves loss the 'cohere' after a certain time. Thus, in an ensemble experiment. trial-to-trial variations in oscillator frequency lead to an apparent damping of wave interference on a timescale called T_2 [11]. Then people discover that once a signal trial of a single quantum oscillator will keep the phase coherence longer than T_1. Finally, random process change the energy from oscillator,bring the system to thermal equilibrium on a timescale called T_2 [11]. Fundamentally$T_2 \leq 2 \times T_1$ and for most system, T_1 will be much larger than T_2. To prolong the T_2 becomes a research subject nowadays.

Besides the coherence time, there are some features which is people nowadays care about. The first thing is scalability. People expect the quantum computer operate in a Hilbert space. One single qubit can be simulated by LC classic oscillator. Because the quantum mechanic allows the entanglement, the logic space can potentially be described by a very large group[12]. This entanglement state can not be described by many signal classical oscillators or qubits[13]. Finally it is the large Hilbert space of a quantum computer that allows it operations unavailable to classical computers. For qubits, the size and energy of a quantum computer generally grows linearly with N and the resources to define or control the qubit are diverse[13]. They may include space on a microchip, classical microwave electronics, dedicated lasers, cryogenic refrigerators, and so on. For a scalable system ,these resources must be made scalable as well, which invokes complex engineering issues and the infrastructure available for large-scale technologies. That leads it difficult to make quantum system scalable.

The second thing is Universal logic. This is particularly important in quantum computers. To standard quantum computing,, it is sufficient to have available nearly 'analogue' single-qubit gates. For example, arbitrary flux direction for one flux qubit. Almost any 'digital' entangling two-qubit can be described logically, such as controlled-NOT gate. People use the logic gate to structure the quantum algorithm such as Quantum Neural Network (QNN)[14]. On the other hand, not all quantum computer is need quantum getes [15]. In adiabatic quantum computation, one defines the answer to a computational problem as the ground state of a complex network of interactions between qubits, and then one adiabatically evolves those qubits into that ground state by slowly turning on the interactions. In this case, evaluation of system is different with first case. Whether the system is complex enough and how long it takes to keep the temperature or turn off the temperature to search the best value of problem become main object detected[16]. Adiabatic quantum computers is near to gate-based computer in power consumption,but it is simpler for technologies.

The most important requirement for quantum computer is correctability[17]. It means that quantum computer must be possible to extract the entropy of the computer

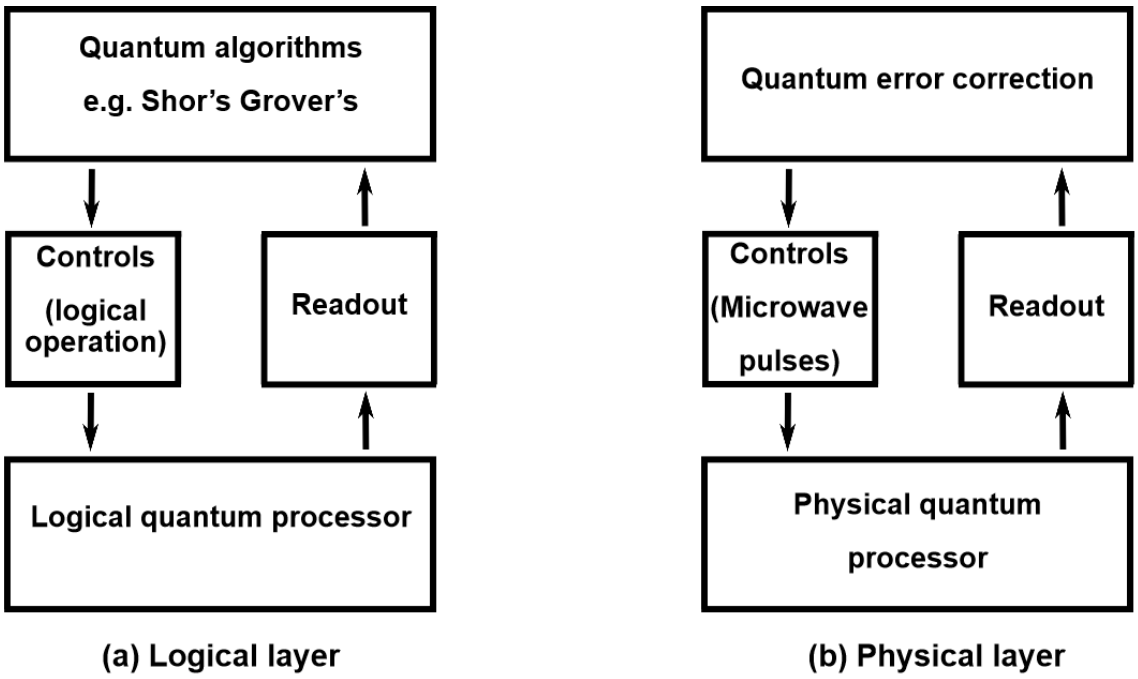


FIGURE 1.1: A systems view of a QEC processor

to maintain the computer's quantum state. Even if it is possible to achieve excellent isolation of quantum computer from environment, no one can execute quantum logic gates with perfect accuracy. Like an analog classical computer, the errors in the quantum gates form a continuum. Errors accumulate over the course of a computation in the gates and cause fault. A device that works effectively even when its elementary components are imperfect is said to be fault-tolerant[18]. Actually,similar problem arise in the theory of fault-tolerant classical computation. However, silicon-based circuitry is remarkably reliable, fault-tolerance is not essential to the operation of modern digital computers[19]. In 1952, Von Neumann suggested improving the reliability of a circuit with noisy gates by executing each gate many times, and using majority voting[20]. Although Von Neumann's theory has a shortcoming that he assumed perfect transmission of bits through the "wires" connecting the gates the assumption was proved by G´acs in 1983[21]. It gives us a enlightenment that fault-tolerant processing of quantum information may be achieved. The main challenge is to construct a universal set of quantum gates that can act on the encoded data blocks without introducing an excessive number of errors[18]. Some schemes for universal computation are outlined[22].

1.3 QEC For Fault-Tolerant Computer

As mentioned that the main challenge to achieve fault-tolerant process is to avoid large errors in basic quantum gates. Except the incomplete isolation environment, the increasing of qubit numbers will arise the noise. Some significant steps has been achieved such as Alexei Kitaev[23]. The reason is that the information is stored in the qubit as a quantum computer. Qubit is required to interact with each other strongly,

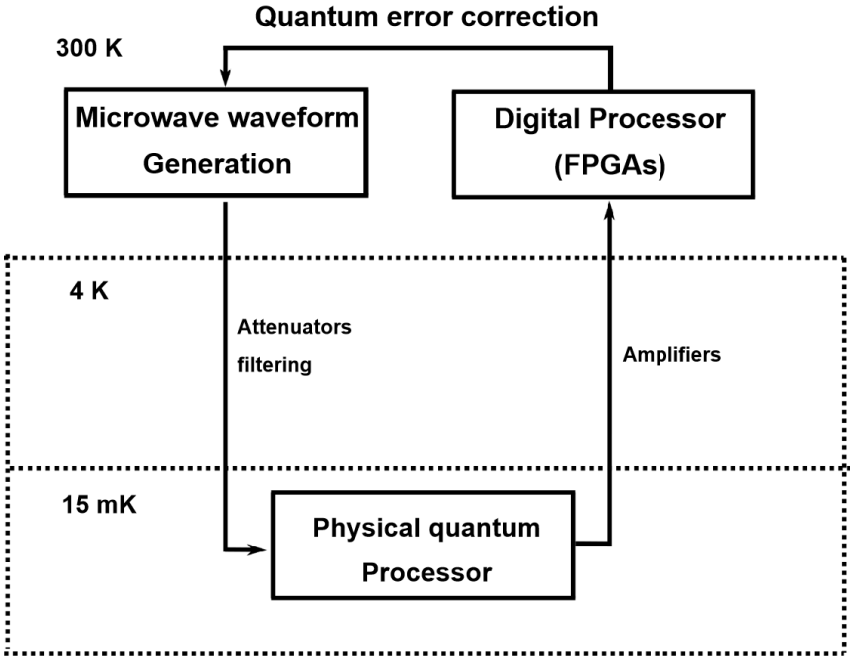


FIGURE 1.2: The physical qubit processor

external inputs for control, and outputs for detection. It is hard to balance the enough control and coupling because of preserving quantum coherence. This conflict represents a fundamental impediment to reducing the physical qubit error rate low enough to perform long/difficult/large-scale/practical quantum computations with them directly[24].

Fortunately, it has been shown that with quantum error correction (QEC) it is possible to perform fault-tolerant quantum computing[25]. The essential idea for QEC is to store information using a larger physical space that are isolation to noise. The particular architecture for implementing a fault-tolerant operating scheme has bearing on the requirements necessary for the underlying physical qubits[26]. A full fault-tolerant quantum computing system is presented within a layered structure as shown in Fig. 1.1. QEC can achieved by two primary layers, a physical qubit layer and a logical qubit layer[27]. Physical layer contains the qubit which constitute the physical quantum processor. The processor uses the measurement outcomes of the physical qubits to realize a QEC code. This classical processor keeps track of the physical errors, and implements the appropriate feedback on the controls of the physical qubits[27]. On the other hand, logical layer functions through control of the physical layer. Logical qubits are encoded within the physical qubits, and logical controls and readouts are governed through a processor that determines how to implement difficult quantum algorithms, e.g. Shor's, Grover's, and quantum simulation[28][29]. Many types of qubits has been explored applied in experimental systems, such as superconducting qubits, trapped-ion and so on. For purpose of quantum computing, it is important to normalize decoherence time to the quantum gate lengths. That means the longer decoherence time for qubit, the more operations can be finished. As now, the superconducting qubits holds the potential of hundreds μs decoherence time and each quantum gate takes several 10 ns, the number of operations per coherence time becomes a very promising number (almost 1000 operations).

Fig. 1.2 presents the physical qubit schematic. Microwave pulses are generated

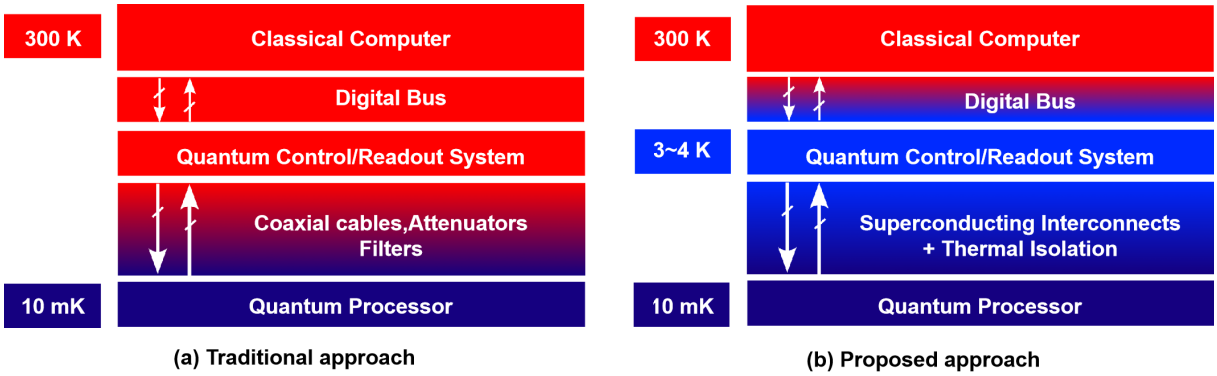


FIGURE 1.3: Approach to interfacing the quantum process and classical computer

at room temperature using synthesizers, arbitrary waveform generators, and mixers. These pulses are filtered and attenuated to input to the qubit. High-fidelity readout of the qubit state requires quantum-limited and other cryogenic amplification to overcome thermal noise for digitization and weighted measurement[30]. Physical control and readout function is orchestrated by digital process (FPGAs) to perform the error correction protocol.

1.4 Researc Purpose

As presented in Fig. 1.2, the microwave generator is placed at room temperature. However, it is possible that these feedback loop can be implemented within low temperature although it is start from Cryogenic-CMOS technology[31][32]. Fig. 1.3 presents the traditional and proposed approach to achieve the loop which connect the quantum process and classical computer. Currently,quantum process system can be realized by using signal from room-temperature. Here, quantum process is connected to classical computer using meters of lossy coaxial cables which is shown as (a). In the future,the quantum process will be scaled to million qubit level. The control and readout system must be integrated and implemented in "near" to quantum process to avoid too many cables. For this purpose, several research propose that to scale the quantum control and readout system within cryogenic temperature which is shown as (b). If the control and readout system is implemented within cryogenic temperature, the circuit based on Josephson Junction (JJ) becomes feasible.

Our work seems to be significant which is currently underway toward implementation of the schematic presented in Fig. 1.4. The room-temperature continues signal is applied to cryogenic microwave generator which is designed by single flux quantum circuits (SFQ)[33]. And cryogenic microwave is generated and drive qubit which is under 15 mK. The driven qubit will cause the Ribi oscillation so that qubit state can be readout by Josephson parametric oscillator (JPO) by compare the phase shift[34]. AQFP cell can readout the oscillation phase and to improve the sensitivity, we design the integrator. On the other hand, the there are two sides to control the microwave generator. We design the microwave duration controller using AQFP circuits and microwave envelope controller using Cyro-CMOS technology. Thus, we can structure the

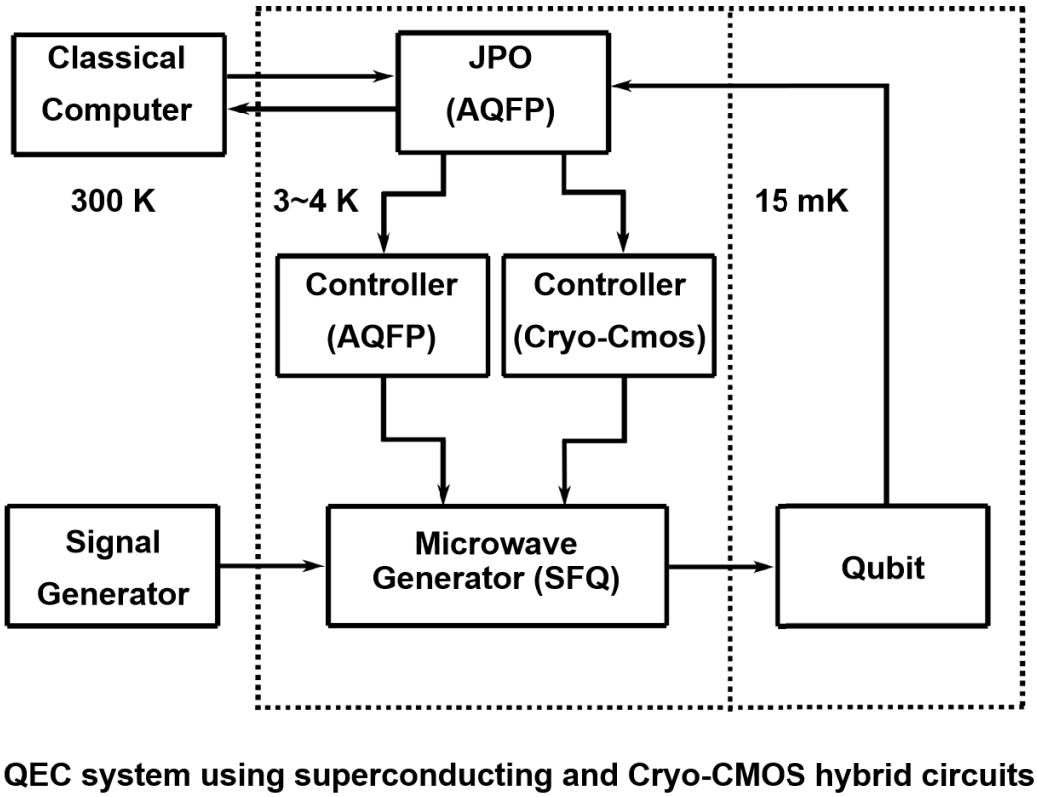


FIGURE 1.4: QEC system using superconducting and Cryo-CMOS hybrid circuits

simple feedback loop to achieve qubit controlling. Besides, we suggest some improvement to this system and fabricate the chip using HSTP process.

This thesis is divided into 5 parts and content of each chapter is list as follows:

The first chapter describes the background about the quantum process

The second chapter describes the microwave generator design within 4.2 K and measurement result.

The third chapter describes the microwave duration controller and integrator applied in JPO using AQFP including measurement result.

The forth chapter describes the microwave envelope controller using Cryo-CMOS technology including measurement result.

The fifth chapter describes the improvement of this system.

The sixth chapter describes summary of this thesis.

Chapter 2

Microwave Generator Using SFQ

In this chapter, we describe the microwave generator structure with fundamental elements. We will start from characteristics of superconducting circuits based cell which including JJ and SFQ family cell. Then we will introduce the operation principle of microwave generator. Finally we will state the measurement environment of microwave generator and show the measurement result

2.1 Josephson Junction

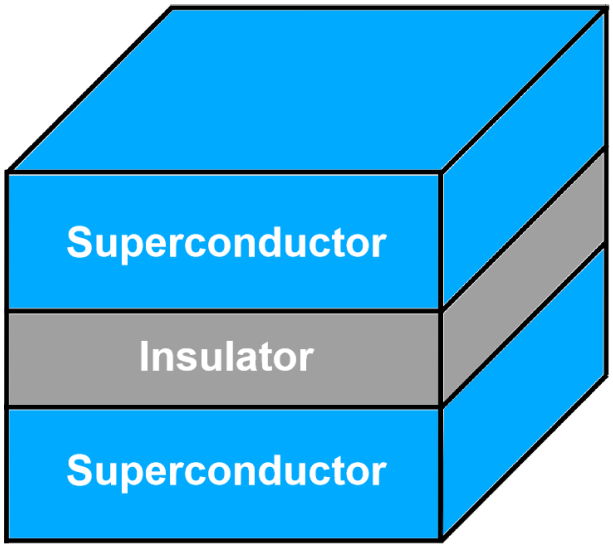


FIGURE 2.1: Model of Josephson junction

The most important cell of superconducting circuits is Josephson junction (JJ) and model is presented as Fig. 2.1. JJ consists of two superconductors where there is a insulator between them. This structure is know as SIS and if the insulator is thin enough, electrodes in superconductor can tunnel though the barrier. This phenomenon is called quantum tunneling effect and if allows current crossing the insulator barrier even if there is no external biased voltage. The crossed current of JJ is called Josephson current and the value can be given as follows:

$$I = I_c sin(\theta_1 - \theta_2) = I_c sin(\phi) \tag{2.1}$$

Here θ_1 and θ_2 is the phase factor of two superconductor, ϕ is the phase difference between θ_1 and θ_2. I_c is the critical current of JJ. Phase changes with time will arise the voltage linearly in superconductor with following formula:

$$\frac{\partial \Delta\phi}{\partial t} = \frac{2e}{\hbar}V \tag{2.2}$$

Here V is the voltage caused by switching JJ, e is elementary charge and $\hbar$ is the reduced Planck constant. From the previous formula, one thing is revealed that alternative current cross though the junction, which is also called AC Josephson effect.

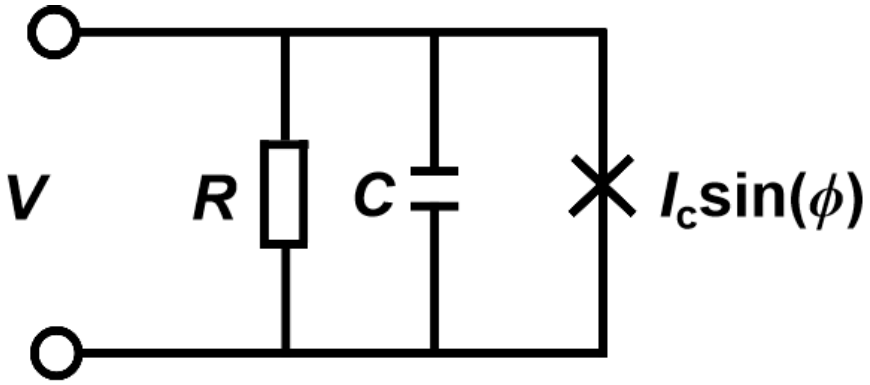


FIGURE 2.2: Equivalent circuit of a Josephson junction

To achieve the small-signal analysis of JJ, we present the equivalent circuit model of JJ which is shown as Fig. 2.2. Here the resistance R and capacitance C is shunted to JJ and ϕ is phase difference of two ports of JJ. We analyze this model based on Thevenin's equivalent theorem and the formula can be presented as follows:

$$I = I_c sin\phi + \frac{V}{R} + C\frac{dV}{dt} \tag{2.3}$$

Then we can combine the two formula (2.4) and (2.5), the formula can be presented as follows:

$$I = \frac{\hbar C}{2e}\frac{d^2\phi}{dt^2} + \frac{\hbar}{2eR}\frac{d\phi}{dt} + I_c sin\phi \tag{2.4}$$

The new time variable τ is available as follows:

$$\tau = \omega_c = \frac{2eI_cR}{\hbar}t \tag{2.5}$$

In conclusion of these formula, we can get as follows:

$$\frac{I}{I_c} = \beta_c\frac{d^2\phi}{d\tau^2} + \frac{d\phi}{d\tau} + sin\phi \tag{2.6}$$

The parameter β_c is McCumber parameter defined as

$$\beta_c = \omega_c CR = \left(\frac{2e}{\hbar}\right)\cdot(I_cR)\cdot(CR) = \frac{2eI_cR^2C}{\hbar} \tag{2.7}$$

Besides the AC Josephson effect, there is also a DC Josephson effect. It is much easy to understand that if the current I cross though the junction is smaller than I_c , there will be no voltage because circuits is under superconducting state. On the other hand, if the current I is larger than I_c, the superconducting state will be destroyed and there is voltage arisen on JJ.

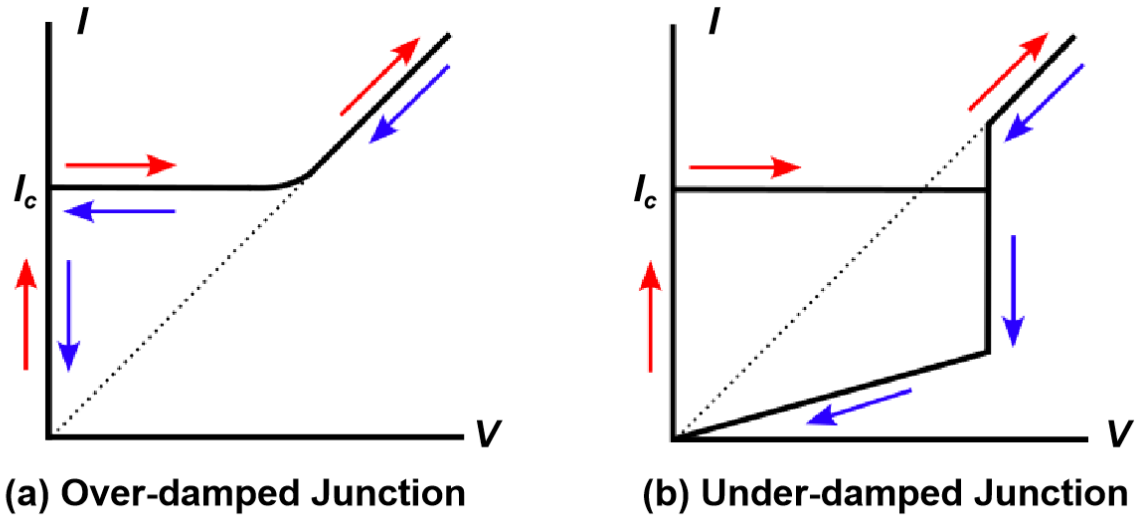


FIGURE 2.3: $I - V$ characteristic of Josephson junction

β_c is mainly decided by shunt resistor R because capacitance C is almost decided by process. According to formula (2.6), the $I - V$ characteristic of JJ can be calculated if we set the β_c to a constant. However, the the $I - V$ characteristic of JJ will be changed in different case of β_c. If β_c is about constant 1, the voltage of JJ will decay to 0 very fast once the large current I cross though junction. On the other hand, if β_c is about constant 0, the voltage of JJ will holds on a time until the current decay significantly. For these two different cases, we can present the figure which is shown in Fig. 2.3. Over-damped Junction is the situation that β_c is smaller than 1 and Under-damped Junction is the situation that β_c is bigger than 1.

2.2 Signle Flux Quantum Logic Circuits

Based on magnetic flux quantization theory, magnetic flux exists in a superconducting contour loop can be quantized and the minimum magnetic flux unit is shown as Φ_0. Based on this character, we can store information in the loop with form of magnetic flux. Once a magnetic flux escapee from the loop, there is a pulse signal generated by JJ because junction switches. So that we can transport the flux message by switching the JJ. The imagination photo of SFQ circuits is presented as Fig.2.4. The value of Φ_0 is presented by following formula:

$$\Phi_0 = \frac{h}{2e} = 2.07 \times 10^{-15}\text{Wb} \tag{2.8}$$

$$\Phi = \int V\,dt = \int \frac{\Phi_0}{2\pi}\,d\phi = \Phi_0 \tag{2.9}$$

The escape flux value is Phi_0 when JJ switches. Besides, we can get the flux on JJ according to the Faraday's laws which is presented in (2.9). The phase of JJ changes 2π once the JJ switches. JJ phase changing cause the voltage of JJ changing, which means the pulse is generated on junction. Thus, we can set one Φ_0 as an information carrier to achieve the SQF logic, where the generated pulse signal represents the logic "1".

Fig.2.4 presents the physical layer of SFQ circuits and the superconducting circuits loop are connected serially. Adjoining loop use the same junction (grey) and junction connect to junction with inductance (blue). Extra bias current is required to each loop because it can provide an initial current to JJ so that it can switches more easily. When there is a flux (red) escape from the loop, the current in the loop rotate clockwise and the value can be calculated as follows:

$$I \cong \frac{\Phi_0}{L} \tag{2.10}$$

Here the L is the inductance of superconducting loop. If the $I > I_c$, JJ switches and delivers the quantum flux to the next loop. On the other hand, if the $I < I_c$, JJ will not switch and the flux will store in the loop. Generally, this case is caused because the inductance L of loop is very big so that the current changes very small according to (2.10). Both two situations can be used to design the SFQ circuits. The time of JJ switches is very fast, which is about several picoseconds. The amplitude of SFQ voltage can arrive about hundreds of microvolts according the formula (2.9).

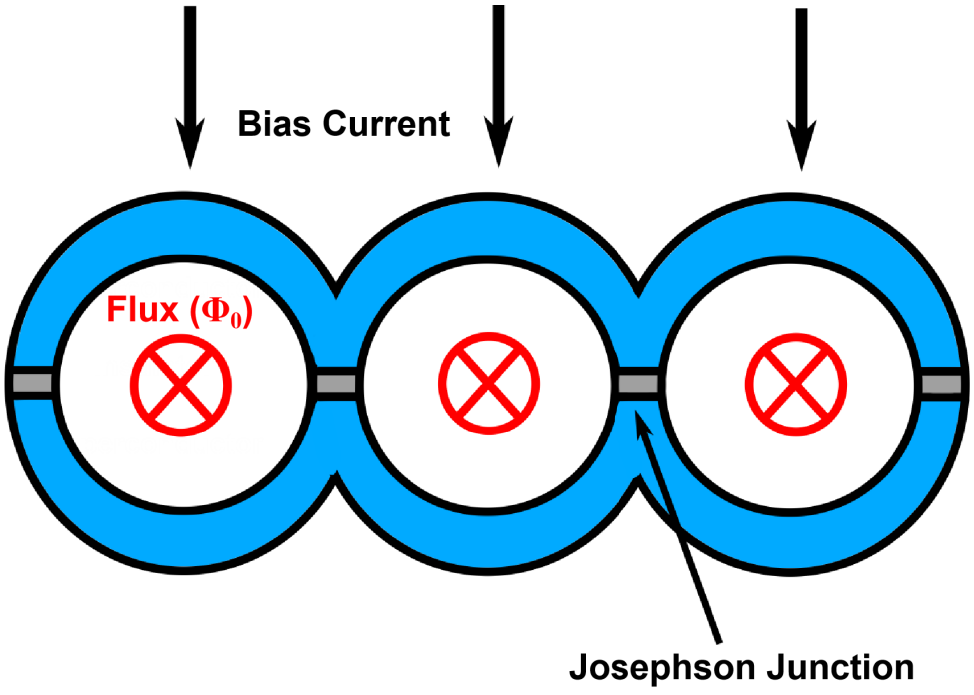


FIGURE 2.4: Imagination of SFQ circuits operation

2.3 SFQ Logic Gate

As mentioned, we can use the characteristic of flux transmission in superconducting loop to achieve logic message. Nowadays we have build up the SFQ cell library based on the transmission and storage functions of SFQ circuits. The section we will introduce some basic SFQ logic cell which is the elements to form the digital applications.

2.3.1 Josephson Transmission Line (JTL)

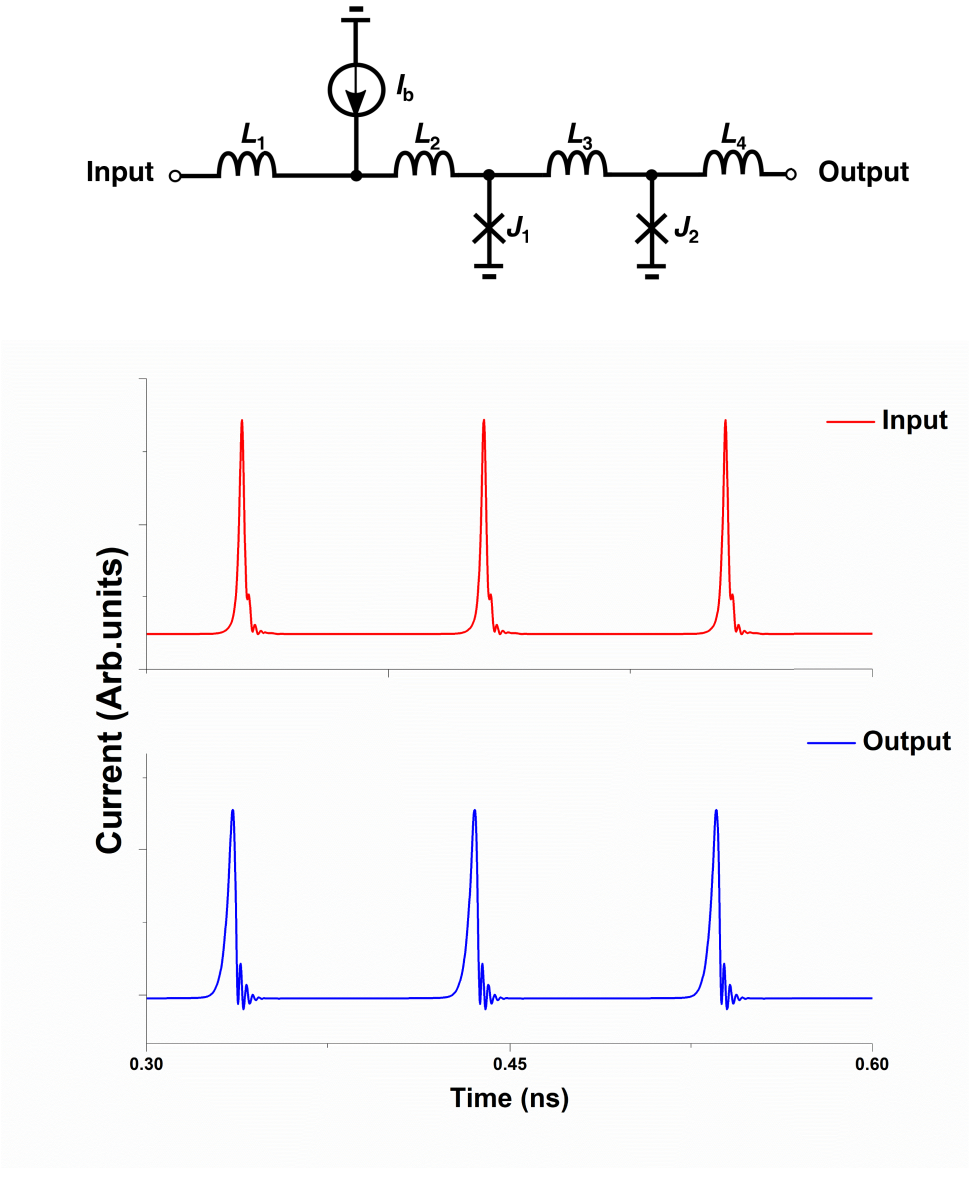


FIGURE 2.5: Josephson transmission line

The structure of Josephson Transmission Line (JTL) is presented as Fig.2.5. It contains just two JJs and several inductance. When there is one pulse input though the inductance L_1, the loop which contains the L_2 and J_1 will store this flux message and

the current which across though the J_1 becomes big. When current is beyond the critical current of J_1, J_1 switches and phase of J_1 turns 2Π. Then there will be a flux store in loop which contains the J_1,L_3,J_2 because of J_1 switches. The changing phase of J_1 also cause the changing phase of J_2 if inductance L_3 is not too big to store a flux. With this processing the JJ will switch one by one and propagate SFQ pulse. The simulation result is presented at bottom of Fig. 2.5. As the result, JTL can propagate an SFQ pulse from port “input” to "output".

2.3.2 Confluence Buffer (CB)

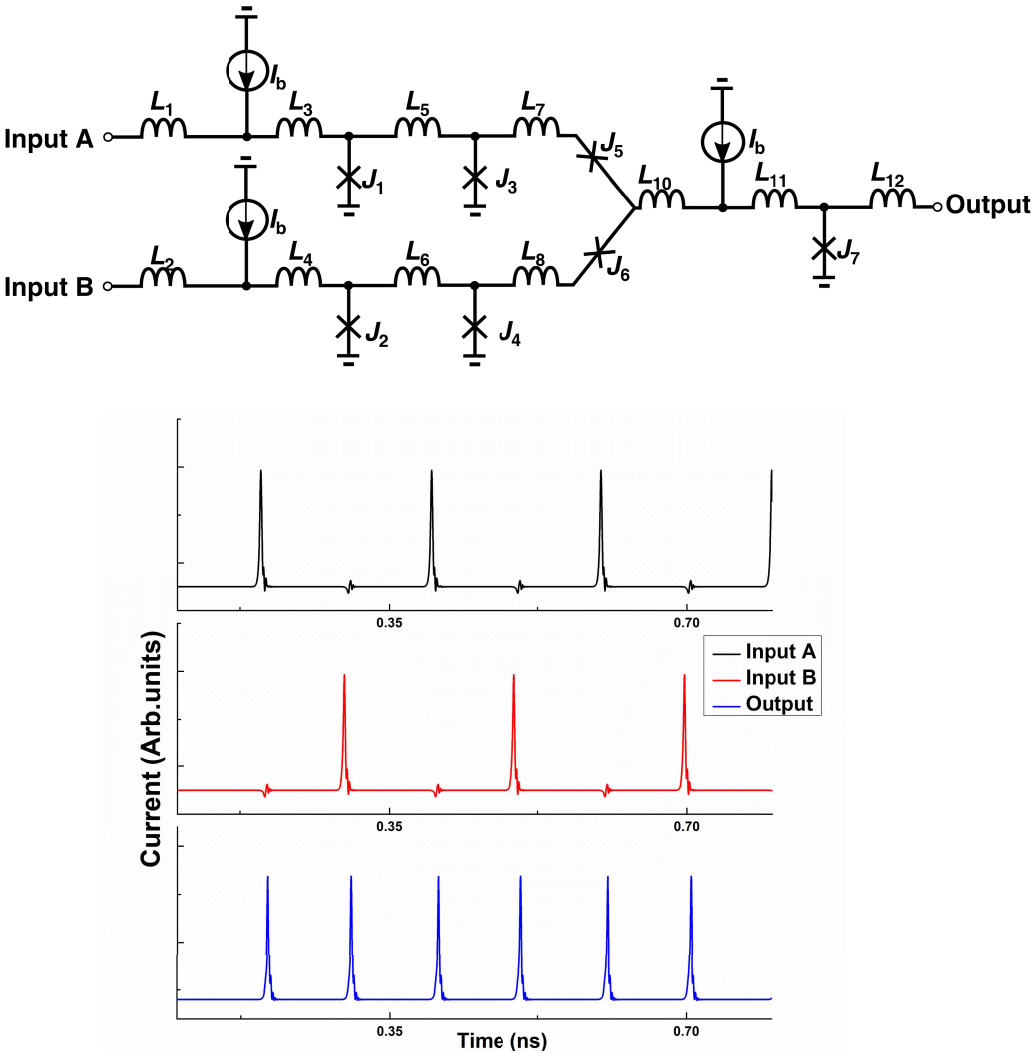


FIGURE 2.6: Confluence buffer

Here we present a structure of confluence buffer (CB) to discuss the situation that two pulses input to one superconducting loop. The structure is presented in top of Fig.2.6. The input A and input B propagate a pulse though inductance L_1 and L_2. The loop which contains the J_1, J_3 and J_7 propagates the pulse signal when there is a pulse exist at input A. With the same operation, the loop which contains the J_2, J_4 and J_7 propagates the pulse signal when there is a pulse exist at input B. Thus, the SFQ CB

cell can reproduce an SFQ pulse once there is an incoming SFQ pulse input from any input. To prevent the wrong direction of transmission such like pulse pass though the J_7 and pass though the J_8, the J_5 and J_6 are inserted between the L_7 and L_8. Because the J_6 switches earlier than J_4, it disrupts the loop and prevents the SFQ pulse from propagating in the wrong direction. In addition, J_5 perform the same function with J_6 to when an pulse signal is propagated from input B. If the pulses are input at the same tame, the error will occurs because CB just can generate one pulse at one time. The simulation is presented at bottom of Fig.2.6. Output hold the almost same time interval between both sides of SFQ pulse input.

2.3.3 T-Flip Flop (TFF)

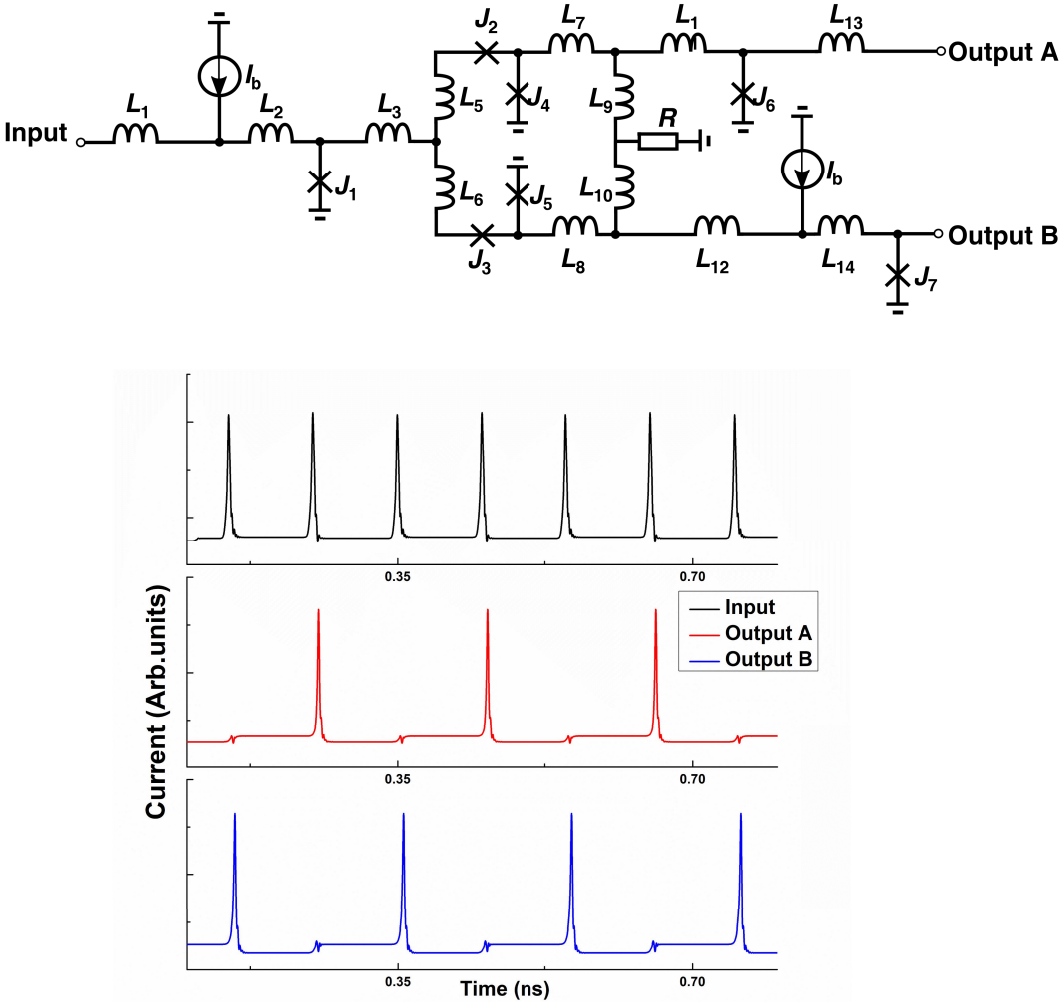


FIGURE 2.7: T-flip flop

Here we introduce the T-flip flop (TFF) whose function is inverse with CB. The structure is presented at top of Fig.2.7. Pulse is propagated though inductance L_1 from input port. There are two loops share one JJ (J_1), which are J_1,J_2,J_4 and J_1,J_3,J_5. When first pulse is propagated, the J_2 will switch earlier than J_3 because the critical current of J_2 is smaller than J_3. So that the phase of J_2 turns 2Π. Thus, the phase of JJ (J_5) will

switch and propagate one pulse signal though the inductance L_14 to output B. On the other hand, the loop which contains the J_5, L_8, L_10, L_9, L_7, J_4 store a flux because the phase of J_5 turns 2Π. This case the J_4 does not switch so that there is a large current store in the inductance L_9 and L_10. When second pulse is propagated though L_1, the J_4 becomes much easier than J_5. Thus, the J_4 switches and J_5 keep the state in this case. The pulse signal generated by J_4 is propagated though inductance L_13 to output A. After that, the loop of J_5, L_8, L_10, L_9, L_7, J_4 recover initial state and current in L_9 and L_10 reduce. Therefore, the function of TFF can be realized that input pulse is divided in two parts in sequence. The simulation of TFF cell is presented at bottom of Fig.2.7. The function can be confirm according to the simulation result when the frequency of pulse signal arrives about 10GHz.

2.3.4 Non Destructive Read Out (NDRO)

Here we preset the structure of Non Destructive Read Out (NDRO) at top of Fig.2.8. Generally, the continues pulses sequence is propagated though the inductance L_3 from CLK port. Because the critical current of J_6 is smaller than J_10, J_6 will switch earlier than J_10 when J_3 switches. Thus the flux in loop which contains the J_10,J_6,J_3 will not be propagated into next loop. Oh tne other hand, if there is a pulse which is propagated though the L_1 from input port, junction J_7 will switch. In this case the loop which contains J_3,J_6,L_4,L_9,J_5 stores a flux. The current in inductance L_5 will increase and current inductance L_4 will decrease. That means the junction J_3 become hard to switch than J_2. Thus, next pulse which is propagated from input again will not impact the state because J_4 switches earlier than J_7. So the current in the inductance L_12 will increase and junction J_10 become easy to switch. So after that if pulse is propagated from CLK port, junction J_10 switches earlier than J_6 and pulse signal can be propagated to output port.

On the other hand, if there is a pulse which is propagated thought L_2 from reset port. The junction J_8 will switch and it leads to L_9 switch. Then the stored flux escapes from loop which contains the L_10,J_7,J_8. The current in inductance L_10 decreases and junction J_10 becomes hard to switch. So after that if pulse is propagated from CLK port, junction J_6 switches earlier than J_10 and pulse signal can be prevented to propagate to output port.

The simulation result is presented at bottom of fig.2.8. According to result, we can get the pulse sequence (black) only can be propagated during the period between the input and output. NDRO can be used as a switch to control the pulse sequence or registration which can store the information.

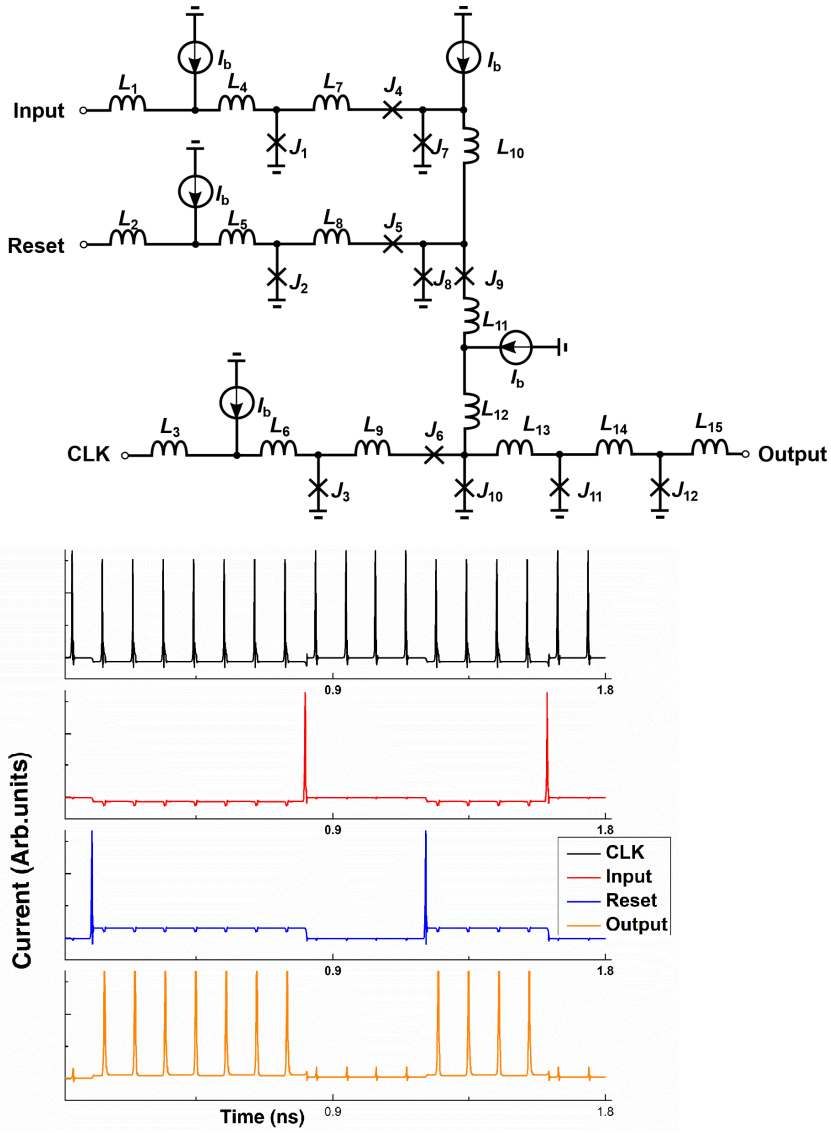


FIGURE 2.8: Non Destructive Read Out

2.3.5 DC/SFQ Converter (DSC)

Here we present a SFQ cell which can convert the non-SFQ signal to SFQ pulse. The structure is presented as top of Fig.2.9. The signal come from input port, generally it is current signal. Once the current is big enough, the junction J_2 will switch and generate a pulse signal to output prot. When the voltage drops, the current flows in the DC direction, so the SFQ is released by switching the escape junction J1 so that no output can be obtained. The simulation result is given at bottom of Fig.2.9. When input signal arrives at top, one pulse will be generated and propagated from output port. This cell realize the function that converter current signal to SFQ pulse signal.

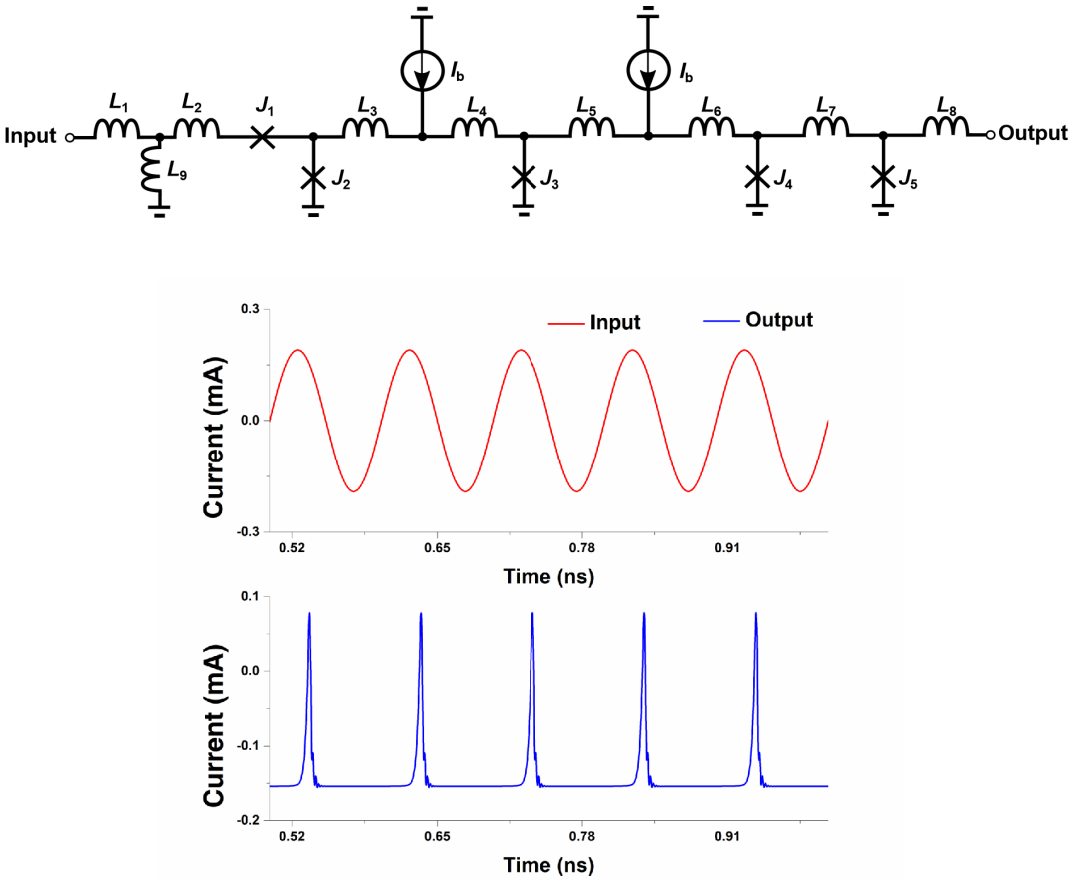


FIGURE 2.9: DC/SFQ Converter

2.4 Qubit Control

In this section, we will mainly introduce the Microwave pulse generator. Firstly, we will discuss the generated microwave's to state of qubit. Thus, we will decide the parameter of microwave which we should pay attention. Then we will present the structure of microwave pulse generator and explain the operation function. Last we will present the measurement environment and result.

2.4.1 Flux-Tunable Transmon Qubit

Here we present the schematic of a flux-tunable transmon qubit which contains the h XY-drive, Z-drive, and readout ports at Fig.2.11. The target qubit consists of capacitor L_Q in in parallel with a Josephson junction loop. The JJ can be thought of as a non-linear inductance which formulla is given as follows:

$$L_J = \frac{L_c}{\cos(2\pi\Phi_E/(\Phi_0)} \tag{2.11}$$

$$L_c = \frac{\Phi_0}{2\pi I_c} \tag{2.12}$$

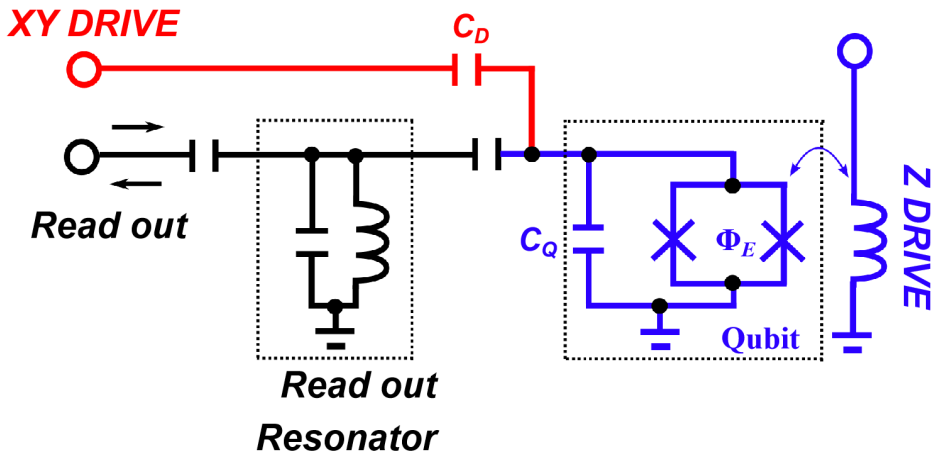


FIGURE 2.10: Flux-Tunable Transmon Qubit

Here,the Φ_E is the external flux across the loop, Φ_0 is the flux quanta. L_c is decided by critical current of JJ which is influenced by proportional junction area. Based on that, the flux-tunable transmon qubit can be thought of as a frequency-tunable non-linear LC resonator. The transom qubit will behave quantum mechanically when the temperature is cooled to suppres the thermal population of the non-linear resonator. Generally, the effective photon temperature is approximately 250 mK for the typical qubit frequency of 5GHz. Thus, if the devices are close to several mK, the thermal excitations are sufficiently suppressed.

To control the qubit state, the XY-drive (red) should be used which is presented in Fig.2.11. The excitation frequencies of XY influence the spectral width of microwave excitation pulses. Generally, the the anharmonicity of qubit should be as large as possible in order to achieve more operations before the decoherence time.

The Z-drive (blue) port provides control of the qubit frequency by using an external current. This play an important role in system which can realize several operations: control of the qubit frequency, multi-qubit connection and qubit initialization. In this research we assume that the Z-plane can set the qubit frequency of 5Ghz and do the initialization.

Actually, the qubit state can be readout by capacitively coupling an ancillary linear resonator (black).The coupling between the readout resonator and the qubit will cause a dispersive frequency shift of the readout resonator up or down in frequency. The readout resonator will interrogate at the average of two frequencies which behave the qubit state $|0\rangle$ and $|1\rangle$. Then dispersive frequency shift will produce a state-dependent phase shift on the interrogation signal, which can be detected and used to determine the state of the qubit.

2.4.2 Control of Transmon Qubit

Here we will discuss quantitatively about the control effect by XY-plane microwave signal. Assuming that voltage driven signal can be given as follows:

$$V_D(t) = a(t)\sin(\omega_D t) + (\pi - \phi_D) \tag{2.13}$$

Then the Hamiltonian of the driven circuit in the rotating qubit by the drive signal can be written as follows:

$$H_D \approx g\frac{a(t)}{2}(\cos(\phi_D\sigma_X) + \sin(\phi_D\sigma_Y) - \frac{h\pi\Delta_\omega}{4}\sigma_Z \tag{2.14}$$

Here the g shows the drive coupling strength which is decided mainly by capacitance C_D and C_Q. Δ_ω is the offset frequency which is the difference of driven frequency and qubit resonant frequency. σ_X,σ_Y,σ_Z is the Pauli spin matrices and formula is given as follows:

$$\sigma_X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \sigma_Y = \begin{bmatrix} 0 & -i \\ i & 0 \end{bmatrix}, \sigma_Z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} \tag{2.15}$$

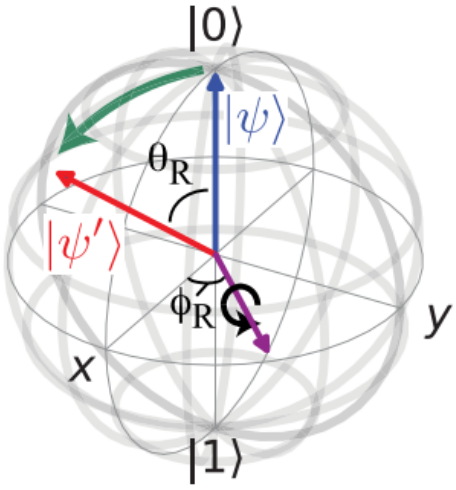


FIGURE 2.11: Rotation of Qubit

Pauli spin matrices are always used in QEC system to perform the quantum error and quantum correction. It is also the basic quantum gate to achieve the quantum algorithm. Here we give the qubit rotation Imagine figure which refers to the thesis[9]. Once the microwave drive the qubit, the qubit which is shown at Bloch space will start to rotate. The Hamiltonian inflect the rotation and the formula is consisted by Pauli spin matrices. Here, Pauli-X gate perform the state reversal according to the formula (2.15). So turn back to the formula (2.14) we can get that the initial phase of microwave decides the qubit rotation direction. For example, if the initial phase is 0, the H_D is almost decided by σ_X. On the other hand, if the initial phase is π, the H_D is decided by $-\sigma_X$. It is desirable to only discuss rotations about the XY plane of the Bloch sphere. In Fig.2.11 ,/$theta_R$ reveals the rotation angle. According to the thesis[9], /$theta_R$ can be presented as follows:

$$\theta_R = 2\pi\frac{g}{h}\int_{t_0}^{t} a(t')\,dt' \tag{2.16}$$

The formula shows that the amplitude of microwave and the time which microwave keeps deciedes the state of qubit. The qubit is almost driven by XY-plane. On the other hand, the Z-plane can be calibrated by software[9] so that the qubit should nominally

be driven on resonance ($\Delta_\omega = 0$). Although the amplitude of microwave and time duration do the combined action on qubit, the decoherence time of qubit limits the time duration. So the shorter time duration, the more power of microwave is required. Besides, during the time of microwave duration, the amplitude of microwave will influence the quantum fidelity[35]. Gate fidelity is a measure of how close the effect of an applied gate is to that of the desired unitary and can be limited by a number of factors, including control errors, noise, and decoherence[36]. Generally, the envelop of microwave, which behave the amplitude changes via time, is set to Gaussian function because it can arrive high fidelity though experiment[37]. In conclusion, we need the microwave signal which the duration and envelope can be controlled within cryogenic temperature.

2.4.3 Filter Response of Pulse Signal

There is only pulse signal exist in SFQ circuits. To generate the microwave signal, we suggest a method that using pulse signal though the filter and we can get the microwave response. Here we analyze the different types of filter's impact on generated microwave. Here, we assume the the SFQ Pulse is ideal and response function of each types of filter can be given as follows:

$$F(\omega) = \begin{cases} K & -\omega_0 < \omega < \omega_0 \\ 0, & others \end{cases} \tag{2.17}$$

$$F(\omega) = \begin{cases} K & others \\ 0, & -\omega_0 < \omega < \omega_0 \end{cases} \tag{2.18}$$

$$F(\omega) = \begin{cases} K & -\omega_1 < \omega < \omega_2 \\ 0, & others \end{cases} \tag{2.19}$$

$$F(\omega) = \begin{cases} K & others \\ 0, & -\omega_1 < \omega < \omega_2 \end{cases} \tag{2.20}$$

Here, the K behaves the loss constant. Function (2.17) perform the frequency response of Low-pass filter. Function (2.18) perform the frequency response of High-pass filter. The ω_0 is the cut frequency of filter. Function (2.19) perform the frequency response of band-pass filter. Function (2.20) perform the frequency response of Band-stop filter. The ω_1 and ω_2 is the bandwidth of filter. SFQ pulse can be thought as an ideal impulse impact function ($\delta(t)$). Thus one pulse input to filter, the response function can be presented on frequency domain as follows:

$$H(\omega) = 1 \times F(\omega) \tag{2.21}$$

Then we do the Fourier transform to the (2.21), the function on time domain can be given as follows:

$$h(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} H(\omega) \times e^{-j\omega t}\, d\omega \tag{2.22}$$

High-pass filter and Band-pass filter is not to be applied because the $\delta(t)$ is high frequency signal. We can not obtain the microwave signal With the high frequency

component. Thus, we just discuss the Low-pass filter and Band-pass filter's impact on generated microwave.

To the low-pass filter, the function (2.22) can be presented as follows:

$$h(t) = \frac{K \times \omega_0}{\pi} sa(\omega_0 \times (t - t_0)) \tag{2.23}$$

Here $sa(x) = \sin(x)/x$.

The cut frequency influence the output amplitude. However, the larger cut-frequency will arise external frequency component. Generally, we set it to from 5.5 to 7.5 GHz because of 5GHz qubit oscillation frequency. We can plot the function (2.23) and compare it to simulation result as Fig.2.12.

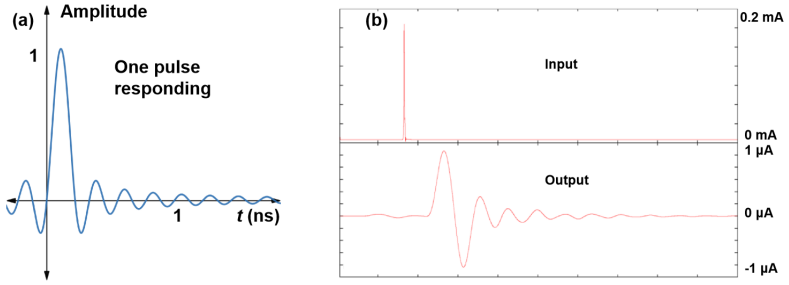


FIGURE 2.12: Mathematical model and simulation of One pulse response

In this case, the cut frequency of filter is 6.5 GHz and the loss constant is Independence with frequency. We use the JTL cell to generate a standard pulse and input to filter. The waveform of (a) and (b) is similar. According to the mathematical model, the approximate microwave can be generated and simulation result can be used to confirm. However, it is hard to control the amplitude of microwave only by one pulse. Lots of pulses are required to input to filter. We present the schematic as Fig.2.13.

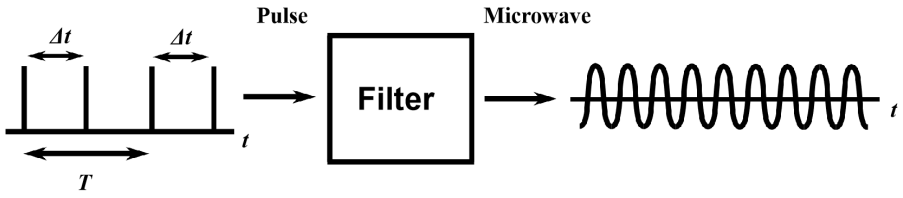


FIGURE 2.13: Mathematical model and simulation of one pulse response for low-pass filter

To control the amplitude of microwave, we suggest the schematic that pulse-pair to input to filter. The duration between each pulse-pair is main frequency component. It is obvious that time $\delta(t)$ is smaller than T. Thus, the frequency component of δt will be removed by filter at output and keep the main frequency component of T. What's more, if we can control the interval of pulse-pair, the amplitude of microwave can be changed because pulse density changes. To confirm this theory, we present the Fig.2.14

In this case, we set the same filter to calculate the mathematical model and we input one pulse-pair. The interval of pulse-pair (δt) decreases from the 0.1 nanosecond which

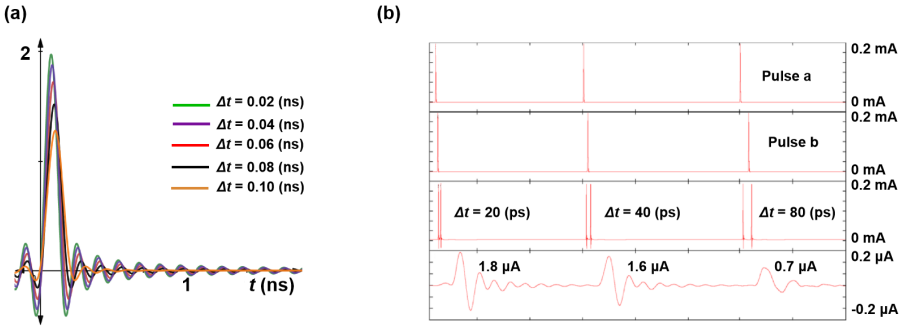


FIGURE 2.14: Mathematical model and simulation of pulse-pair response

is the maximum value because we assume (T) as 0.2 nanosecond. Confluence pulse will increase the pulse density near-double so that the amplitude of microwave becomes double than before. Than interval of pulse-pair become longer which leads the pulse density smaller so that the amplitude of microwave also decreases like Fig.2.14 (a) shows. We also do the simulation to compare the waveform which is presented in Fig.2.14 (b). In this simulation we input two pulse (A and B) and use the Confluence Buffer to combine them. We have three examples to show the larger interval of pair-pulse, the smaller amplitude of microwave. Fig.2.15 present the relationship of amplitude of microwave and interval of pair-pulse in normalization. As the Fig.2.15 shows, the simulation variation trend is almost the same with theoretical value. The simulation value is smaller than theoretical value because the SFQ pulse is not ideal pulse signal. The circuits reflection is bigger than ideal model.

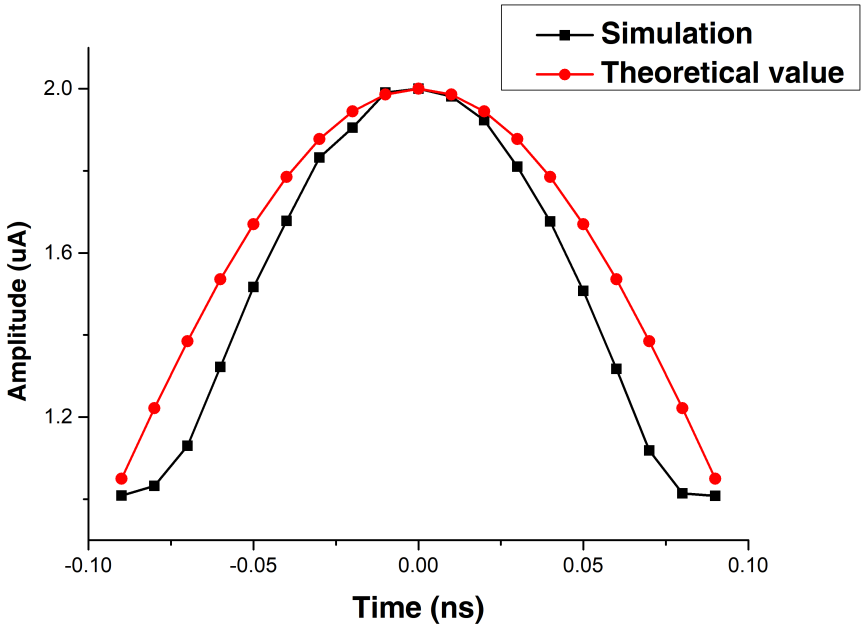


FIGURE 2.15: Mathematical model and simulation of pulse-pair response

On the other hand, if we change the low-pass filter to band-pass filter, the microwave will be generated by applying the pair-pulse. The formula is given as follows:

$$h(t) = \frac{K \times \omega_0}{\pi}(sa(\omega_2 \times (t - t_0)) - sa(\omega_1 \times (t - t_0))) \tag{2.24}$$

Here, we assume ω_2 is bigger than ω_1. The waveform is present in Fig.2.16. It is different with low-pass filter response as there is minus component in the function (2.20). Using one pulse into filter, the near-microwave signal can be generated directly. However, the amplitude will decrease largely using one pulse response. Besides, the tail can be found behind the main microwave. The tail lead to the transmission latency. We do the same simulation of band-pass filter response using one pulse. The result is similar with mathematical model. The reason why simulation microwave is asymmetric is that the initial state of circuits is start from 0. Also the circuits component such as impedance mismatch will arouse the asymmetric microwave.The amplitude is decrease to about 0.1 μ A which is match to calculated results.

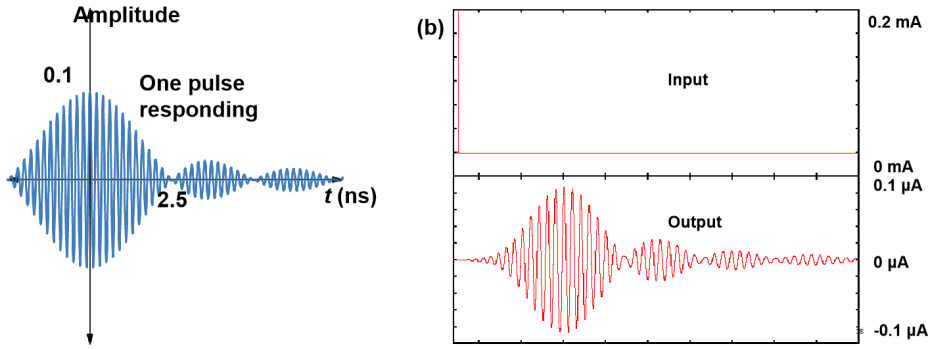


FIGURE 2.16: Mathematical model and simulation of one pulse response for band-pass filter

So if we input the several pair-pulses into filter, the pair-pulses will be superposed and form the microwave signal both of low-pass filter and band-pass filter. The mathematical model is presented in Fig.2.17. The response of low-pass filter (a) has less latency because single pulse owns less ripple which can be found in Fig.2.12. However, the microwave generated by low-pass filter owns the DC component because the main value of pair-pulse is positive. Lots of pair-pulse sequence will lead the average value of microwave to positive which can be though the DC component. On the other hand, band-pass filter will avoid this phenomenon because single pulse response is longitudinal symmetry. However, the latency exist obviously which can be explained using formula (2.24). And the tail can be found which may influence the subsequent microwave form if the sequence is close to each other.

Both filter can generate the microwave to drive qubit by input the pair pulse. However, there is no consensus that which filter is better to generate microwave. Generally, People using the filter to decrease the thermal impact of quantum process. Most people use driven microwave generated by signal generator which is under room-temperature. Thus, it is meaningful that apply two types of filter driven and compare effect in measurement. The amplitude of microwave can be controlled by changing

the interval of pair pulse. Thus, the superconducting circuits to control the interval becomes very important.

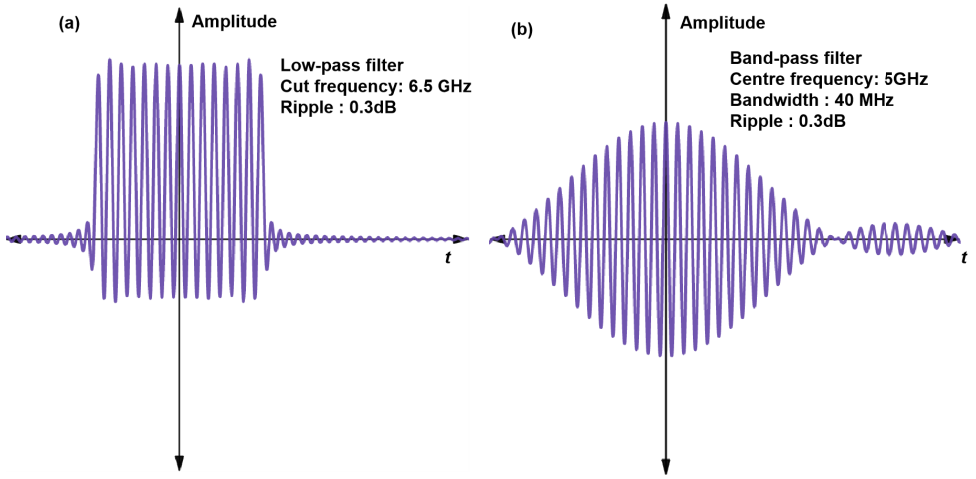


FIGURE 2.17: Mathematical model and simulation of one pulse response for band-pass filter

2.4.4 Delay Generator (DG)

Here, we will introduce the designed delay generator using SFQ circuits. As mentioned, the amplitude of microwave can be controlled by changing the interval of pair pulse. So if there are two same pulses sequences, and we just make some controllable delay between these two pulses sequences and combine them using confluence buffer. The two pulse can be seen as a pair pulse and the delay is Δt which is the same with Fig.2.13. Original interval of pulse sequence can be seen as T which is the same with Fig.2.13. In our design, the time T is 0.2 nanosecond and Δt is less than 0.1 nanosecond. The large range of Δt is required.

The Structure is presented in Fig.2.18. Here, we input two sequences pulse sequences from inductance L_{in1} and L_{in2}. The initial interval of pulses of In_1 and In_2 is set to δt_0 which is equals 0.1 nanosecond. The first pulses (blue) is propagated though inductance into loop which contains J_1,J_2,L_2,L_4.The J_1 and J_2 switches will switches at same time because the current cross the L_2 and L_4 is the same. It is the same situation of J_3 and J_4. However, once there is control current input as Fig.2.18 shows, the initial state of JJs will change. With the current input, there is external flux input to the loops so that the current in the inductance L_2 decrease because the opposite coupling between the L_2 and L_1. On the other hand, the current in the inductance L_4 increase. Thus, J_1 will become switch harder than before. According to that the, the pulse which is generated by J_1 will propagate slower than before and the pulse which is generated by J_2 will propagate faster than before. Here, we choose the slower pulse to output and sink the faster pulse. The next pulse (red) input to the loop which does the same effect. The different thing is that we choose the faster pulse to output and sink the faster pulse. Thus, the original pulse interval (Δt_0) becomes Δt by reconstruction of pulse sequences.

We need two loops to construct the DG. Although one loop can realize the pulse delay function, the latency is very small so that we have to connect several DGs to achieve enough range latency of pair-pulses. Small latency will also cause the error of confluence buffer which will be connect to DG easily. Therefore, that means the number of input ports and output ports should be same. Thus, we need two loop which own one input pulse and two output pulses. So that there will be two external outputs which should be sink.

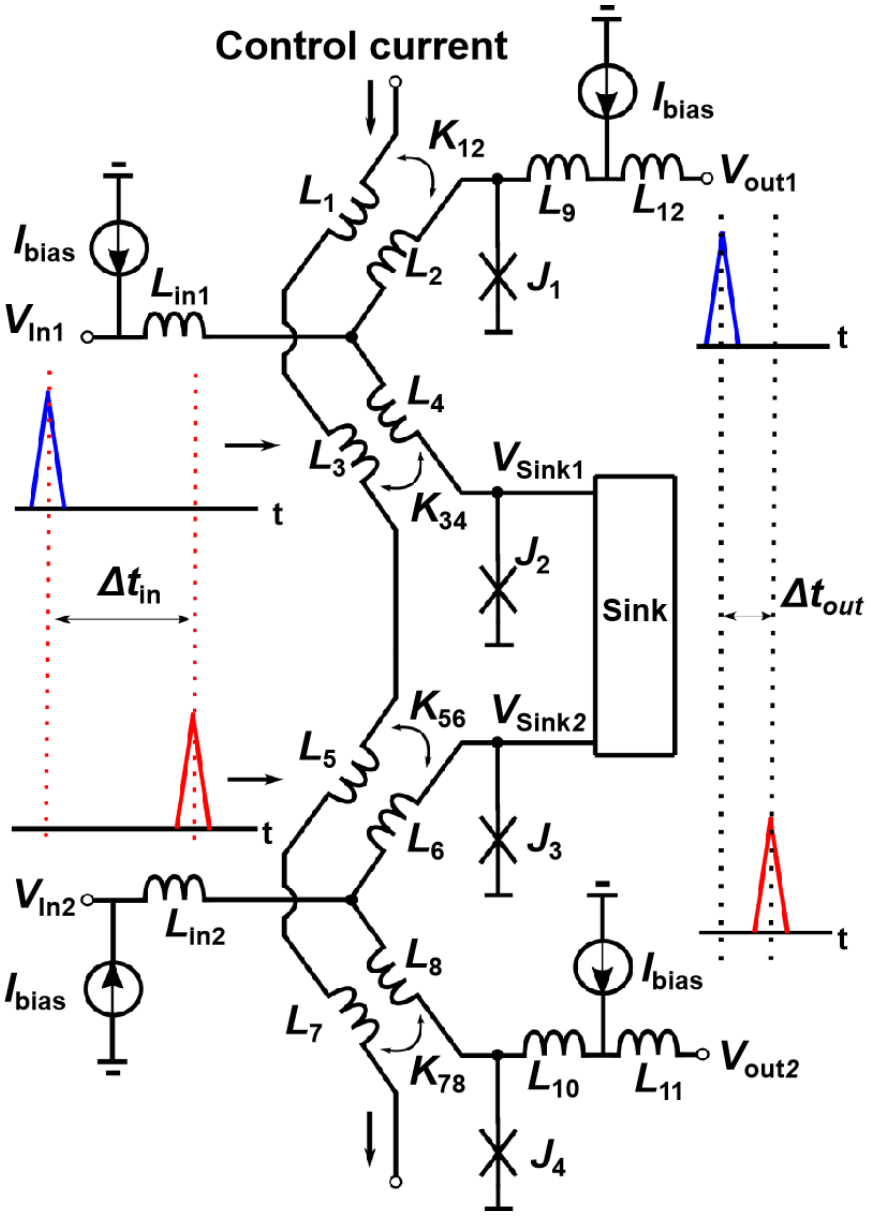


FIGURE 2.18: Delay Generator (DG)

2.5 Microwave Generator With Pair Pulses

In this section will introduce the microwave generator structure and operation principle. Besides we will give the photo of fabricated chip and measurement result.

2.5.1 Microwave Generator

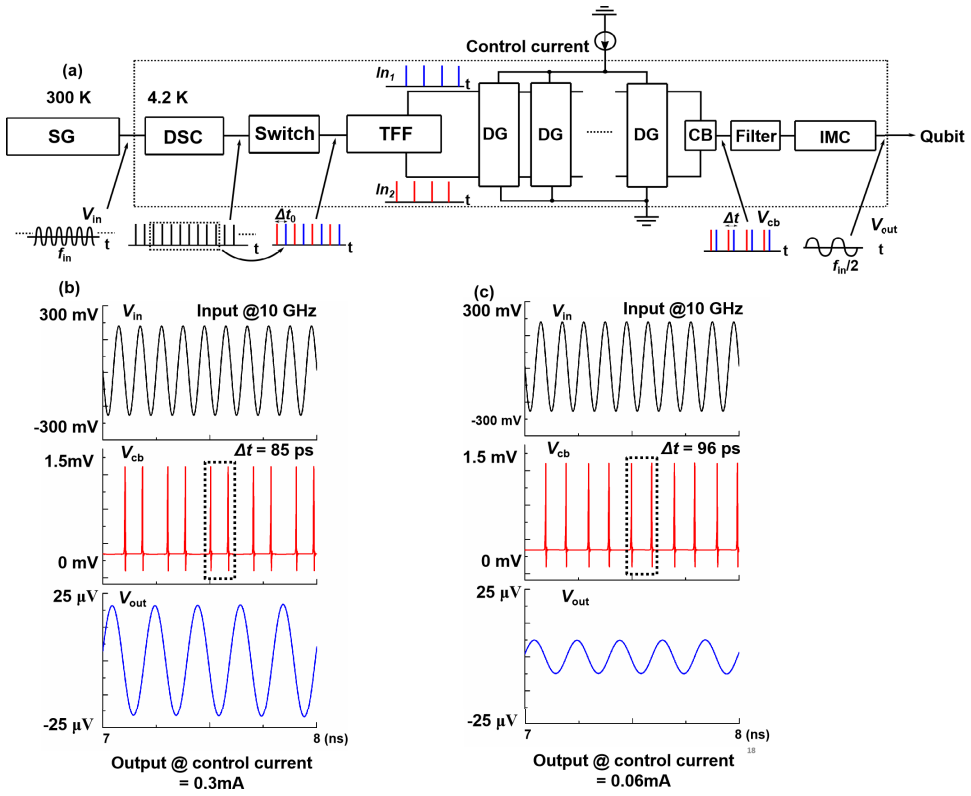


FIGURE 2.19: Microwave generator and operation principle

Here, we present the structure of microwave generator designed by SFQ cell in Fig.2.19. Here the SG is the signal generator, IMC is the impedance matching circuits. The structure is presented in Fig.2.19 (a).

The point of the PP-MPG is that (i) the output microwave amplitude can be controlled by the time difference Δt between paired SFQ pulses, and that (ii) the output microwave frequency f_{out} is separated from the input microwave frequency fin as $f_{out} = f_{in}/2$ to prevent the crosstalk between the input and output microwaves. The operation of the PP-MPG is as follows: A continuous microwave with a frequency of fin from a signal generator (SG) is applied to the DC/SFQ converter (DSC). Then, the DSC produces a continuous SFQ pulse train with an iteration frequency of f_{in}, and the following SFQ switch chops the continuous pulse train into a pulse train with an appropriate length. Furthermore, the two-output T flip-flop (TFF) lets the pulses from the SFQ switch travel to the two output ports alternatively, thus making two output pulse trains. Each pulse train includes half the number of the input pulses and thus has an iteration frequency of $f_{in}/2$. Moreover, the two pulse trains have a phase difference of

π, i.e., a time difference of Δt_0. Δt_0 is then changed to Δt by letting the two pulse trains travel through cascaded delay generators (DGs), the details of which will be explained later. Moreover, the confluence buffer (CB) merges the two pulse trains from the DGs and thereby produces a train of paired pulses, each with a time difference of Δt. Finally, a microwave pulse with a frequency of $f_{out} = f_{in}/2$ and an amplitude determined by Δt is generated from the pulse-pair train by the filter and impedance matching circuit (IMC).

Figure.2.19 (b) and (c) show simulation waveforms of the PPG by a Josephson circuit simulator, JSIM, for $f_{in} = 10\,GHz$ and $f_{out} = f_{in}/2 = 5\,GHz$, where V_{in}, V_{cb}, and V_{out} denote the input microwave, the SFQ pulses from the CB, and the output microwave, respectively. The left-hand waveform are for $\Delta t = 85\,ps$, and the right-hand ones are for $\Delta t = 96\,ps$. The comparison between the left-hand and right-hand waveform clearly indicates that V_out changes with Δt. This is because as Δt decreases, the f_{in} component in V_{cb} decreases whereas the f_{out} component in V_{cb} increases.

Low pass filter is presented at Fig.2.20. The typical T Type low-pass filter is applied with 2 stages. The simulation of S-parameter result is given at bottom. Simulator is Advanced Design system (ADS). Cut frequency of filter is about 6.5 GHz. Attenuation gradient is about 40dB/dec with 2 stages of filter for saving chip area. Here we use the low-pass filter to generate microwave. This part can be exchanged to band-pass filter and there is an improvement about removing the IMC which is applied in band-pass filter. This method will be introduced in the later chapters.

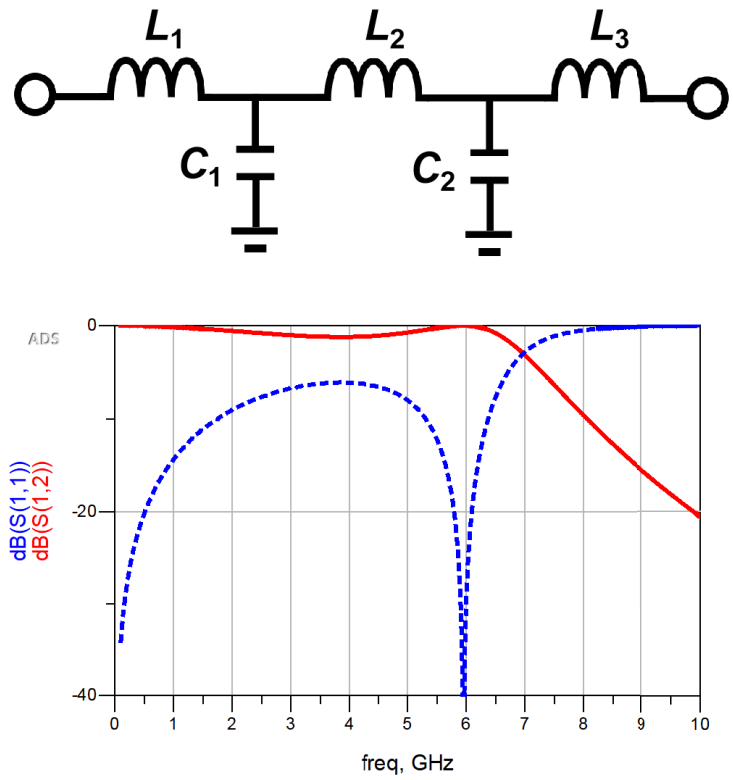


FIGURE 2.20: Low-pass filter

TABLE 2.1: Chip parameter.

No.	Parameter name	Value
1	Chip Area	3000 μm $\times$ 1000 μm
2	Input Signal Frequency	10 GHz
3	Output Signal Frequency	5 GHz
4	Cut frequency of Filter	6.5 GHz
5	Numbers of JJ	170
6	Bias Current (total)	20 mA

2.5.2 Photo and Parameter of Fabricated Circuits

Here, we present the photograph of microwave generator chip. The chip is fabricated by AIST $10kA/cm^2$ Nb high-speed standard process (HSTP)[38]. The chip contains the verification function for TFF at low speed. Besides We set 8 DGs to expand the interval of pair pulse and all DGs apply the independent control current. The margin will be wide and system become controllable easily but it sacrifices the power consumption. It can be improvement in the future. The parameter is given as at Tab.2.1. Although the area arrives about 3000 μm $\times$ 1000 μm, the most area is the parts of low pass filter and IMC. As mentioned, the output frequency is close to qubit oscillation frequency which is 5 GHz. Therefore,the input frequency is set to 10 GHz according to the operation principle. Total bias current arrives about 20 mA because DGs arrays occupy lots of cells.

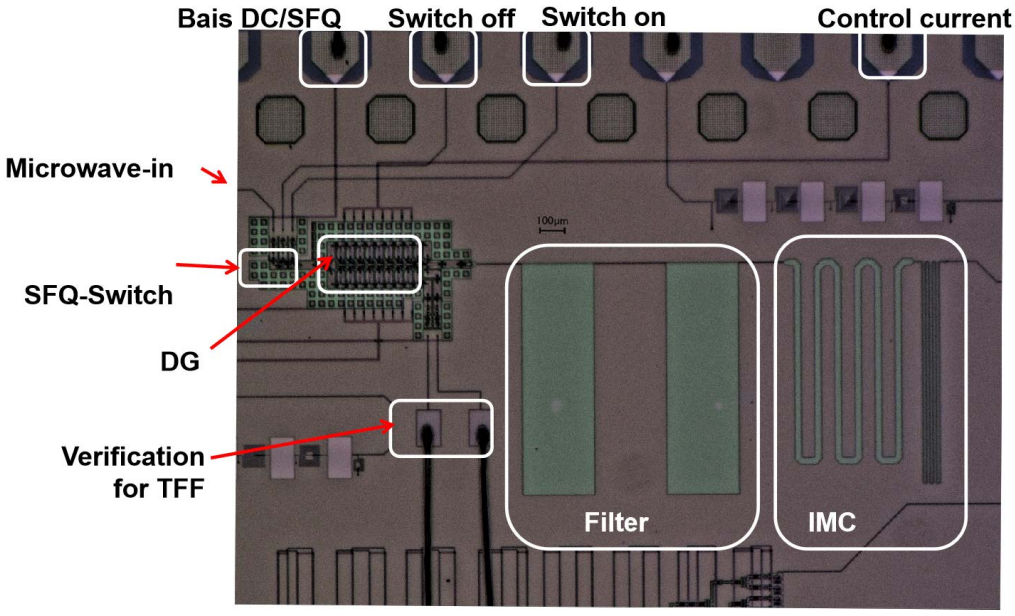


FIGURE 2.21: Photograph of chip

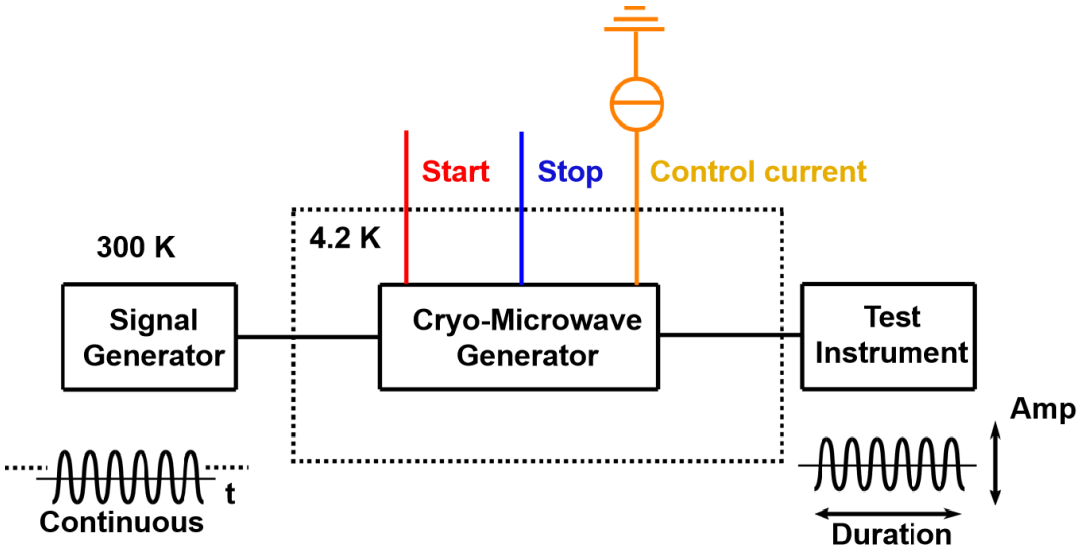


FIGURE 2.22: Measurement process

Then, we will introduce the environment of measurement. The most objects of investigation are duration time and amplitude of microwave as Fig.2.22. The continuous signal is input from room temperature, here, we set it to 10 GHz sine signal. The start (red) and stop (blue) SFQ pulse signal will control the duration of microwave. The control current (yellow) have impact on the amplitude of microwave. We put the circuits into liquid helium so that the environment temperature can be cooled down to 4.2 K. The test instrument can be chosen and it is spectrum analyzer generally.

2.5.3 Function Verification Under Low Speed

Here, we present the function verification process and result in Fig.2.23. In the function verification, we mainly pay attention on the TFF cells within low speed. Because the latency caused by DGs is very small, about several picosecond, it is very hard to be detected under low speed. Fig. 2.23 (a) illustrates the measurement method. We input a series of square wave within room-temperature. One square is transformed to one pulse on the chip. The pulse on and pulse off control the interval of the pulse sequence. Output of TFF is separated and detected by SFQ to DC converter (SDC). Fig. 2.23 (b) exhibits the experiment result. Here, the frequency of input pulse sequence is 100 kHz. The output of the TFF can be available only between the pulse on and pulse off. One rising or falling edge of output wave means one pulse generated. The result shows the TFF circuits divide the pulses well.

The function verification is required is that we can observe directly the SFQ pulse can be chosen by switch under low speed. It is hard to observe the generated microwave whether the duration has been chosen because crosstalk is very strong under high speed frequency. What's more, the generated microwave is small and it is mixed with noise. The function verification can help us to confirm the margin of DC bias current. Especially, the TFF cell is important for generating microwave. It is better to get the margin under low speed in advance of high speed measurement.

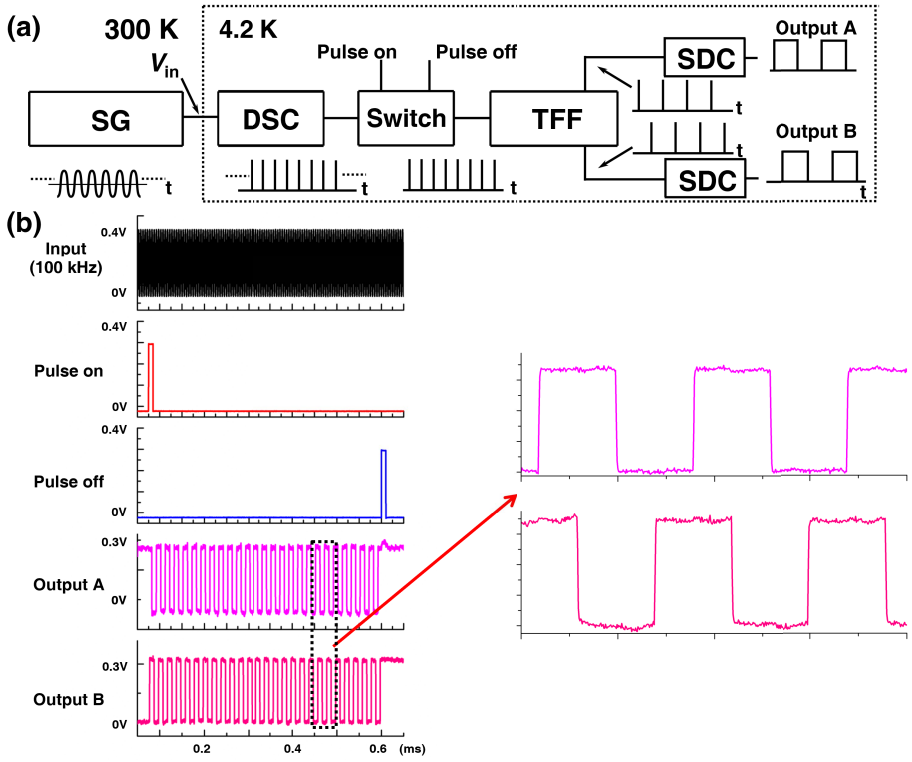


FIGURE 2.23: Operation function of verification under low speed

2.5.4 Measurement Under High Speed

Duration Measurement Under High Speed

on Fig.2.24, we can adjust the duration of start (red) and stop (blue) signal to control the duration of microwave and the phenomena has been observed directly under low speed. The sampling period is decided as fig .2.24 shows. The interval between start and stop will change the duty ratio of microwave which will reflect on the measurement result obtained by spectrum analyzer. Under duration measurement, we set the control current to a constant.

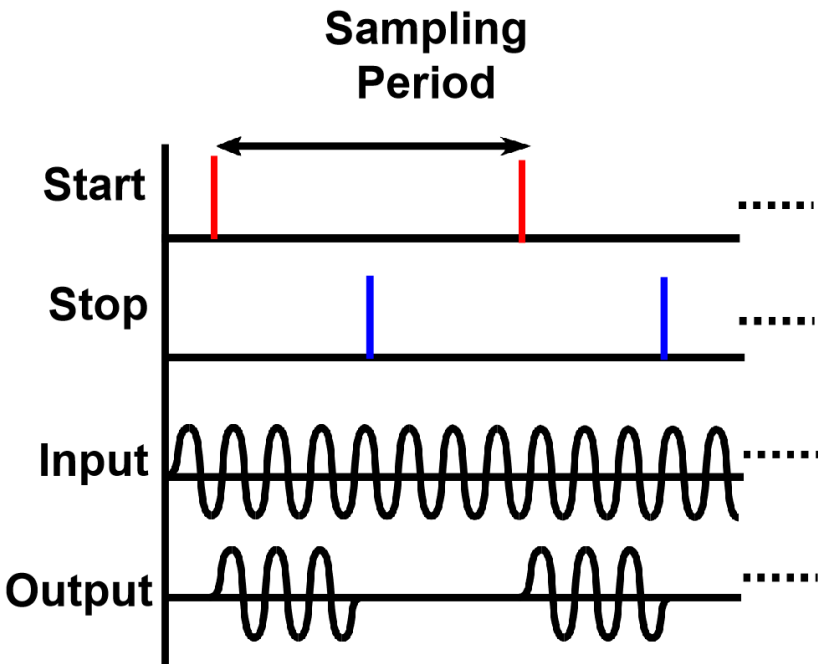


FIGURE 2.24: Duration measurement process

In this case we use oscilloscope to observe the waveform firstly. The signal should be amplified by 36 dB so that can be observed theoretically. The result is presented on Fig.2.25. Here, we apply the input output signal continuously to observe the waveform. The color grid method should be used to do the statistics on probability of microwave. According to the measurement, there was a small increase in the output signal at period of start and stop. The transmission latency is about 15 ns mainly caused by prob and test instrument.

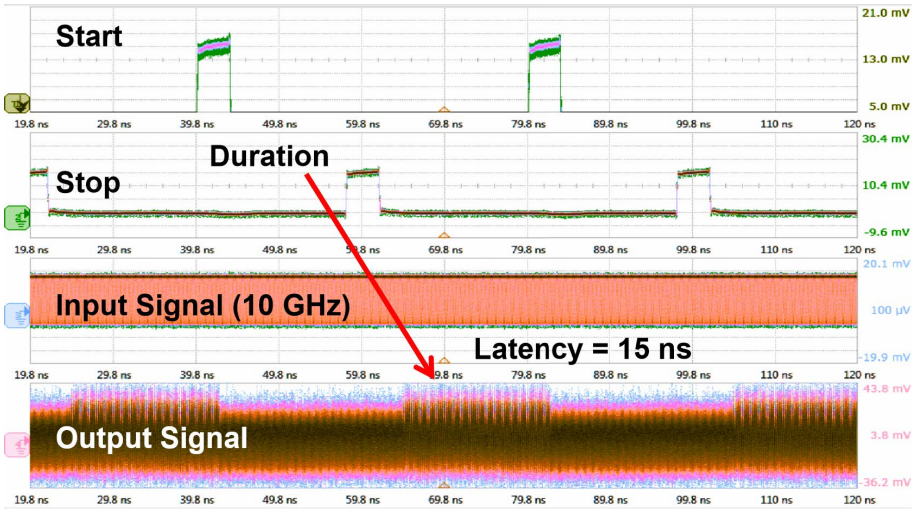


FIGURE 2.25: Microwave detection on oscilloscope

Then, we will use the spectrum analyzer to detect the sampling frequency whether

occurs. According to Fig.2.24, the continuous output microwave is cutoff intermittently. Refer to Fig.2.26, we will explain the sampling theorem with quantitative analysis. Generally, continuous microwave's Fourier transform is given as follows:

$$F(\omega) = \pi(\delta(\omega - \omega_0) + \delta(\omega + \omega_0) \tag{2.25}$$

Here, the ω_0 is frequency of microwave. And the microwave which is cutoff intermittently can be seen as sampling microwave using square function. The frequency of square function is sampling frequency (ω_s) and function can be presented as (2.26). Here, $f_s(t)$ is signal which has been sampled. $f(t)$ is sampled function and $s(t)$ is sampling function.

$$f_s(t) = f(t) \times s(t) \tag{2.26}$$

$$F_s(\omega) = \frac{1}{2\pi} F(\omega) \bigotimes S(\omega) \tag{2.27}$$

Fourier transform of function (2.26) is presented as (2.27). Then we set the sampling function to square function, and sampled function is microwave. The formula of (2.27) can be presented as follows:

$$F_s(\omega) = \frac{1}{2\pi} \times \frac{2\pi\tau}{T_s} \sum_{n=-\infty}^{\infty} Sa(\frac{n\omega_s\tau}{2})\delta(\omega - n\omega_s) \bigotimes F(j\omega) \tag{2.28}$$

$$F_s(\omega) = \frac{\tau}{T_s} \sum_{n=-\infty}^{\infty} Sa(\frac{n\omega_s\tau}{2})F(j(\omega - n\omega_s) \tag{2.29}$$

$$F_s(\omega) = k \sum_{n=-\infty}^{\infty} Sa(kn\pi)F(j(\omega - n\omega_s) \tag{2.30}$$

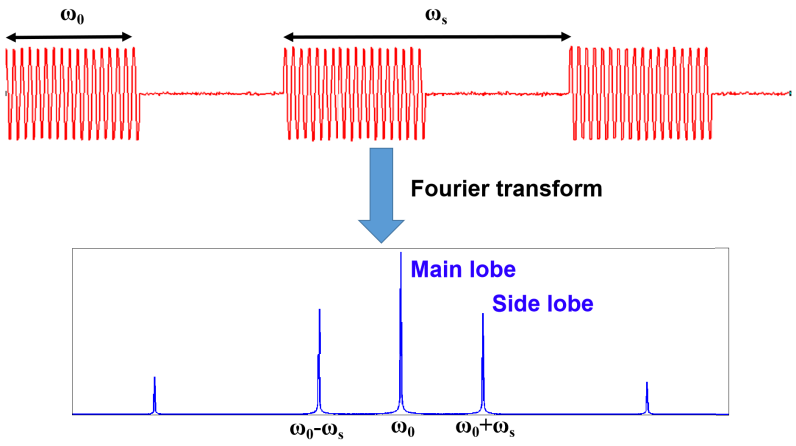


FIGURE 2.26: Fourier transform of intermittent microwave

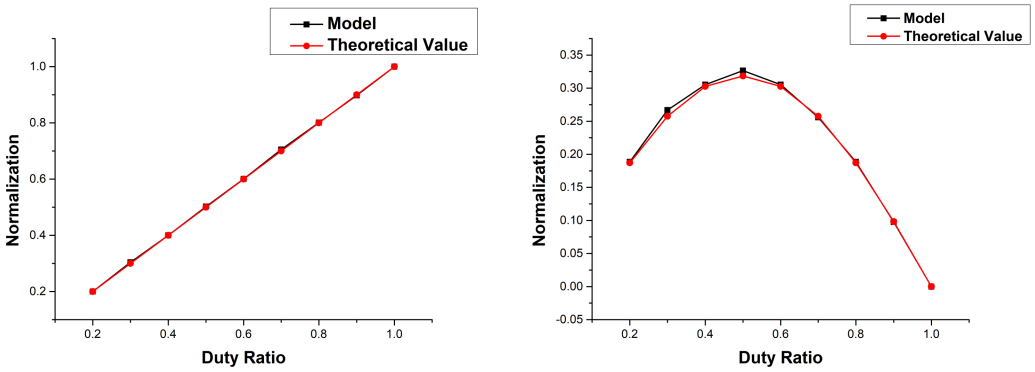


FIGURE 2.27: Main Lobe and Side Lobe vs. Duty Ratio

Here, the τ is the width of sequence function and T_s is sampling frequency. The duty ratio can be present as τ/T_s. Formula (2.28) shows that the frequency of main lobe should be $\omega_0/2\pi$ when $n = 0$. The frequency of side lobe should shift by $\pm\omega_s$ when when $n = 1$. If we set the duty ratio as k, the formula (2.29) can be written as (2.30). k decide the numbers of lobe before the first zero point. For example, we set the $k = 50\%$, there is only one side lobe before the first zero point.

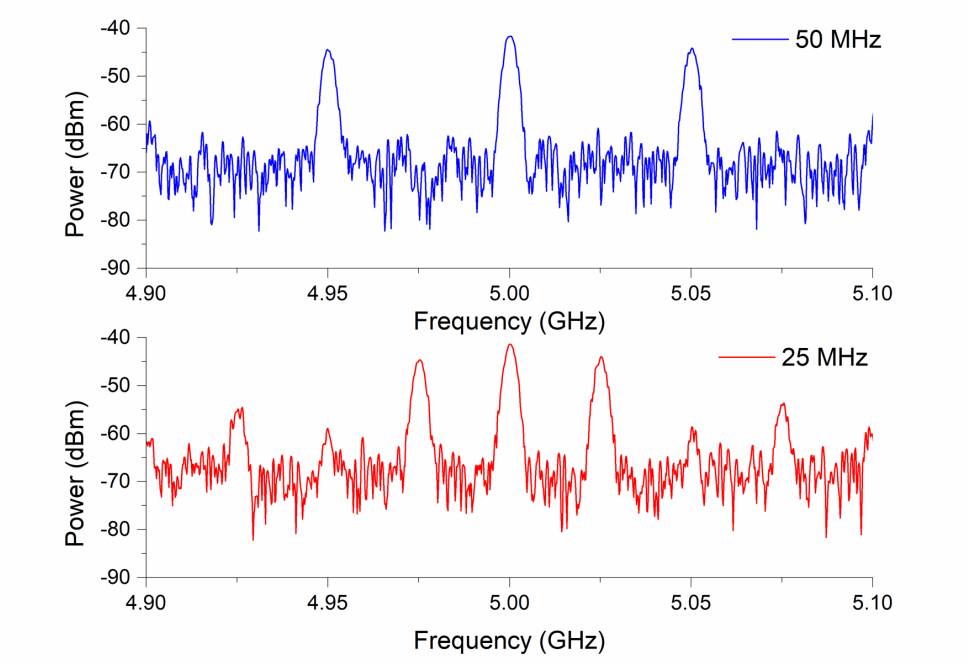


FIGURE 2.28: Measurement Duration Result

Then we do the mathematical model using the Matlab tools. The filter is set to chebyshev I type. We do Fourier transform to waveform presented at top of Fig.2.26. Besides, we add the thermal noise to simulate the circuits environment. The result is given at bottom of Fig.2.26. The waveform is match the expectation. The variation trend of main lobe and side lobe vs. duty ratio is presented at Fig.2.27. This model is almost the same with theoretical value. The main lobe is linear to duty ratio. The side

lobe is largest when duty ratio is 50%. That means when duty ratio is less than 50%, sampled signal does main favour. when duty ratio is beyond 50%, sampling frequency does main favour. The value of model is little bigger than theoretical value because of added thermal noise and designed filter model owns the decay.

The measurement is presented at Fig.2.28. As analyzed before, if we set the duty ratio to 50%, there is only one side lobe before zero point. In this measurement, we keep the control current to constant (0.3 μA). We present two examples which the sampling frequency is 50 MHz and 25 MHz. As figure shows, the sampling frequency can be revealed at side lobe. As fig.2.27 presented, the ratio of main lobe and side lobe is about 0.6 ($sidelobe/mainlobe$) when duty ratio is 50%. Signal power will decay by 0.36 and we transform it to power, which is about 4.43 dBm. That means the difference between main lobe and side lobe will arrive 4.43 dBm, where measurement value is near to this value.

Amplitude Measurement Under High Speed

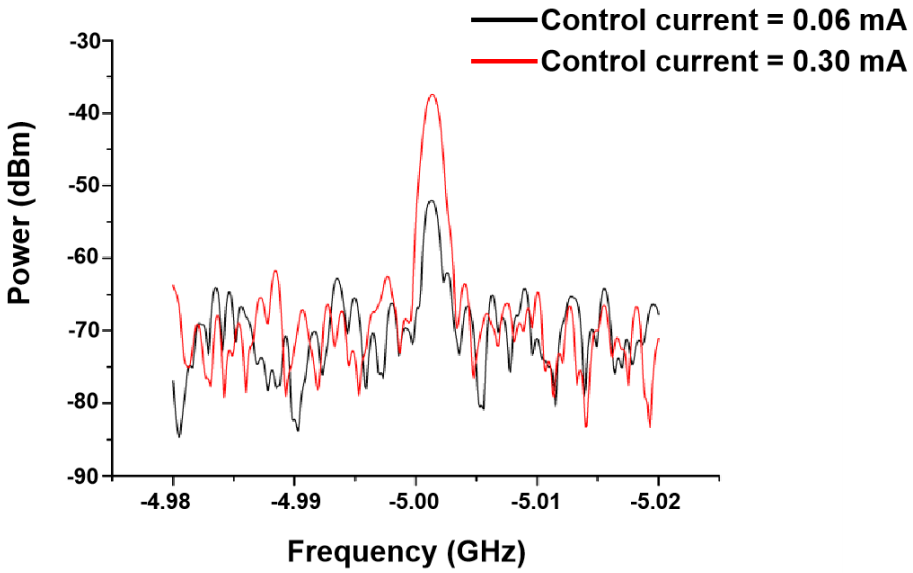


FIGURE 2.29: Measurement result with different control current

Fig.2.22 reveals the measurement process and here we remove the stop (blue) signal so that the output microwave will be continuous. The side lobe will be removed and we just need to change the control current (yellow) to change the amplitude of microwave. It is obvious that the amplitude of microwave will be revealed on the value of main lobe.

Here, we give the measurement result in Fig.2.29. The experimental instrument is spectrum analyzer. The amplitude change is very to be observed at oscilloscope because strong cross talk signal and thermal noise. Here,We amplify the signal (+38 dBm) and input to the analyzer. In this measurement we modulate the control current to present the value of main lobe. Fig. Fig.2.29 exhibits the experiment result. We scan the frequency from 4.9 GHz to 5.1 GHz and the main lobe is available at the 5 GHz because of TFF circuits. We set the control current to 0.3 mA and the main lobe is 38.67 dBm. The power is about 5.3 dBm larger than the signal which is sampled. It is close to theoretical value according to sampling theorem. Then we set the control current to 0.06 mA the main lobe falls to 52.73 dBm. That is because the control current makes the pulses duration smaller. Thus, the amplitude value of microwave will be larger.

We make a summary of the output power and control current in Fig.2.30. We present output current and output power with the control current. The variation tendency shows a parabola type. The red line shows the measurement data and black line shows the simulation data. We simulate the output power consumption with load 50 ohm. We transform the measurement data by removing the enlargement factor, which present a parabola shape as well. The tendency between the simulation and measurement is resemblance. The data of simulation is little larger than that of the measurement when the control current is from 0 to 0.3 mA. It is due to the attenuation

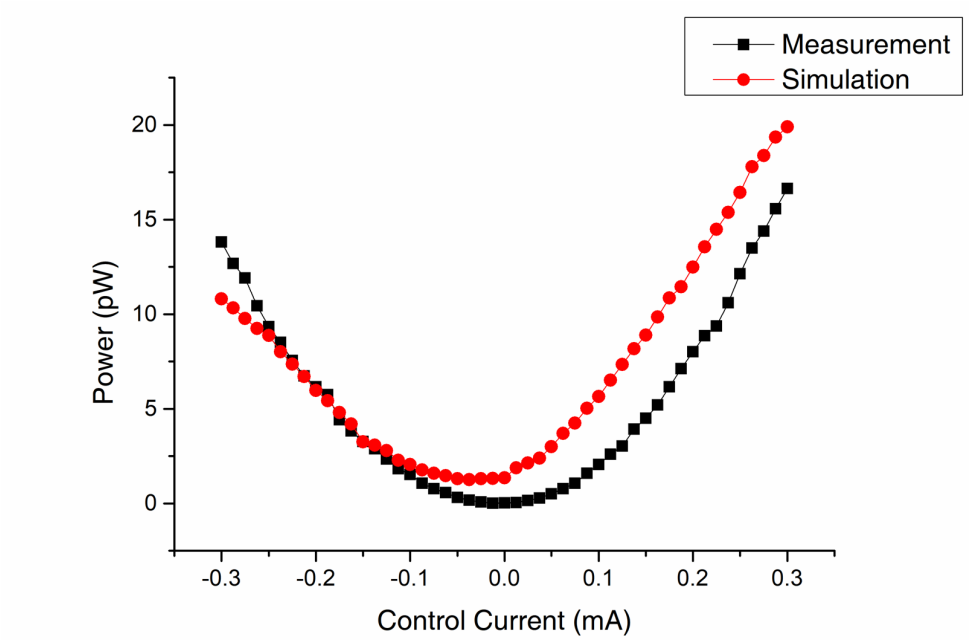


FIGURE 2.30: Signal strength vs. different control current

TABLE 2.2: Circuits Margin of Measurement

No.	Parameter name	Value
1	Margin of Bias current (Design)	$[-17\%\ 15\%\mu]$
2	Margin of Bias current (100 kHz)	[-15% 10%]
3	Margin of Bias current (5 GHz)	[-15% 4%]
4	Range of Control Current (Design)	[-3.2 mA 3.2 mA]
5	Range of Control Current (Measurement)	[-2.4 mA 2.4 mA]
6	Success rate of Measurement	4/5

excited in the measurement equipment (such as cables or probes). The result is not exactly symmetry because of the circuits parameter. Thus, the amplitude of output will be linear when control current is positive.

2.6 Conclusion

In conclusion, we suggest a variable amplitude microwave pulse generator circuits with superconducting circuits. We integrate the SFQ circuits and low pass filter on the chip and measurement at 4.2 K. We confirm the function of the circuits with low-speed signal at first. Then we apply the 10 GHz microwave to the MPG and the on-chip circuits can generate the 5 GHz output microwave. We observe the main lobe of the microwave in the spectrum analyzer when we modulate the control circuits. We confirm that input the larger control current, the system can generate larger microwave amplitude. At the control current range of 0 mA to 0.3 mA, the amplitude can achieve linear feature. Based on PPG system, it reveals the potential of controlling the microwave envelop if the control current can be controlled. What's more, we confirm the duration of microwave can be controlled according to the sampling theorem. It can be observed directly on the oscilloscope, however, the cross talk and noise have impact on it. The measurement result is given at Tab.2.2.

However, the control signal of this microwave generator is required from room temperature. To QEC system, the message from qubit should turn back to classic computer then feed back to microwave generator. To achieve the goal which is presented in Fig.1.3, we suggest to design a control system under cryogenic temperature with superconducting circuits or cryogenic circuits. The main targets for controlling are duration and control current.

Chapter 3

Timing Controller Circuits And Integrator Using AQFP

In this section we will introduce the timing controller and integrator circuits designed by Adiabatic Quantum Flux Parametron Circuit (AQFP). As mentioned, the quantum control and read-out system is required to implemented with cryogenic temperature. In the previous chapter, we introduce the microwave generator designed with SFQ circuits. However, the SFQ circuits owns a disadvantage is that it will cost lots of power on quiescent dissipation because it is required bias current all the time. DC-bias current will produce lots of thermal noise so that it will have impact on Quantum process especially under mK. The low power consumption should be applied. fortunately, the AQFP can take on it because it has no DC-bias current to junction. Therefore, we desired to design the controller with AQFP.

On the other hand, the state of qubit can be readout by Josephson parametric amplifier (JPA) or Josephson parametric oscillator (JPO). Thus, we can observe the phase shift to calculate qubit state and phase can be read out by AQFP circuits. To improve the sensitivity of readout system, we design the integrator using AQFP circuits. All the circuits structure and measurement result within 4.2 K will be presented in this chapter.

3.1 Adiabatic Quantum Flux Parametron (AQFP)

AQFP circuits can operate with energy dissipation close to the thermodynamic. Therefore, it can be an energy-efficient superconductor logic element based on the quantum flux parametron. There are many researches about AQFP have been reported and the logic cells designed by AQFP have been established. This section we will introduce the operation of AQFP and logic cell made by AQFP.

3.1.1 Structure of AQFP

Here, we present the schematic of AQFP in Fig.3.1 (a). Excitation current is applied to add the external flux to the loop. The external current from L_1 is added to L_4 though coupling factor K_1. The loop left contains the J_1, L_4, L_6 and loop right contains the J_2, L_5 and L_6. Assume that the structure is symmetrical and $J_1 = J_2$, $J_4 = J_5$, the external flux which is from excitation current is the same to two loops. The flux cause the current is the opposite direction in inductance L_6. Thus, the loops function can be given as follows:

$$\phi_{J1} = \frac{2\pi L_6 I_6}{\Phi_0} - \frac{2\pi L_4 I_4}{\Phi_0} - 2\pi\frac{\Phi_{ex}}{\Phi_0} \tag{3.1}$$

$$\phi_{J2} = \frac{2\pi L_6 I_6}{\Phi_0} + \frac{2\pi L_5 I_5}{\Phi_0} + 2\pi\frac{\Phi_{ex}}{\Phi_0} \tag{3.2}$$

Here, we define the clockwise direction as positive current. The Φ_{ex} is external flux. According to (3.1) and (3.2), the formula can be given as follows:

$$\phi_{J1} = -\frac{\pi L_5}{\Phi_0}(I_4 + I_5) - 2\pi\frac{\Phi_{ex}}{\Phi_0} - \frac{\pi L_4 I_{in}}{\Phi_0} \tag{3.3}$$

$$\phi_{J2} = -\frac{\pi L_5}{\Phi_0}(I_4 + I_5) - 2\pi\frac{\Phi_{ex}}{\Phi_0} + \frac{\pi L_4 I_{in}}{\Phi_0} \tag{3.4}$$

Here,we assume current I_in is input current and $I_in = I_4 - I_5$. The formula (3.3) and (3.4) reveals each JJ phases before switch. Once we input a external flux ($0.5\Phi_0$) the difference of JJ's phase will arrive more than 2π. It means at least one JJ will switch. Formula (3.34) reveals that once the input current is positive (red arrow), phase of J_1 will be beyond $-\pi$. The current on J_1 be reversed and generate a flux which is opposite of the original flux (red cycle). On the other hand, if input current is negative (blue arrow), the phase of J_2 will be beyond $-\pi$ and generate a flux which is opposite of the original flux (blue cycle). Therefor, the message can be propagated using this principle. It can be seen as a buffer and symbol is presented in Fig.3.1.

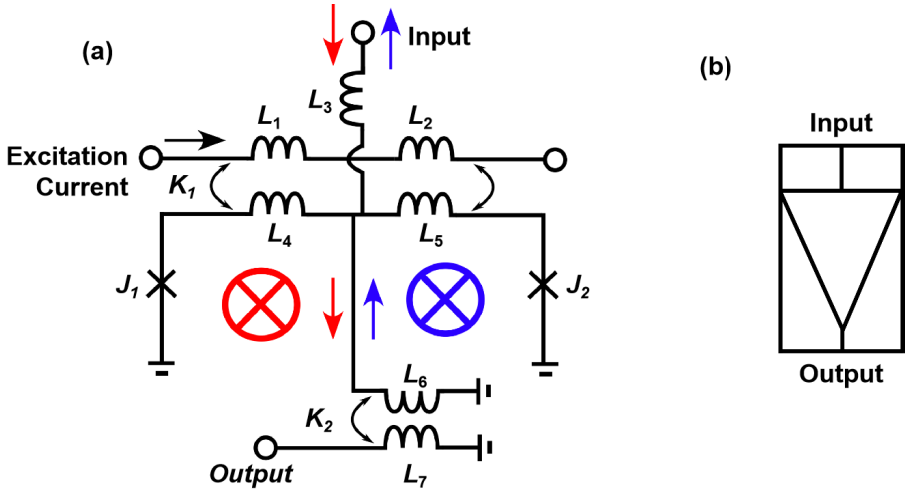


FIGURE 3.1: Schematic of AQFP and symbol

Then we will explain it why it performs adiabatically. The potential energy of is behaved by the sum of the energy stored in J_1, J_2, L_4, L_5, and L_6. The energy of J_1 and J_2 is presented as follows:

$$U_j = E_j(-cos(\phi_1 - \phi_2)) = -2E_j cos(\phi_-)cos(\phi_+) \tag{3.5}$$

Here, the $E_j = \frac{I_c\Phi_0}{2\pi}$, $\phi_- = (\phi_1 - \phi_2)/2$, $\phi_+ = (\phi_1 + \phi_2)/2$. I_c is is the critical current of junction respectively. The energy in the L_6 is given as follows:

$$U_m = E_j \frac{\phi_q^2}{2\beta_q} \tag{3.6}$$

Here, $\beta_q = 2\pi L_6 I_c/\Phi_0$ and ϕ_0 is the normalized flux associated with L_6.

The we add the potential energy with L_4 and L_5. Then the total energy stored in inductance can be presented as follows:

$$U_m = E_j \frac{(\phi_{L1}^2 + \phi_{L2}^2)}{2\beta_L} + E_j \frac{Œ_q{}^2}{2\beta_q} \tag{3.7}$$

Here, The $\beta_L = 2\pi I_c/\Phi_0$. ϕ_{L1} and ϕ_{L2} are the normalized fluxes associated. Generally, the energy $U = U_m + U_j$ and the function can be presented as follows:

$$\frac{U}{E_j} = \frac{\phi_q^2}{2\beta_q} + \frac{(\phi_+ - \phi_{in} - \phi_q)^2}{\beta_L} - \frac{(\phi_- - \phi_x)^2}{\beta_L} - 2cos(\phi_+)cos(\phi_-) \tag{3.8}$$

Here, the $\phi_{in} = 2\pi\Phi_{in}/\Phi_0$ is the normalized input flux and $\phi_x = 2\pi\Phi_x/\Phi_0$ is the normalized excitation flux. For facilitating the calculation, we remove the ϕ_q and assume the $\phi_- - \phi_x$ is close to zero. As a result, the formula can be approximated as follows:

$$\frac{U}{E_j} = \frac{(\phi_+ - \phi_+ - \phi_{in})^2}{\beta_L + 2\beta_q} + \frac{(\phi_- - \phi_x)^2}{\beta_L} - 2cos(\phi_+)cos(\phi_-) \tag{3.9}$$

The average energy dissipation per device of CMOS logic is presented as $\overline{E_d iss}$. The dissipation corresponds to about 20000 $k_B\ T$ at 300 K if we take the Intel's Xeon Platinum 8180 microprocessor as an example. It is far from the thermodynamic limit. Comparing to the superconducting logic, RSFQ, the average energy dissipation is about $0.8\overline{I_c}V_b/f$. Where, V_b is bias voltage and $\overline{I_c}$ is average critical currents of the Josephson junctions. Generally, we set the operation frequency to 50 GHz and $\overline{E_d iss} = 6 \times 10^{-18}$J, which corresponds to 10000 $k_B\ T$ at 4.2 K. As for AQFP logic circuits, the 8-bit carry look-ahead adder with $24k_BT$ at 5GHz[39]. AQFP has enormous advantage on power consumptions compared to other circuits.

Here, we present the variation trend of AQFP's potential energy in Fig.3.2. The initial state of AQFP is at bottom of valley. This time the potential energy is presented as blue solid line. Then the external flux is applied into loop, for example it arrives 0.25 Φ_0, the bottom of valley rises up and the black ball is arisen. When external flux arrives about 0.32 Φ_0, there is almost no barrier at the bottom of valley. The black ball will roll to one side if there is input from outside. In this example, we add input negative current and the ball roll to left side. Then the external flux arrives 0.5 Φ_0, the barrier becomes higher so that it blocks the ball's way to the other side. Thus, the state will keep stable. If the input current is positive, the ball will roll to the right side and state behaves 1. Assume the variation trend of barrier is very slow, it is just need a tiny current to make the ball roll to one side. That behaves adiabatic operation which is no power consumption under low speed operation in theory.

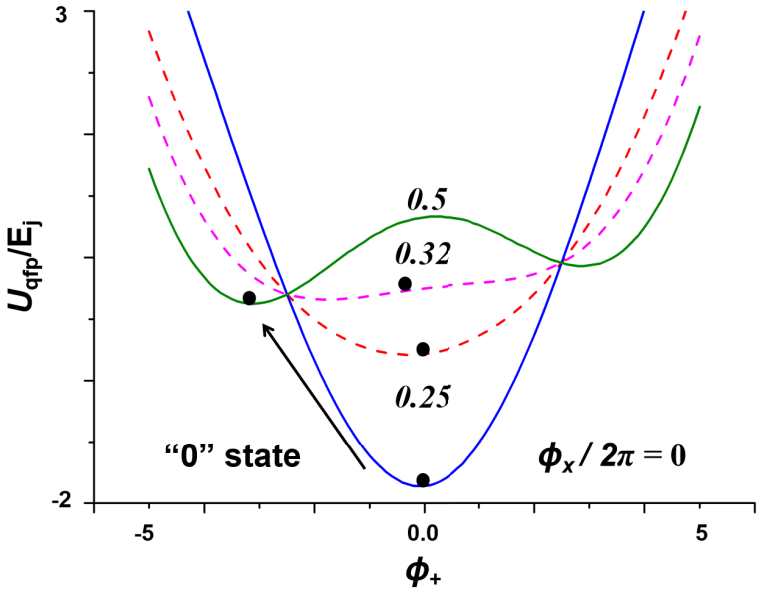


FIGURE 3.2: Schematic of AQFP and symbol

3.1.2 4-Phase Operation

Figure.3.3 shows the operation principle of AQFP. Generally, the message can be propagated by AQFP buffer when $0.5\Phi_0$ is applied into AQFQ circuits by excitation current. We apply this characteristic to design the AQFP logic circuits. We apply two excitation current signal (red and blue) to drive AQFP. It is obvious that the excitation signal (AC1) is $\pi/4$ ahead of excitation signal (AC2). The operation is presented as follows:

1. Value of AC1 arrives the maximum value and apply the $0.5\Phi_0$ to AQFP (No.1). Then the junction of No.1 switches and output large current to next stage AQFP.

2. Value of AC1 starts to fall down and the applied flux starts to decay. On the other hand, AC2 starts to rise and arrives to maximum value. $0.5\Phi_0$ is applied to AQFP (No.2), and the meanwhile, No.2 receive the message which is from No.1.

3. The opposite excitation current direction is applied to AQFP (No.3 and No.4). That means the applied flux direction is contrast to No.1 and No.2. Thus, when the AC1 arrives the minimum value, $0.5\Phi_0$ is applied to propagate the message.

4. No.4 owns the same operation principle with No.3 which is excited when AC2 arrives the minimum value. Therefore,the message is propagated with 4-phase.

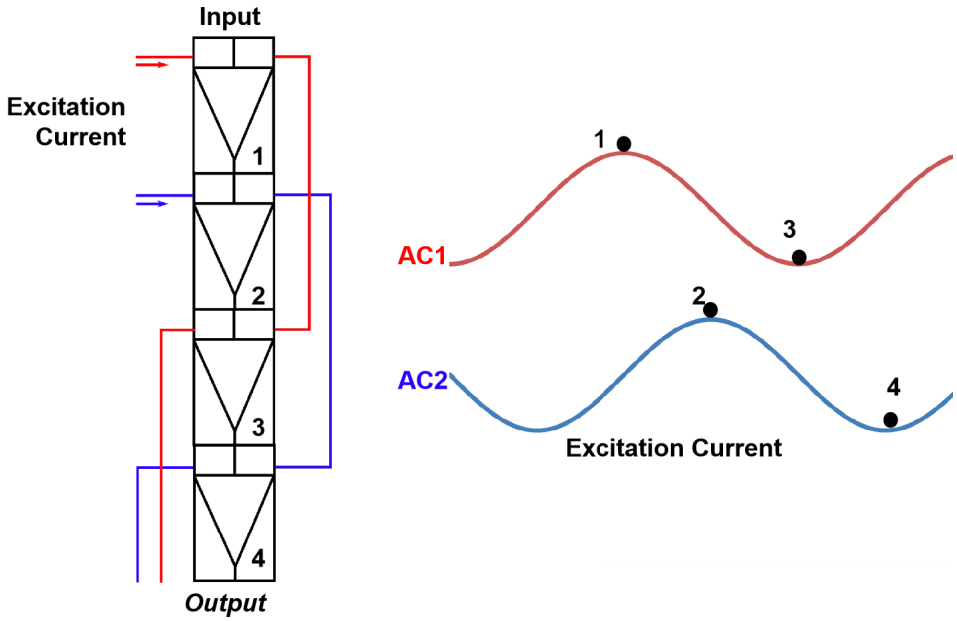


FIGURE 3.3: 4-Phase Operation principle of AQFP circuits

3.1.3 AQFP Logic Cells

In this section we present the logic function of AQFP and potential energy of each logic gate. In this section the used process is MIT $10kA/cm2$ Niobium processes.

AQFP buffer,inverter (inv) and constant to propagate the message is presented in Fig.3.4. shows the symbol of basic AQFP logic gate.

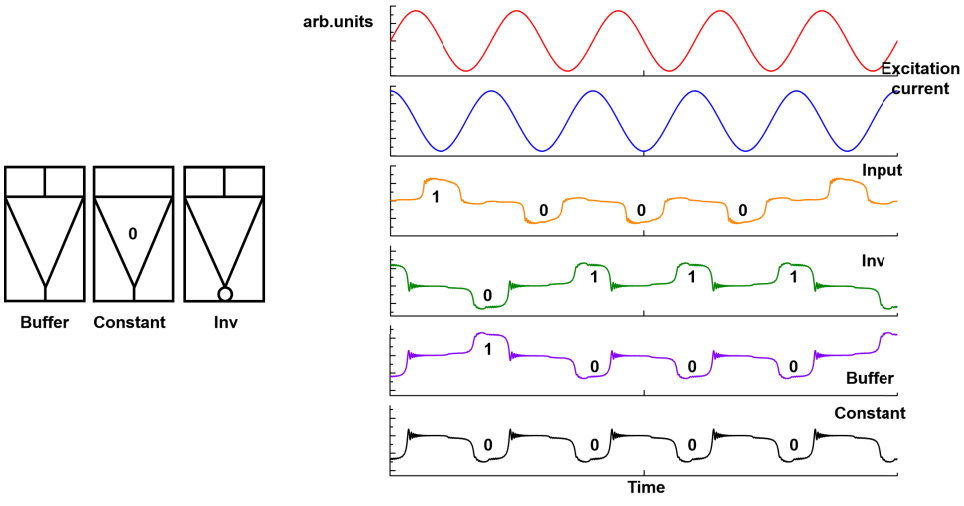


FIGURE 3.4: Basic AQFP logic gate

Fig.3.4. shows the symbol of basic AQFP logic gate. The schematic of buffer is presented in Fig.3.1. If we reversal the coupling fact (K_2), the we can get the inventer gate (Inv) which can reversal the logic of buffer. On the other hand, if the inductance L_5 is larger than L_4, the J_2 switch easily. Then the ball presented in fig.3.2 will roll to

left side without input and behave logic "0". The simulation result is presented on the right of Fig.3.4.

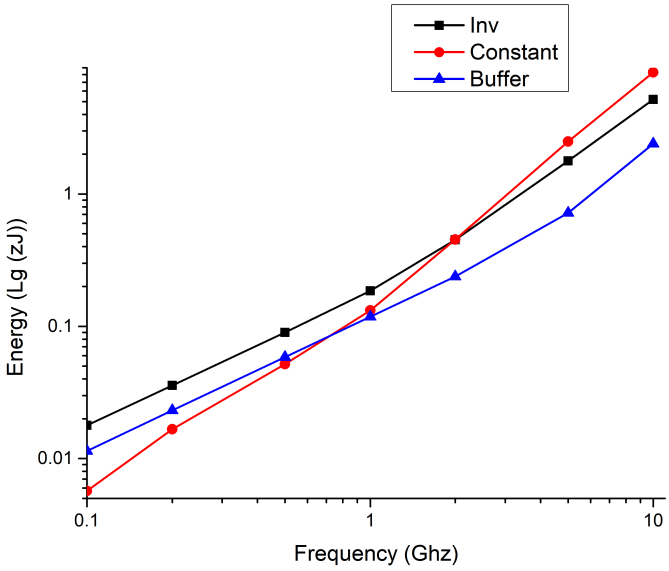


FIGURE 3.5: Potential energy of basic cell

The simulation result of potential energy is presented in Fig.3.5. Energy of three gates perform the linear vs. frequency. The Inv cost more energy because of circuits parameter. The constant perform lower power consumption because it do not need input.

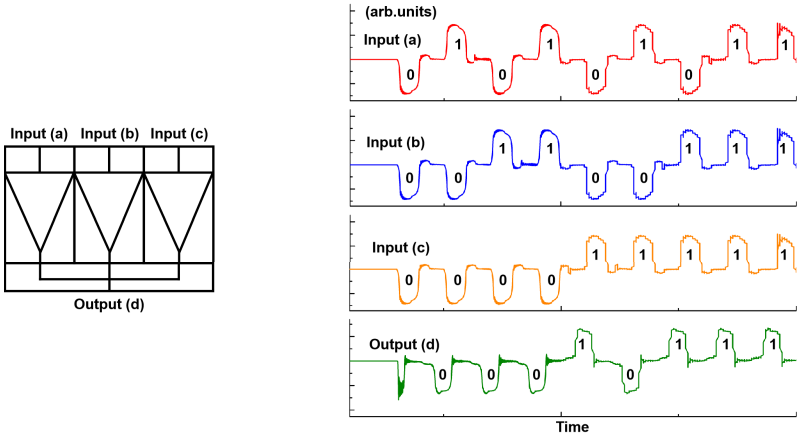


FIGURE 3.6: Majority 3 Gate

Here, we introduce another cell. There are 3 AQFPs is applied and output of them was connect with inductance. The output current from three AQFP and confluence to one point and output to next state. The logic simulation is presented on the right of Fig.3.6. The simulation shows that the output is the majority of input a, b, c. The output has 1/4 cycle latency because propagation characteristic of AQFP. We present the simulation result of energy variation trend of majority 3 in Fig.3.7. Because the

structure is symmetrical, we just present 4 input pattern as examples. The result reveals that when input is all 000, the energy changes linearly vs. frequency. On the other hand, the energy will trend to a fixed value with other pattern inputs. Because other pattern will led to the gate non-adiabatic and gate is still keeps adiabatic if the input is all the same. According to Thevenin's theorem, the output current can be given as follows:

$$d = abc + \bar{a}bc + a\bar{b}c + ab\bar{c} \tag{3.10}$$

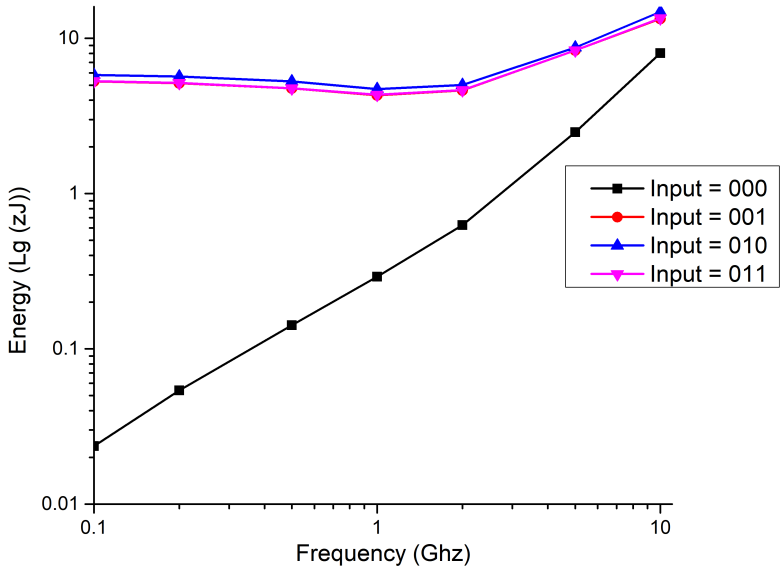


FIGURE 3.7: Energy Variation Trend of Majority 3

Once the cell in the middle of majority gate is constant, the majority gate can be transformed to AND/OR gate on the left of fig.3.8. The simulation result is presented on the right of fig.3.8. Here, the constant “1” can be realized by flip the constant "0" horizontally. The energy is presented in fig.3.9. Input 11 of OR gate and Input 00 of AND gate perform the adiabatic. The other almost perform the non-adiabatic. Totally, the variation trend of AND and OR is the same

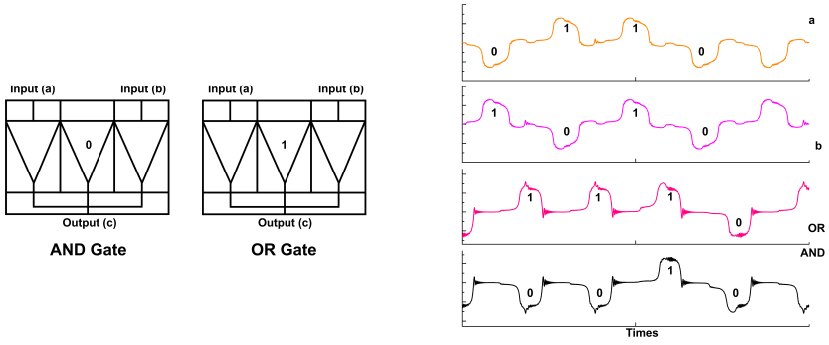


FIGURE 3.8: AND/OR Gate

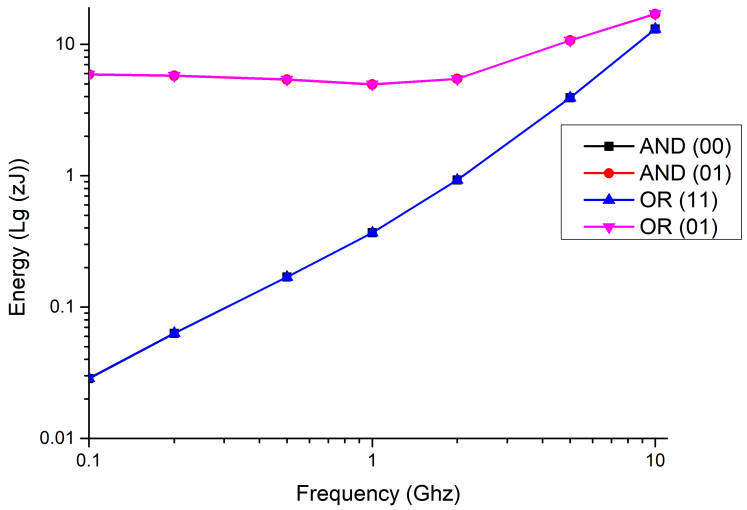


FIGURE 3.9: Energy of AND/OR Gate

Here, we present the majority 5 gate which can is similar with majority 3 gate. Majority 5 gate integrate 5 buffer cell so that it can calculate more data in one phase. However, the branch which is applied to connect the buffer will reduce the current. The margin of this cell seems narrower than majority 3 gate. The potentional energy is presented in Fig.3.11. Because the structure is symmetrical, there is only 10 pattern should be calculated. When the difference between the numbers "1" and "0" is 5, it behaves the adiabatic. When the difference between the numbers "1" and "0" is 3, it behaves the non-adiabatic and energy consumption is become lager. When the difference

between the numbers "1" and "0" is 1, energy consumption is become lagest. Especially, When the code is 00101.

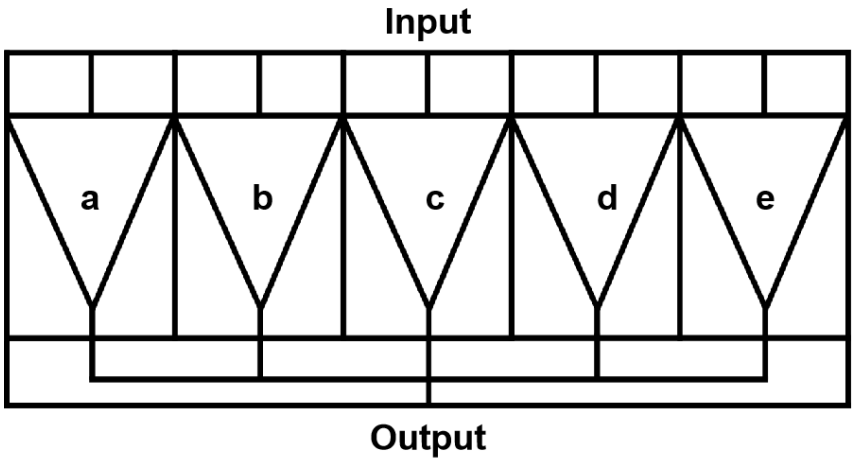


FIGURE 3.10: Majority 5 Gate

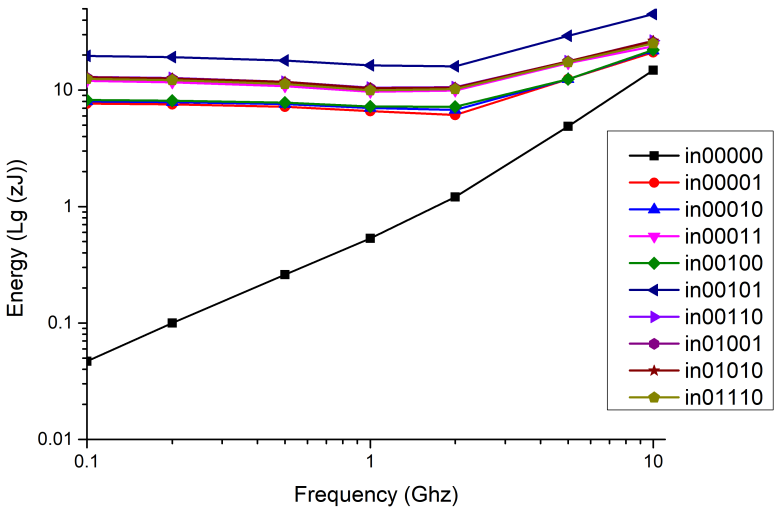


FIGURE 3.11: Majority 5 Gate

3.2 Timing Control Circuits With AQFP

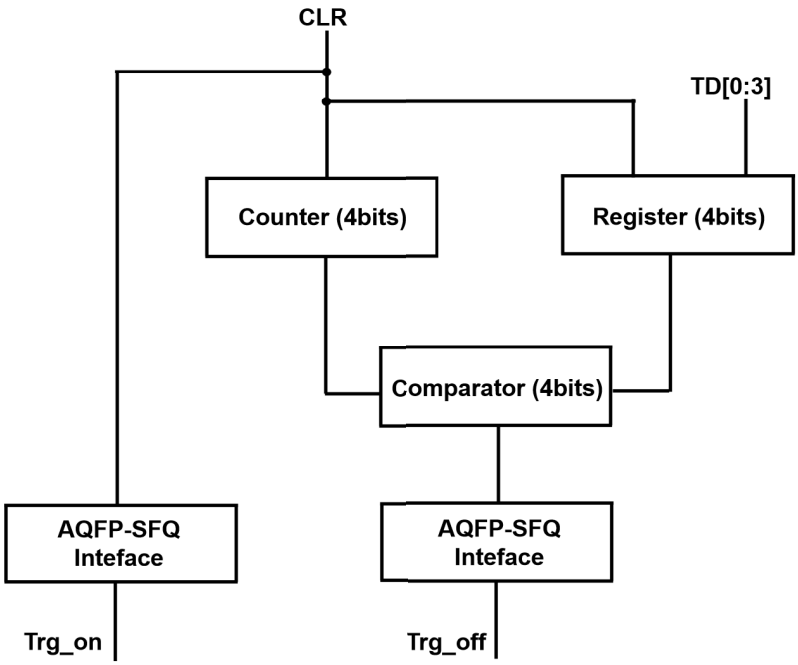


FIGURE 3.12: Timing controller using AQFP

As mentioned we prefer to design a duration system using low power consumption to applied in quantum process. The structure is presented in fig.3.12.

The system is mainly composed of a DC/SFQ converter, an SFQ-switch, an SFQ pulse duplicator, and a band-pass filter. During the operation, microwaves in the gigahertz range are supplied from room-temperature electronics to the microwave pulse generator at 4.2 K. The input microwaves are converted to an SFQ pulse train by the DC/SFQ converter, which generates an SFQ pulse at every rising edge of the microwaves. The continuous SFQ pulse train is then cut off at a specific length by the SFQ switch as determined by the SFQ pulses $Trig_on$ and $Trig_off$, which turn the propagation of the SFQ pulses on and off as depicted in Fig.3.12. The SFQ pulse train is then duplicated by the SFQ pulse duplicator, where the interval between the original and the duplicated SFQ pulses is varied by supplying a control signal given by an CMOS/SFQ amplitude controller. Finally, the duplicated SFQ pulse train is filtered by a superconducting band-pass filter to remove the harmonics of the SFQ pulse. The amplitude of the microwave pulse is changed by varying the interval between the original and duplicated SFQ pulses. When the interval is small, the microwave amplitude is large, and vice versa.

Counter (4bits)

We design a 4 bit counter which contains 4 half adders. The half adder is presented in Fig.3.13. It contains the one calculation cell which is presented at bottom of Fig.3.13. S means the sum bit and C means the carry bit. The XOR gate occupy two phase for calculation which is presented in solid square. The function is list as follows:

$$S = S' \bigoplus C' \tag{3.11}$$

$$C = S' \times C' \tag{3.12}$$

Then we set it as calculation cell to the half adder and we take the reset and input function into this cell. Here, the S_n means the output of sum bit at n-bit and the C_n means the output of carry bit at n-bit. This cell apply 4-phase feed back method where the S_n is used to calculate with CLR signal. Thus the function (3.11),(3.12) can be presented as follows:

$$S_n = (S' \bigoplus C') \times CLR \tag{3.13}$$

$$C_n = S' \times C' \times CLR \tag{3.14}$$

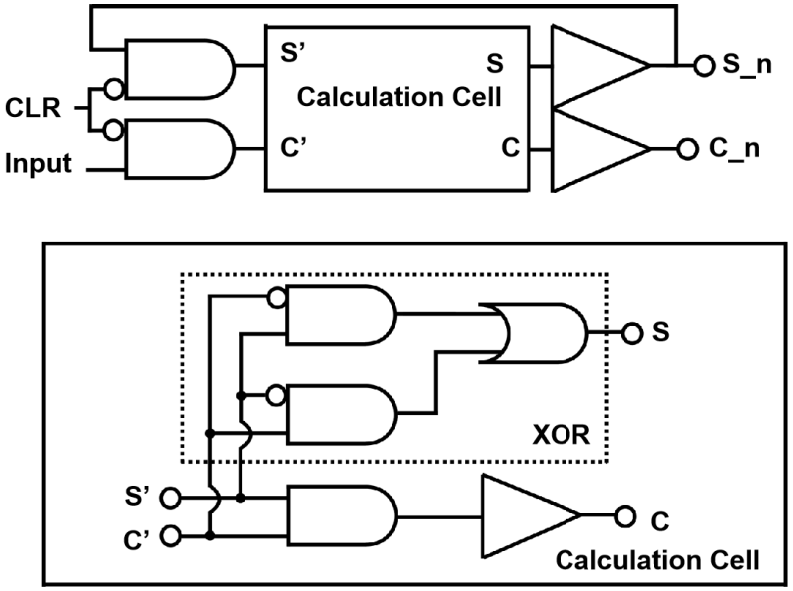


FIGURE 3.13: Half adder with AQFP

Thus the reset function is be added when CLR signal is logic "1". The counter structure is in Fig.3.14. The initial carry bit is input logic "1" continuously. CLR reset signal is applied in every cells by AQFP Buffer chain (hidden). The simulation is presented in fig.3.15. The data ($S_4S_3S_2S_1$) consists system code and counts up with one clock. When CLR_out signal becomes logic "1", system code become (0000).

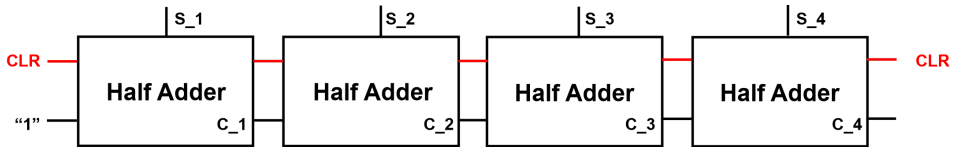


FIGURE 3.14: Counter with AQFP

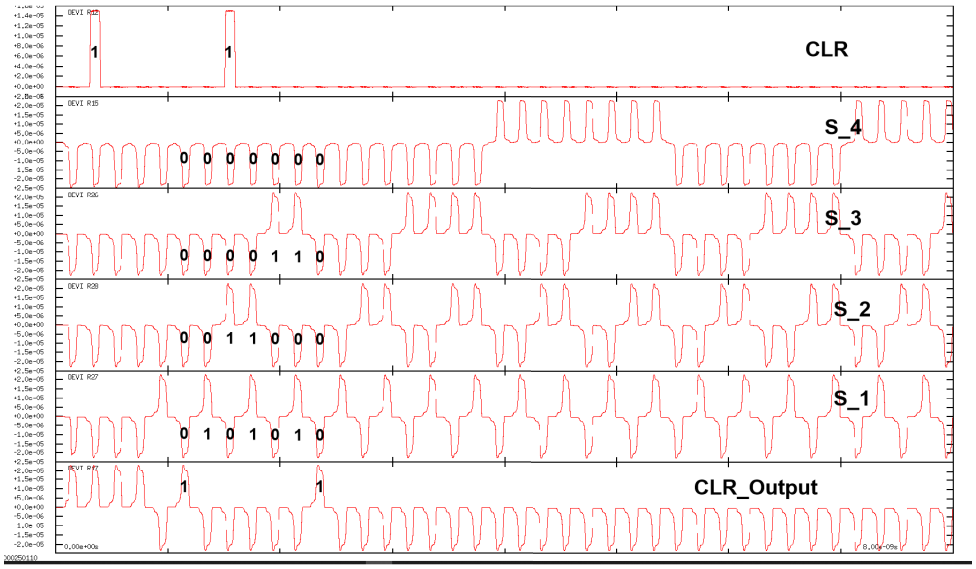


FIGURE 3.15: Simulation result of 4-bits counter

Register

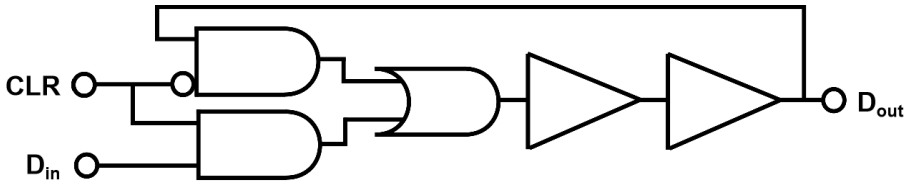


FIGURE 3.16: Structure of Register

Here, we present the register structure in Fig.3.16. Generally, the reset function should be applied. The function can be given as (3.15). When CLR signal is logic "0", the state of register becomes "hold" and register is keep the previous output state. When CLR signal is logic "1", the state of register becomes "write" and register behaves as buffer chain. The truth table is given as (3.16). Simulation result is presented in Fig.3.17. The result is match to expectation.

$$D_{out} = D'_{out} \times \overline{CLR'} + D_{in} \times CLR \tag{3.15}$$

CLR	D_{in}	D'_{out}	D_{out}	$State$
0	X	0	0	*Hold*
0	X	1	1	*Hold*
1	0	X	0	*Write*
1	1	X	1	*Write*

(3.16)

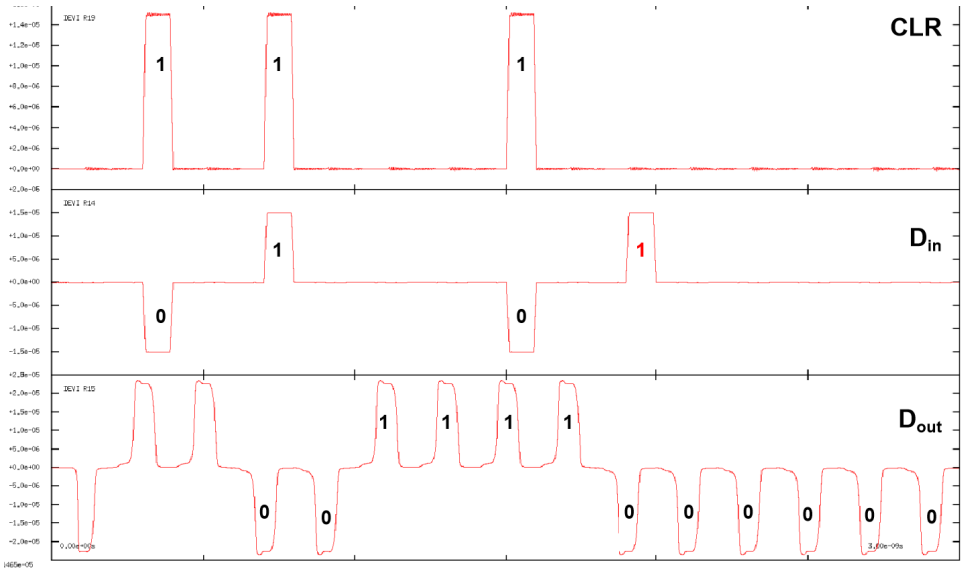


FIGURE 3.17: Simulation Result of Register

AQFP to SFQ Interface

As mentioned, the microwave is generated with SFQ circuits. We control the duration with AQFP circuits and we need a converter which can transform the AQFP signal to SFQ signal. Here, we give schematic of AQFP to SFQ converter in Fig.3.18. AQFP signal which behaves logic "1" input as red arrow. The excitation current apply external 0.5 Φ_0 to the loop which contains J_1,J_2,L_4,L_5. The direction is marked as red circle. Then the J_1 switches and generates large current. Current cross though resistance (R_{out}) and cross to the J_3. Once the current is beyond the critical current, the J_3 switches and propagate the pulse to next loop. The operation is same with SFQ. On the other hand, if AQFP signal which behaves logic "0" input on the opposite direction with red arrow, the J_1 will switch. Because the J_1 is far away from J_3, the generated current is consumed bu R_1 in advance. Therefore, the current can not propagate to J_3 and AQFP logic "0" can not transform to pulse signal.

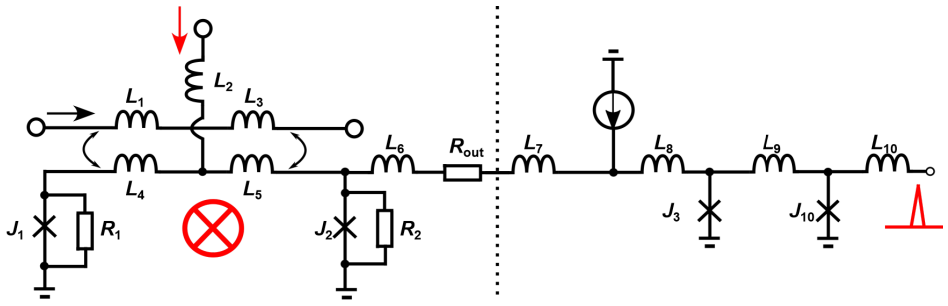


FIGURE 3.18: AQFP to SFQ Interface

Simulation

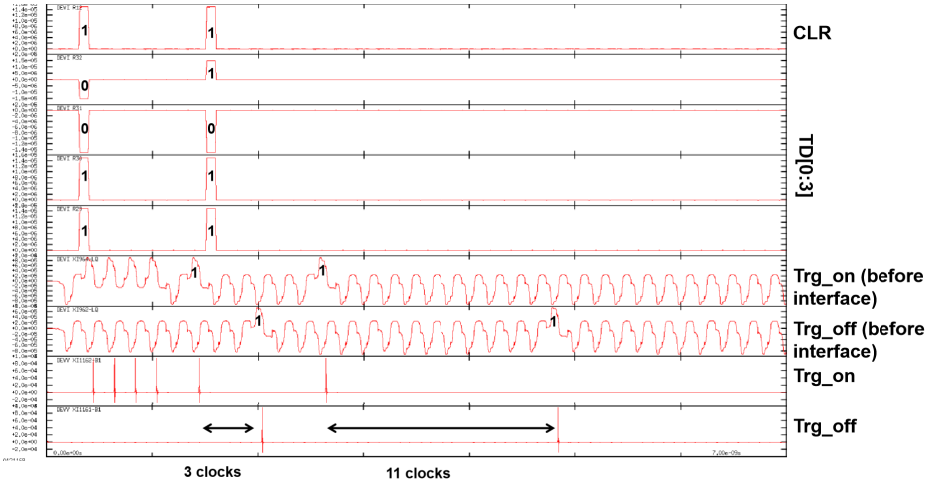


FIGURE 3.19: Simulation result of time controller

Here we do the simulation for the whole system. The result is presented at Fig.3.19. When CLR signal becomes logic "1", the TD[0:3] is input to system. For example, we input "0011" and "1011" as two examples. The decimal of "0011" and "1011" is "3" and "11". Output of Trg_on (before interface) is decided by CLR signal because it is propagated by buffer chain. It can be revealed that the latency of propagation is 4 clocks. Once it pass though the 3 clocks, the Trg_off signal generate logic “1”. Thus, the duration between them is 3clocks. We use this principle as well as input is "1011". Finally, the Interface is applied to transform the AQPF signal to pulse which can be observed by the difference with Trg_on (before interface) and Trg_off.

Chip Fabrication and Measurement result

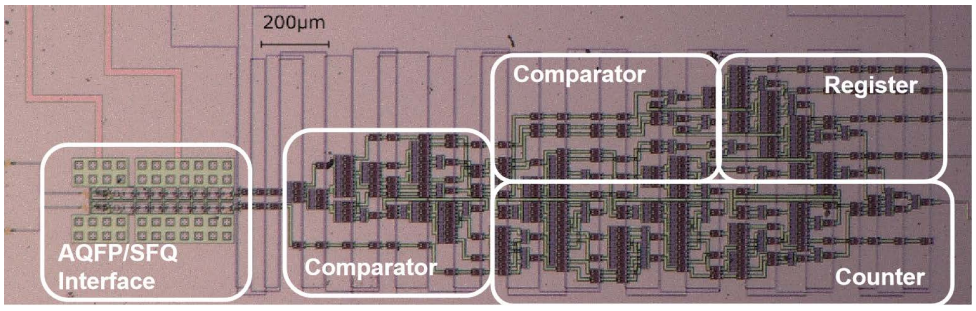


FIGURE 3.20: Photograph of Timing Controller

TABLE 3.1: Circuits Margin of Measurement

No.	Parameter name	Value
1	Chip Area (Counter)	1200 μ m $\times$ 380 μ m
2	Chip Area (Comparator)	1330 μ m $\times$ 380 μ m
3	Chip Area (Register)	600 μ m $\times$ 380 μ m
4	Chip Area (total)	2000 μ m $\times$ 730 μ m
5	Numbers of JJ	604

TABLE 3.2: Circuits Margin of Measurement

Bit Width	Chip Area	Junction Count	Power Consumption of AQFP (1GHz)
4 bit	$2000\mu m \times 730\mu m$	604	$1.25 \times 10^{-9} W$
8 bit	$3200\mu m \times 1050\mu m$	1004	$1.82 \times 10^{-9} W$
16 bit	$5600\mu m \times 1700\mu m$	1804	$2.39 \times 10^{-9} W$

The photograph of fabricated chip is presented in Fig.3.20. The chip is fabricated by process of AIST 10 kA/cm2 Nb high-speed standard process (HSTP)[37]. Chip parameter is presented as Tab.3.3. Besides, we evaluate the relationship of bit width and chip parameter. It is presented at Tab.3.2.

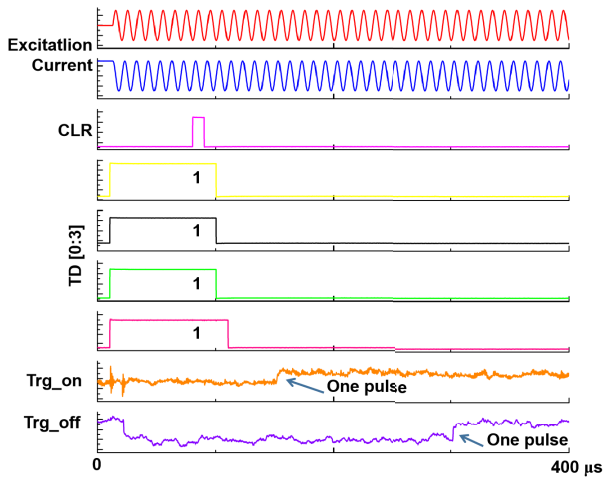


FIGURE 3.21: Measurement result with 100KHz excitation clock

Then we do the measurement result both under high speed and low speed. The low speed measurement result is presented at Fig.3.21. In this case we measure the 100 KHz excitation signal (red and blue). The phase difference of these two signal is 0.5 π. We set input to TD[0:3] "1111" When CLR signal is logic "1" for an example. The Trg_on signal (orange) shows a rising edge that after 5 clocks of CLR. Because we need SFQ to DC converter to confirm the pulse signal, the rising or falling edge of waveform reveals there is one pulse generated[40]. After 15 clocks of Trg_on, the Trg_off (purple) appears one pulse because of we input TD[0:3] as "1111".

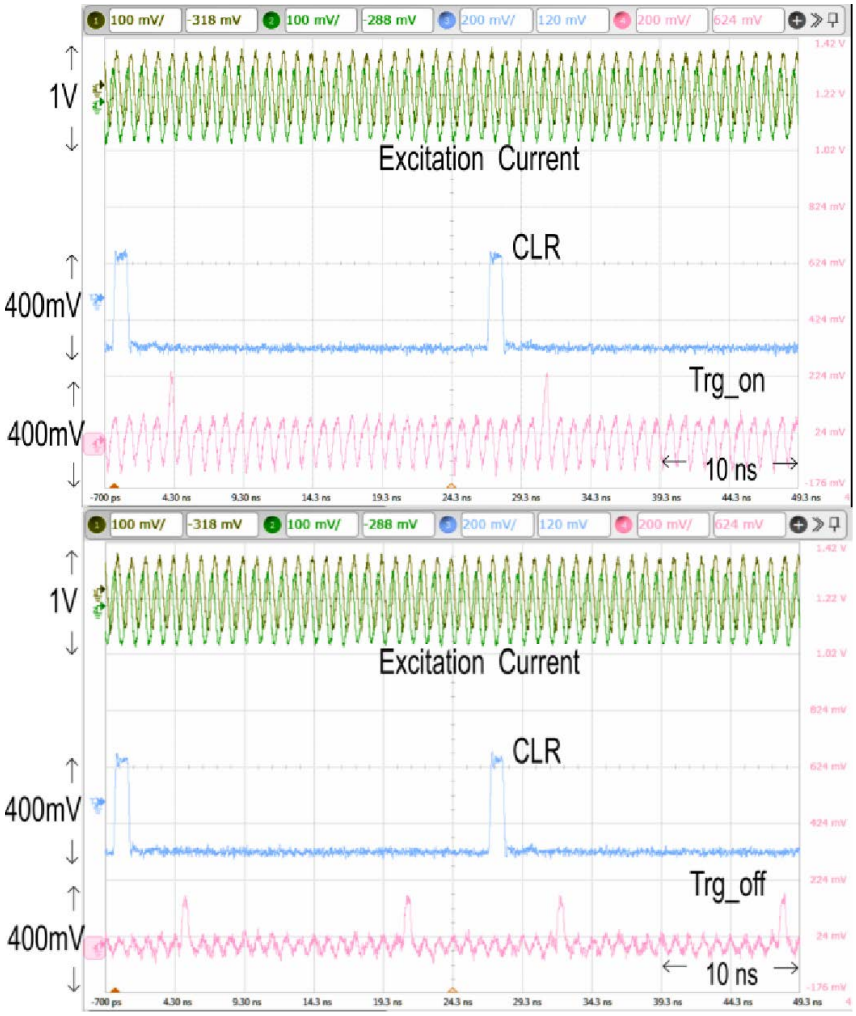


FIGURE 3.22: Measurement result with 1GHz excitation clock

Because our target maximum time interval is 200 ns, the necessary bit length for the counter is 8 bits, assuming with a 1 GHz excitation clock. To demonstrate a small prototype system, we reduced the bit length to 4 bits in the current design. Thus, we do the measurement with 1 GHz excitation clock. Due to confirming SFQ pulse needs a complex circuits, we just confirm the signal Trg_on and Trg_on before interface. The result is presented in Fig.3.22. In this example shows that we input TD as 0001, the duration between Trg_off and Trg_on arrives about 1 ns which is one clock time. During the CLR logic "1" signal, the duration of Trg_off is 16 ns because the counter is 4 bits. We measured the dependence of the time interval on the input data at 1 GHz operation and verified correct operation with a bit error rate less than 1%. The measured margin of the excitation current ranged from -30% to 28%. The relationship of duration time (ΔT) vs.input data TD is presented at Fig.3.23.

The duration time (ΔT) can be presented as follows:

$$\Delta T = TD \times T_{clock} \tag{3.17}$$

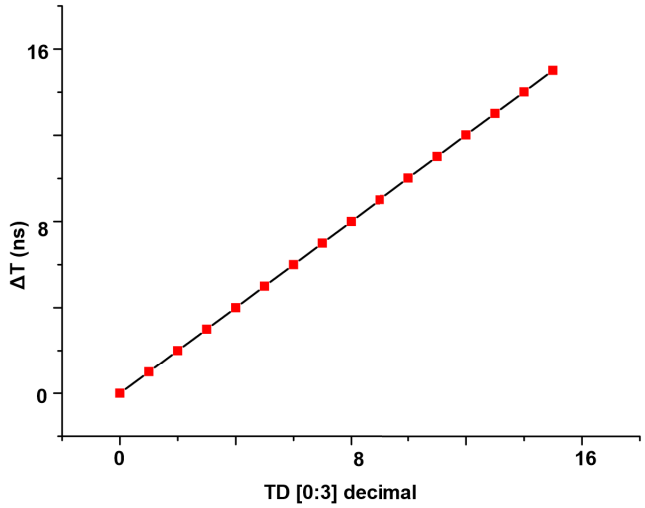


FIGURE 3.23: Measurement result with 1GHz excitation clock

3.3 8-bit Integrator Circuits Using AQFP

Nowadays the research of qubit readout system has been paid attention. People utilize the fact that the resonance frequency of the resonator changes according to the state of the qubit which is coupled to an oscillator[41]. This approach can achieve a high efficiency and nondestructive readout easily. To reduce the influence of thermal noise, people do some work on the low noise amplifier to increase the qubit output amplitude[42]. Some group including NEC release the out-coming result that the Josephson Parametric Amplifier (JPA) can be used in qubit readout circuits[43]. In general, the signal amplification factor of JPA increases with pump power, but there is a certain threshold for pump power determined by the lifetime of interactivity photons. That lads the phenomenon that JPA will oscillate and generate a signal at half pump frequency when the threshold is crossed. That is called Josephson Parametric Oscillator (JPO)[44].

Here, we will explain the principle of qubit readout system simply using Fig.3.24. In this use of the classical oscillator, it does not discriminate between the two different qubit states. On the ohther, it discriminates between energies of radiation emitted by a lossy resonator coupled to the qubit. So that it is possible to detect Rabi oscillation of a qubit. Assume the oscillation frequency of qubit is ω_o and it is coupled by a resonator which oscillation frequency is ω_r. The coupling strength (g) is much smaller than difference of ω_o and ω_r. The probe microwave make the LC resonator to oscillate. Once qubit oscillate with ω_o, it has a impact on LC resonator though the coupling. This influence will led the phase shift of LC resonator and the imagine figure is presented at bottom of fig.3.24. So once we can detect the phase of LC resonator, we can calculate the qubit state roughly. Now the JPO play the role of resonator by applied a pump signal.

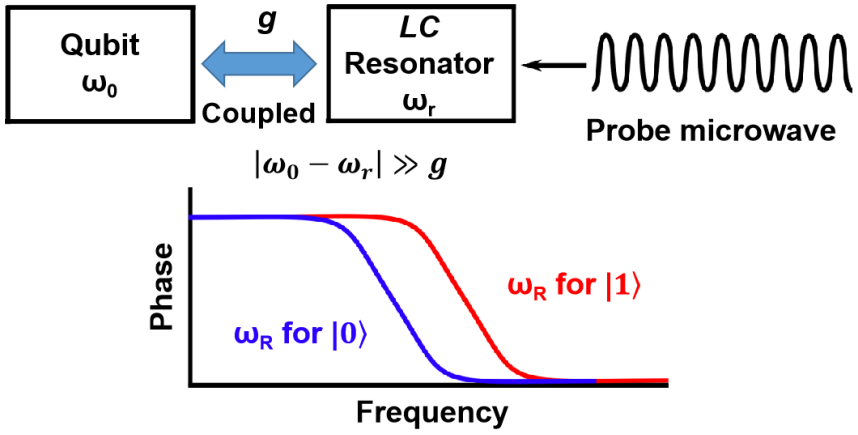


FIGURE 3.24: Qubit readout system

Due to qubit performs within several mk. The low power consumption readout system is required to avoid to influence qubit. Fortunately, AQFQ owns the advantage of low power consumption and it can detect the phase of microwave. The schematic is presented in Fig.3.25. The primary component of JPO is input coupling capacitance C_in, output coupling capacitance C_2, resonance capacitance C_1 and DC-SQUID termination. C_1 and DC-SQUID constitute the resonator. The magnetic flux is penetrated by

L_1 and L_2. Therefore, the boundary condition of resonator can be changed flexibly and hence us to control the resonant frequency. The frequency of input signal V_in is ω_0 and current I_ac provide $2\omega_0$ pump current to the JPA and cause the resonance. The output current in the resonance flows though L_3 and couple to L_4. L_4 connects to AQFP cell and output digital signal. We can detect the qubit oscillation phase matching to AQFP excitation signal.

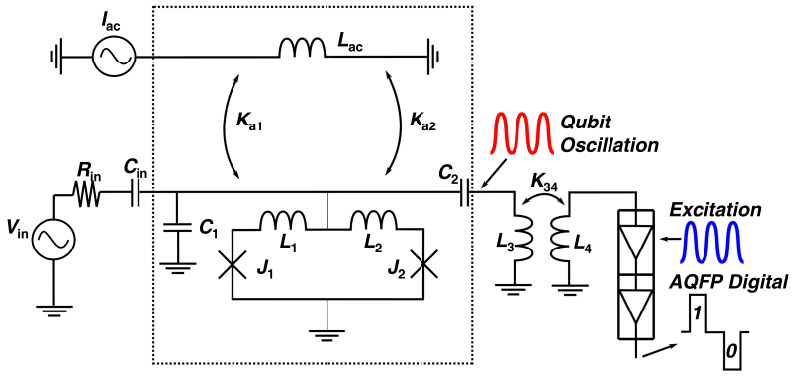


FIGURE 3.25: Schematic of JPO to AQFP

Input current grey zone of AQFP is parameter which shows the ability to resist noise. The narrower grey zone owns the better robust against the noise and better sensitive JPO readout system. Therefore, we will introduce digital process approach to reduce the grey zone of AQFP.

3.3.1 Grey Zone of AQFP

Here we want to introduce the grey zone of AQFP. Generally, output of AQFP should behave logic "1" when propagation current is positive (in Fig.3.1 from top to bottom) and should behave logic "0" when propagation current is negative (in Fig.3.1 from bottom to top). However,in physical layer, there is shunt resistance connect to junction. If we consider the influence on input current, current will vibrate as normal distribution which is presented in Fig.3.26. If we set the center current is 0 and the function of I with thermal noise can be given as follows:

$$f(I) = \frac{1}{\sqrt{2\pi\sigma^2}} exp(-\frac{I^2}{2\sigma^2}) \tag{3.18}$$

σ decide the width of $f(I)$. And we can calculate the probability of output is logic "1". Here, we calculate the shadow area as presented in fig.3.27. The area can be presented as follows:

$$\begin{aligned} P(I) &= \int_0^{+\infty} \frac{1}{\sqrt{2\pi\sigma^2}} exp(-\frac{I^2}{2\sigma^2})\, dI \\ &= 0.5 + \int_0^{I_{in}} \frac{1}{\sqrt{2\pi\sigma^2}} exp(-\frac{I^2}{2\sigma^2})\, dI \end{aligned} \tag{3.19}$$

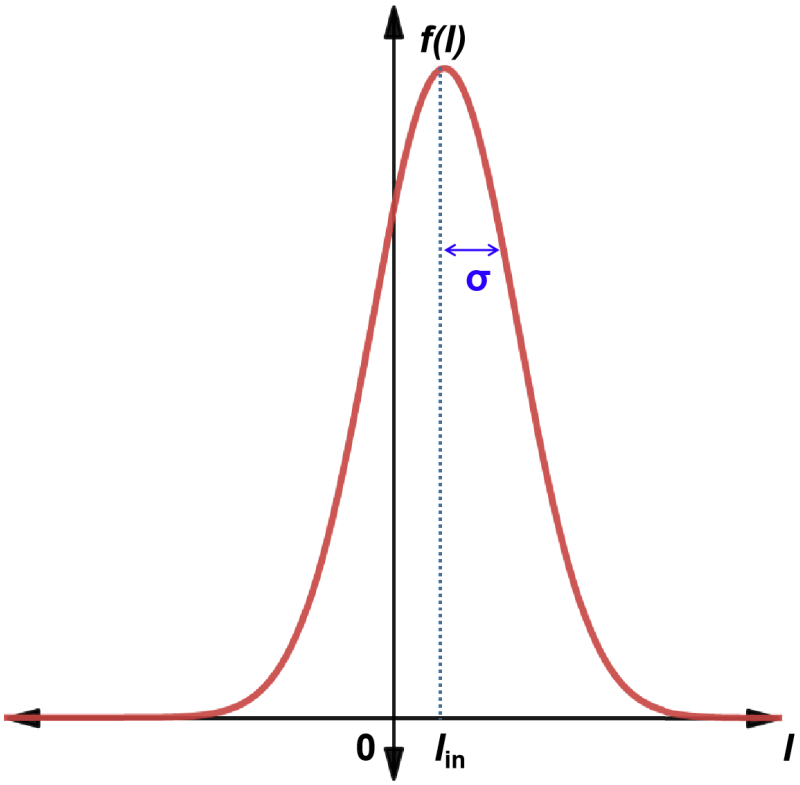


FIGURE 3.26: Distribution of input current considering fluctuations of thermal noise

The we derivative the $P(I)$, we can get as follows:

$$P'(I) = \frac{1}{\sqrt{2\pi\sigma^2}} exp(-\frac{I^2}{2\sigma^2}) \tag{3.20}$$

The width of grey zone can be defined that the slope of reciprocal of tangent when probability $P(I) = 0.5$. It is obvious that $P(I) = 0.5$ when current $I = 0$. Thus, width of grey zone (ΔI) can be given as follows:

$$P'(0) = \frac{1}{\sqrt{2\pi\sigma^2}} = \frac{1}{\Delta I} \tag{3.21}$$

Then we will give the error function that we set the $I = \sqrt{2}\sigma t$, the formula $P(I)$ can be presented as follows:

$$P(I) = 0.5 + 0.5 \times \frac{2}{\sqrt{\pi}} \int_0^{\frac{I_{in}}{\sqrt{2}\sigma}} exp(-t^2)\, dt \tag{3.22}$$

The error function is as follows:

$$erf(x) = \frac{2}{\sqrt{\pi}} \int_0^{\frac{I_{in}}{\sqrt{2}\sigma}} exp(-t^2)\, dt \tag{3.23}$$

And

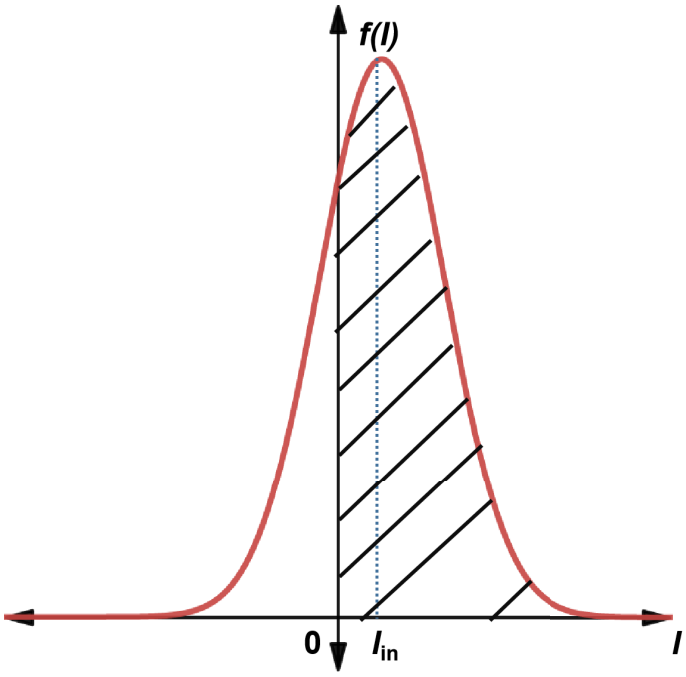


FIGURE 3.27: Shadow Area Perform Logic state "1"

$$P(I) = 0.5 + 0.5erf(\sqrt{\pi}\frac{I}{\Delta I}) \tag{3.24}$$

We can describe the probability of logic "1" using error function. And we present the Imagine figure in fig.3.28 The smaller width grey zone, the higher resolution of one AQFP cell. It can be applied to detect the massage. And vice, the wide grey zone of AQFQ can be used as random number generator.

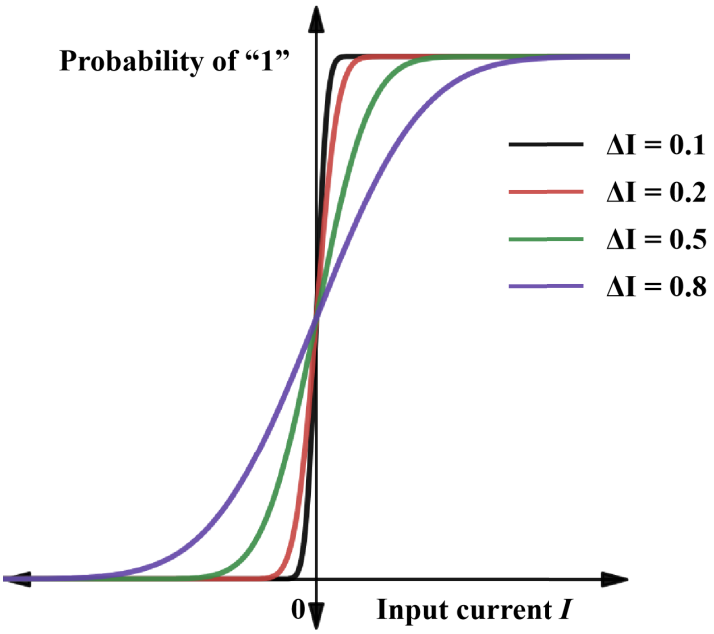


FIGURE 3.28: Output probability P of logic state "1" by I

3.3.2 Integration Theory

As mentioned, we suggest that using AQFP circuits to detect qubit signal phase. AQFP buffer chain sensitive is decided by grey zone of single buffer directly. Compare to improving buffer on physical layer, applying digital method to enhance sensitive will be much easier. Thus, we design the integrator using AQFP circuits to output majority of input data.

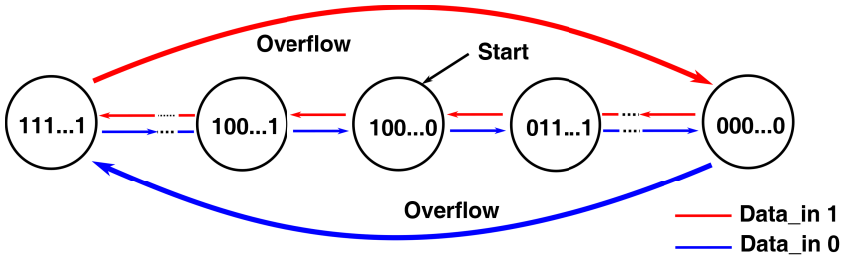


FIGURE 3.29: Principle of integrator

he operation principle is presented as fig. 3.29. At first, we reset the system code to 100...0. Then code will increase or decrease according to input data as figure shows. System should be reset if overflow situation occurs. The most significant bit (MSB) of system code reveals the integral result directly which also means the majority result.

It is obvious that integral data numbers will influence grey zone. Assume that the grey zone of single buffer is ΔI which is given in formula 2-1 (P is possibility of '1' and I is input current). When we input m numbers of data to buffer chain. Grey zone of Buffer chain system is still p because of independence of each data. When we input

m numbers of data into integrator, the situation will become complex because of non-independence of each data. Possibility of "1" occurs on first data is $P(D1)$ is given in (3.25). P(D2) is given in (3.26) and possibility of total m numbers of data is given in (3.27). To calculate the grey zone, it is necessary to do differential calculus to formula (3.28) and result is given as formula (3.29). Thus the relationship of grey zone and integral number can be presented in Fig.3.30. It is obvious that more integral data the narrower AQFP grey zone

$$P'(I)|_{I=0} = P' = \frac{1}{\sqrt{2\pi\sigma^2}} = \frac{1}{\Delta I} \tag{3.25}$$

$$P(D_1) = P \tag{3.26}$$

$$P(D_2) = P^2 + P(1-P) \tag{3.27}$$

$$P_{int}(I) = \frac{1}{M}\sum_{k=1}^{M} P(D_M) \tag{3.28}$$

$$P'_{int}(I) = \frac{1}{2M\Delta I}\sum_{k=1}^{M}\left(\binom{M}{[(M+1)/2]}\frac{M+1}{2^M}\right) \tag{3.29}$$

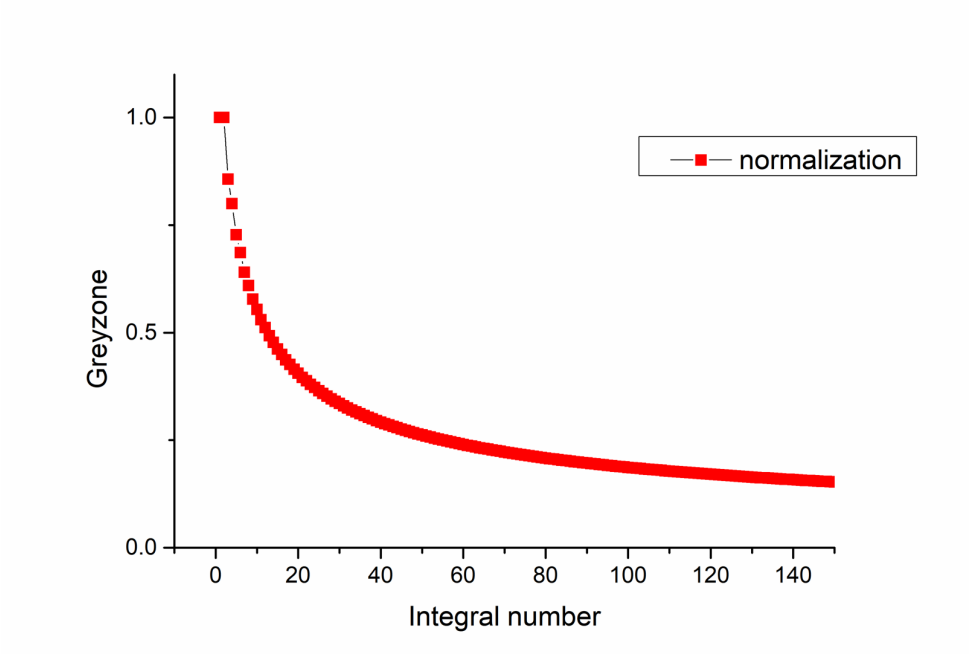


FIGURE 3.30: Theoretical value of Grey zone vs. intergal number

3.3.3 AQFP Integrator Circuits

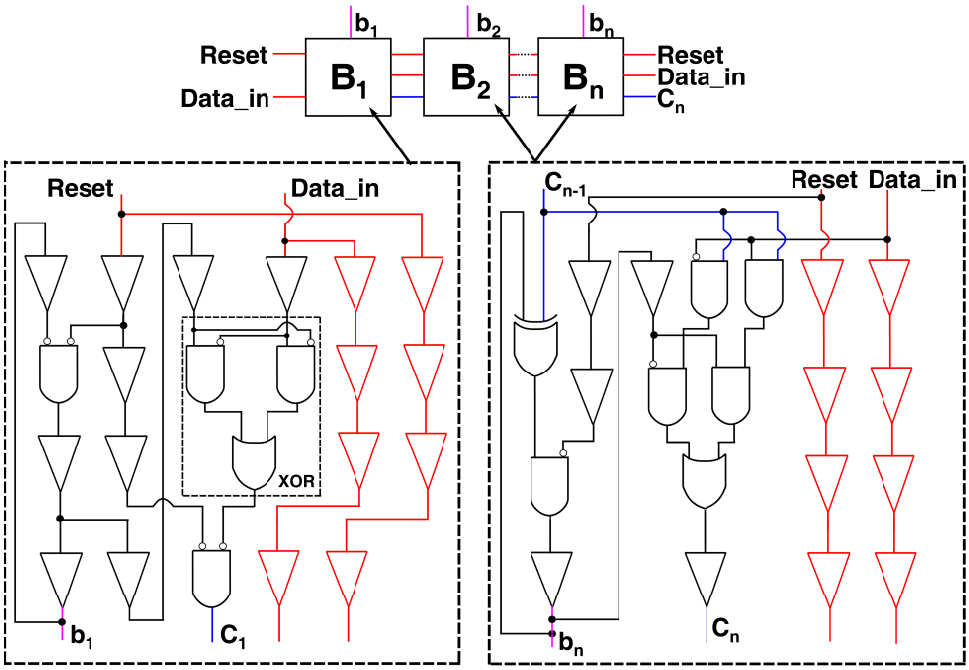


FIGURE 3.31: Integrator system designed with AQFP

Fig. 3.31 illustrates the structure of n-bits AQFP integrator system. The system consists of n blocks where each block process 1 bit data. The first block ($B1$) needs 2 input to accomplish the function. The formula is given as flows:

$$b_1' = \overline{b_1} \times Reset \tag{3.30}$$

$$C_1 = \overline{(Data\_in \bigoplus b_1)} \times Reset \tag{3.31}$$

Here the b_1' is next state of b1. Due to there is no basic logic gate in AQFP, we need to establish XOR gate (dot square) which will be used in other blocks. There are 4 outputs of this block, bit data (b_1), carry bit (C_1), reset and $data\_in$. C_1, reset and $data\_in$ will be used in subsequent block (B_2) for calculation. The rest of block (B_2 B_3 ...to B_n) is the same structure. The formula of this blocks is given as flow:

$$b_n' = (Data\_in \bigoplus C_{n-1}) \times Reset \tag{3.32}$$

$$C_n = \overline{Data\_in} \times C_{n-1} \times \overline{Reset} + Data\_in \times C_{n-1} \times Reset \tag{3.33}$$

The system state consists with ($b_n b_{n-1} \ldots b_2 b1$). The C_n shows the situation whether an arithmetic carry or borrow has been generated out of the (MSB) logic unit. Thus, it can be monitored system code overflow. Here we need Reset and $Data\_in$ signal run though all blocks for calculation using build-in buffer chain (red line). On the other hand, we can not only obtain the grey zone of AQFQ buffer ($Data\_in$), but also the grey-zone integral result (b_n).

TABLE 3.3: Circuits Margin of Measurement

Parameter name	**2 bit**	**4 bit**	**8 bit**
Chip Area (μ m $\times$ μ m)	600 $\times$ 1000	600 $\times$ 1800	600 $\times$ 3200
Numbers of JJ	240	450	782
Excitation Margin (Measurement)	[-33.4%, 32%]	[-32%, 32%]	[-31.8%, 32%]
Power Consumption ($\times 10^{-9} W$)@ 5GHz	0.236	0.84	1.96

3.3.4 Chip Fabrication and Measurement Result

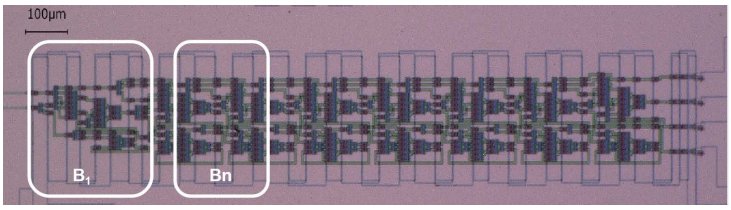


FIGURE 3.32: Photograph of 8 bit integrator

Here, we give the photograph of 8 bits integrator in Fig.3.32. Each block is designed as same width for increasing the extra blocks. It is meaningless to observe all of system state bits expect b_n. To save the chip area we just observe 4 outputs. To confirm the function, we fabricate a 2 bit integrator which only hold the block B_1 and B_n. The measurement of 2 bit integrator result is presented in fig.. In this experiment, we apply 100 kHz excitation signal. To observe the system inside data, there is one clock latency appear on MSB (limited by feed back line length so we add one more 4 phase to observe it). As the fig.3.33 shows, the code with same color constitutes a pair. When the Reset becomes logic 1, state (B_2B_1) is set to 10. We confirm the operation is as Fig 2 present. The overflow occurs when state changes from 00 to 11 or from 11 to 00. At this moment, the C_2 will turn logic 1 to show this situation.

We list a table to present the chip parameter estimate the power consumption[1]. Because the block width is almost the same, so with the increasing of blocks, the chip just becomes longer. We do the measurement of 3 different bits integrator with 100 kHz excitation signal. The margin almost the same which is about 30%. The numbers of JJs almost multiple increase with bit numbers. The power consumption is simulated by JSIM which excitation signal is about 5 GHz.

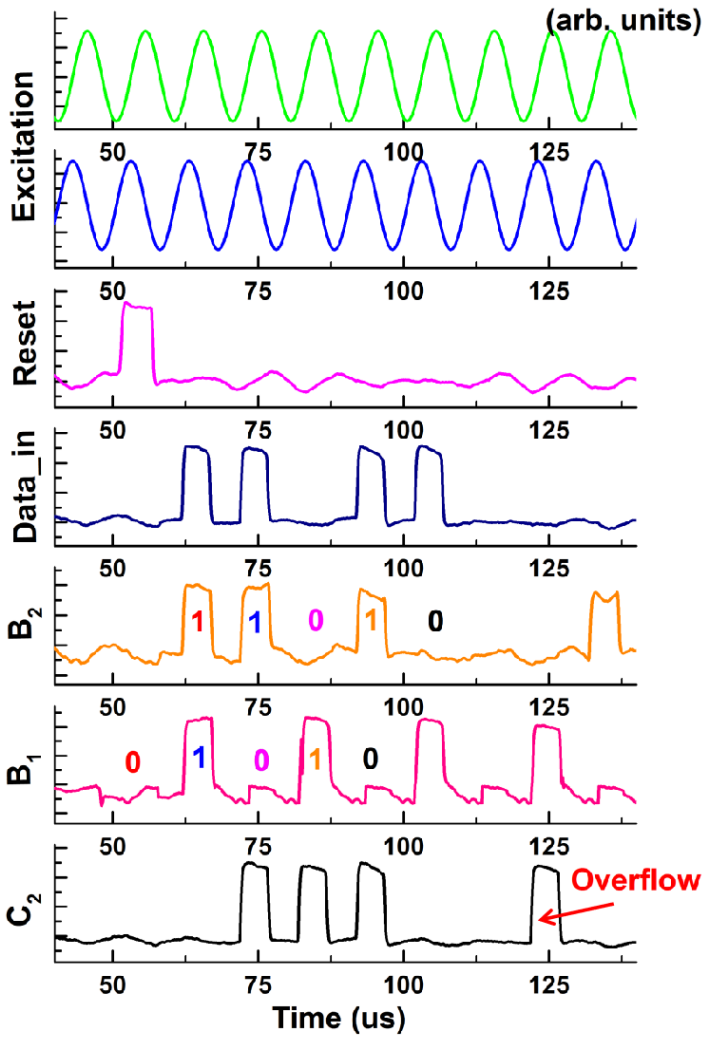


FIGURE 3.33: Measurement result of 2 bit integrator

Besides, we do the experiment to calculate the grey zone of system. We reset the system every few clocks to avoid the overflow. During the time we change the different dc signal to *data_in*. Then we count the numbers of logic 1 and calculate the probability. The result is presented fig.3.34 (a). In this graph we list 4 examples of integral numbers of data. The change tendency of curve will become stepper when we integrate more data. When input current is about -0.9 uA, the probability is about 50%. That is because parameter of fabricated AQFP cell exist deviation. Fig.3.34 (b) reveals the relationship between integral numbers and grey zone. It shows that value of grey zone become smaller when we integrate more data. The curve tendency conforms to the theoretical expectation.

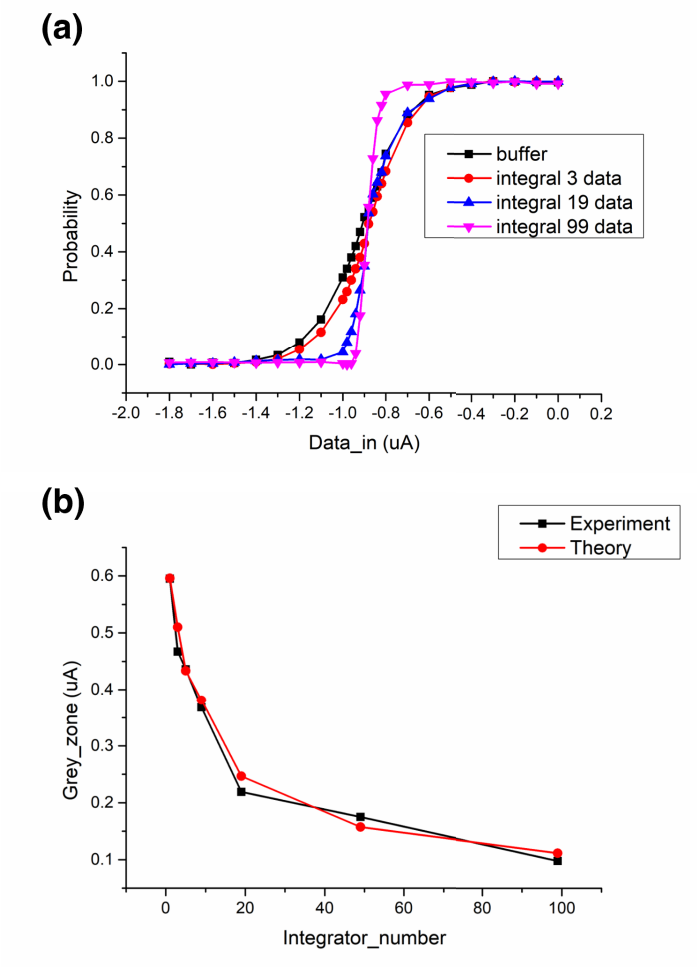


FIGURE 3.34: Grey zone vs. integral numbers

3.4 Conclusion

In this section we introduce the designed circuits which uses AQFP cell. AQFP owns the lower power consumption compared with SFQ circuits which reveals the potential to instead SFQ circuits to control qubit. The timing controller circuit is applied to microwave generator and we confirmed the operation with measurement. To read out the state of qubit, the JPO is required and the phase should be detected. Thus, we designed the integrator using AQFP for improving sensitive of detecting phase. We test the circuits with 2bits,4bits and 8bits. It is obvious the the more number of bits can contain more input data. On the base that AQFP can detect microwave phase, we expect to apply the integrator on the JPO.

Although the duration can be controlled by AQFP, it is also hard to design a kind of superconducting circuit for adjusting duration of pair pulses. The strong and stable current is required as control current in fig.2.19. Therefor, we pay attention on Cryo-CMOS circuits as control current and it will be introduced in next chapter.

Chapter 4

Arbitrary Envelope Signal Generator Using Cryo-CMOS

As mentioned in chapter2, we designed the microwave generator and confirm the function within cryogenic temperature. The microwave amplitude is changeable according to control current. Thus, we can change the variation trend of control current to modulate microwave. However, we evaluate the value of control current and several milliampere is required in microwave generator. What's more, the control current should be stable. Fortunately, there is a technique to support this function, Cryogenic-CMOS. Firstly, the current which is generated by Cryogenic-CMOS is much stabler than superconducting circuits. Secondly, it can perform at least of 1 GHz operation speed within cryogenic temperature. The decoherence time of transform qubit is more than 20 μs. We can generate thousands of operations with cryogenic-CMOS before the decoherence time. Thirdly, we can put the CMOS circuits far away from quantum process to avoid the impact of thermal noise on quantum process.

4.1 Device of NMOS and PMOS

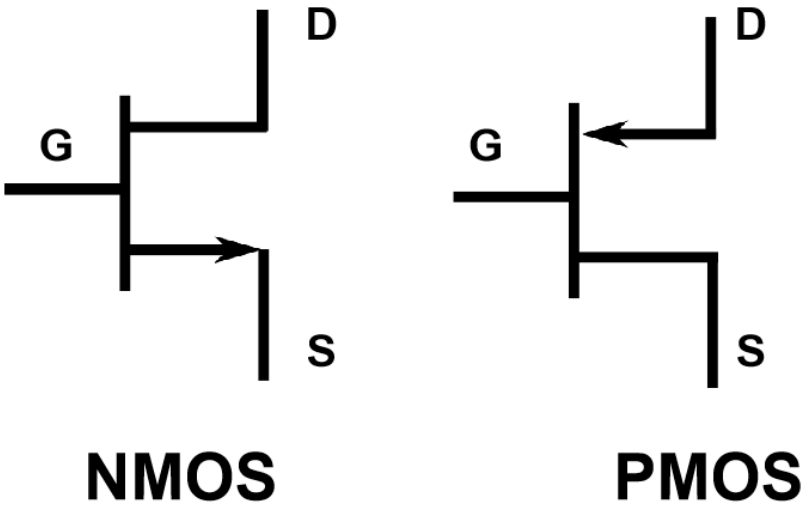


FIGURE 4.1: Model of CMOS

Here we give the the model of CMOS in Fig.4.1. Both of them contains the gate (G),source (S) and drain (D). The current can be gives as follows:

$$I_D = \begin{cases} \beta((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}) & \text{if } V_{GS} - V_{TH} < V_{DS} \\ \frac{\beta}{2}(V_{GS} - V_{TH})^2 & \text{if } V_{GS} - V_{TH} \geq V_{DS} \end{cases} \tag{4.1}$$

Here, β is presented as (4.2). The μ is electronic mobility, C_{ox} is capacitance which is mainly decided by device process. W is the width and L is length of of transistor. We give the simulation result of I-V characteristic.

$$\beta = \mu C_{ox} \frac{W}{L} \tag{4.2}$$

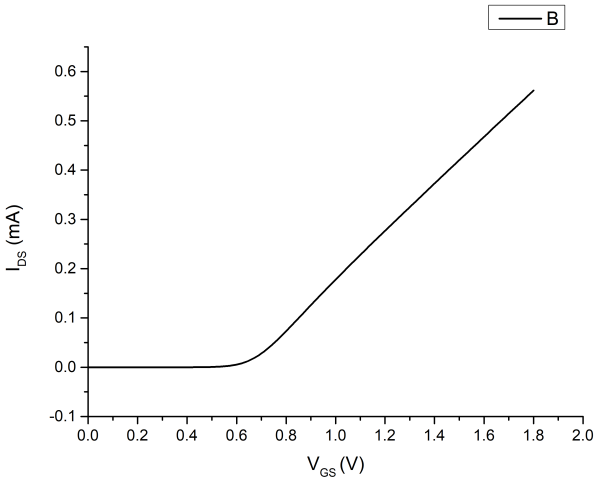


FIGURE 4.2: I-V characteristic

Here, we give the I-V characteristic of NMOS in fig.4.2. The V_{TH} is about 0.65 V of NMOS. Due the V_{DS} is 1.8 V, the NMOS keep in the linear region. The slope of curve can reveal the parameter β.

The I-V characteristic about V_GS is presented in fig.4.2. The saturation region of NMOS can be observed obviously. However, the current will not keep as a constant because of channel length modulation. It is caused when V_DS continuous to increase, the effective channel length decreases instead. Generally,this phenomenon is quite obvious if the L of device is smaller. The function can be written as follows:

$$I_D = \frac{\beta}{2}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{4.3}$$

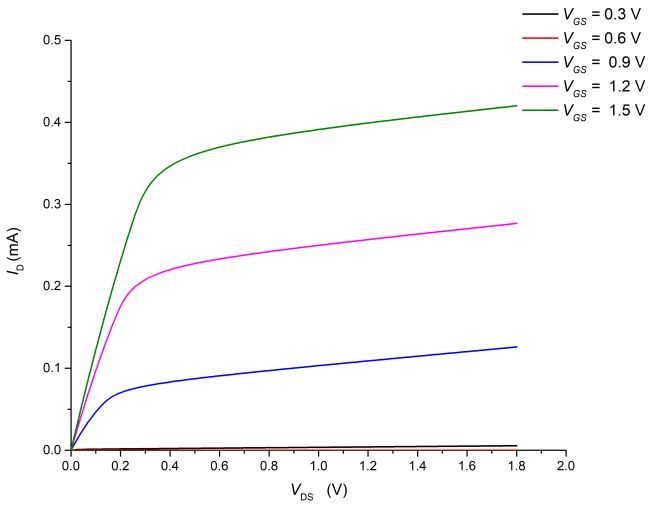


FIGURE 4.3: I-V characteristic

4.1.1 Digital Cell Designed Using CMOS

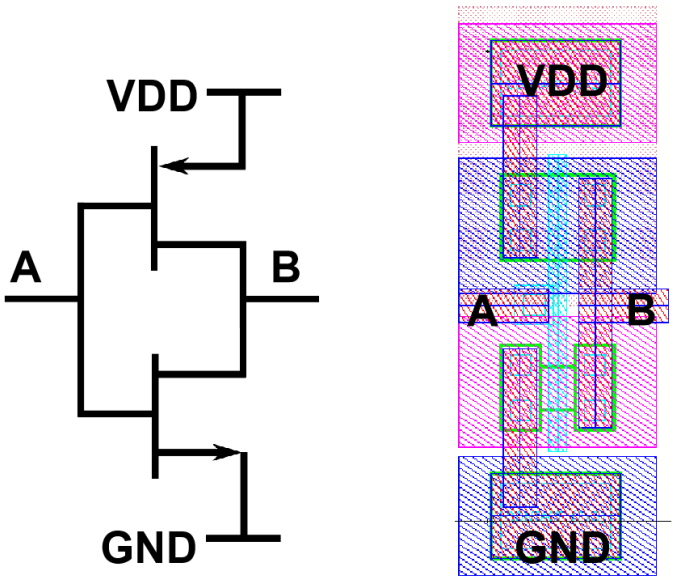


FIGURE 4.4: Schematic and layout of of Inverter

Here, we will introduce some sample examples that the digital cell designed by CMOS. Fig.4.4 present the symbol and layout figure. Generally, we set the voltage (VDD) to logic "1" and GND to logic "0". When voltage (A) is logic "1", the PMOS will close and NMOS will open. Thus, the voltage (B) is close to GND and become logic "0". We use this characteristic to reverse the logic. Formula is presented as follows:

$$B = \overline{A} \tag{4.4}$$

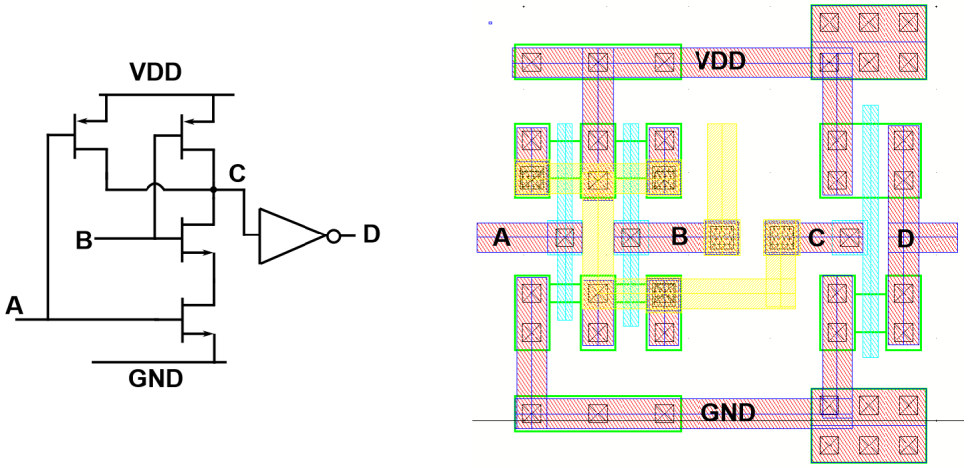


FIGURE 4.5: Schematic and layout of of AND GATE

Here, we present AND gate in fig.4.5.Only when input A and B is logic "1", The NMOS open and output C is nearly close to ground. Either A or B has to be logic "0", the PMOS will open and C is nearly close to VDD. Then we reverse logic C to D. The formulation can be presented as follows:

$$D = \overline{C} = A + B \tag{4.5}$$

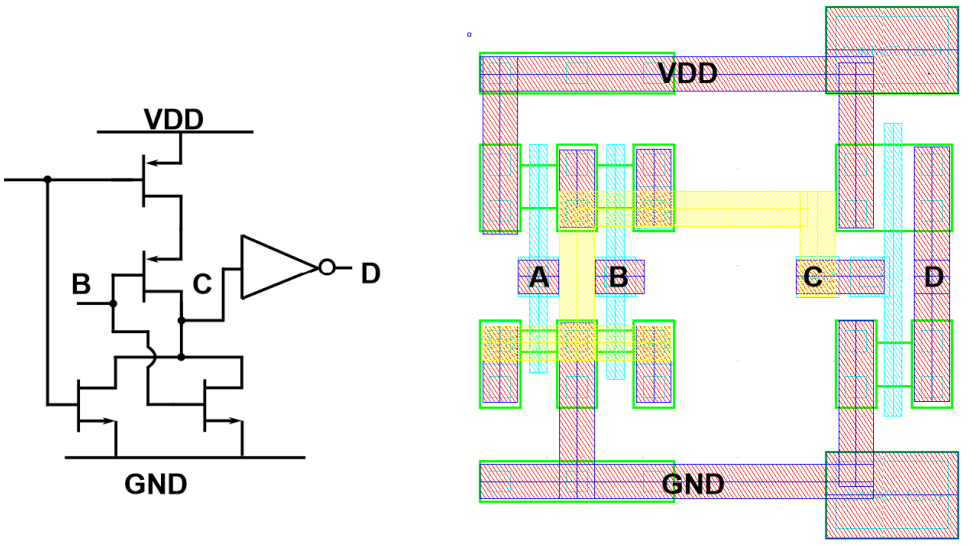


FIGURE 4.6: Schematic and layout of of OR GATE

Here, we present OR gate in fig.4.6.Only when input A and B is logic "0", The PMOS open and output C is nearly close to VDD. Either A or B has to be logic "1", the NMOS will open and C is nearly close to GND. Then we reverse logic C to D. The formulation can be presented as follows:

$$D = \overline{C} = A \times B \tag{4.6}$$

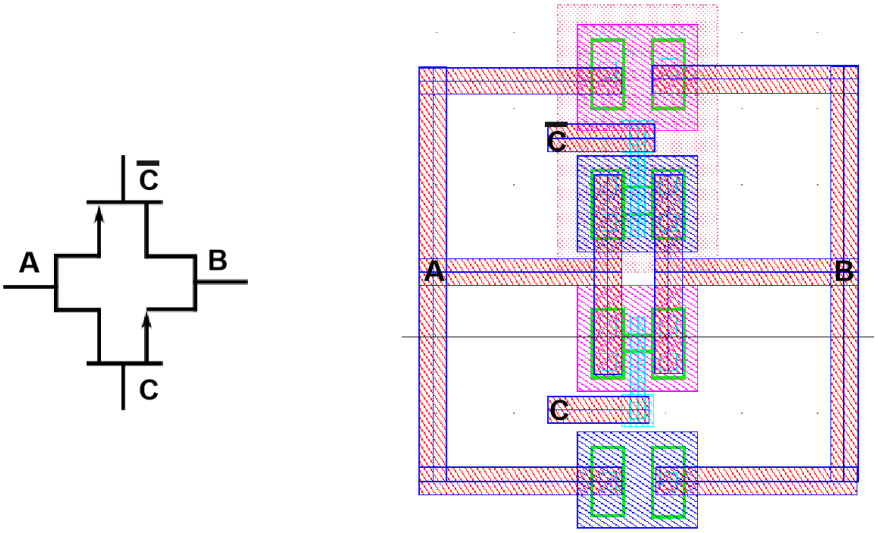


FIGURE 4.7: Schematic and layout of of Transmission GATE

Here, we present transmission gate in fig.4.7. We use NMOS and PMOS to consist this cell. When One of the transistor is on state, the other will keep on. If one transistor of them becomes smaller by input signal, another will be bigger. That is the reason why transmission gate can be seen as a stable resistance.

The formulation can be presented as follows:

$$A = B, \text{ when } C \text{ is logic 1} \tag{4.7}$$

4.1.2 D Filp-Flop

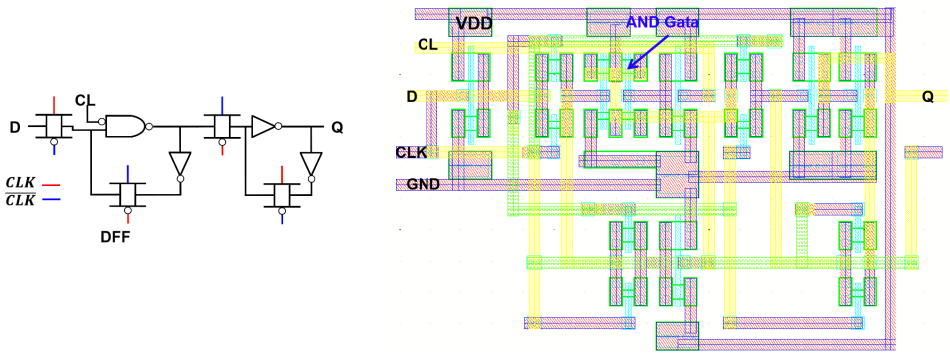


FIGURE 4.8: Schematic and layout of of DFF

Here, we present the schematic and layout of D filp-flop (DFF). The structure is master-salve type. Once the clock signal (CLK) is logic "1", the DFF will record the data D. Then clock turns logic "0", the data is stored in the loop and keep output. The reset function (CL) is added to control DFF state. Reset function can be achieved by many methods.We can reset the state as logic "1" shown in fig.4.8 and reset the state as logic "0" shown in fig.4.9.

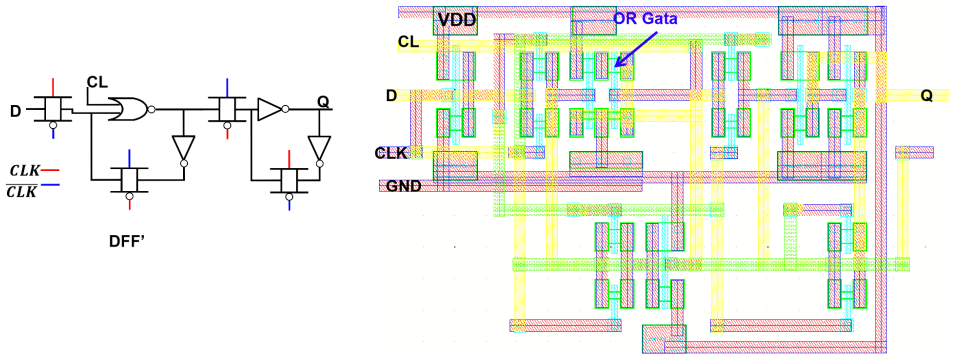


FIGURE 4.9: Schematic and layout of of DFF'

The simulation result is presented in fig.4.10. When Clock (CLK) Turns to "0", output of DFF and DFF's is the last record data (D). When reset signal is logic "1", the DFF is reset to "0" and DFF's is reset to "1".

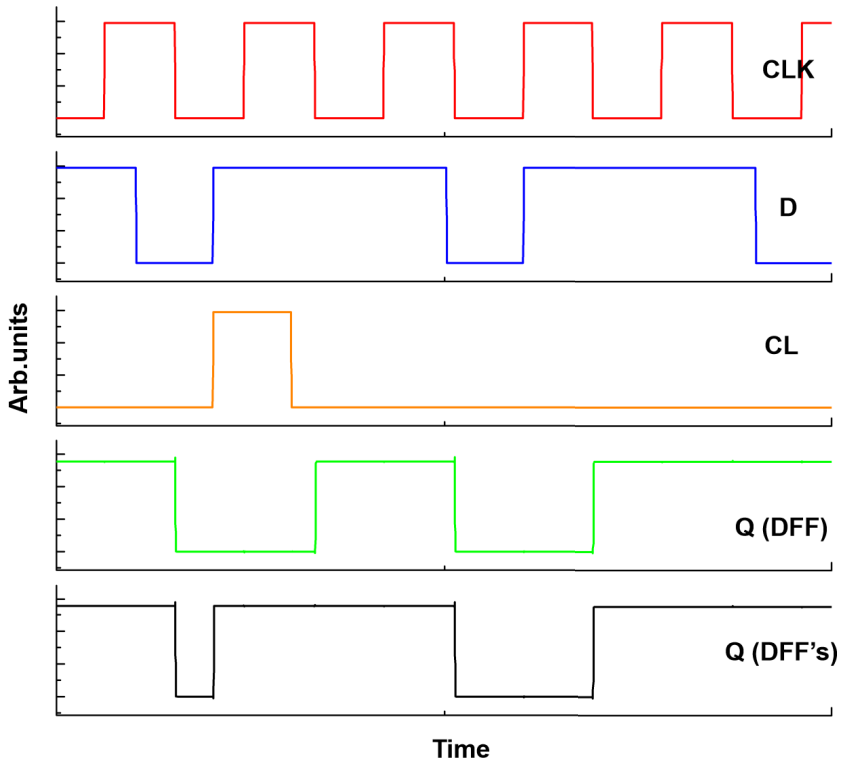


FIGURE 4.10: Simulation result of DFF and DFF's @ 1GHz

4.1.3 Digital to Analog Converter

Theory

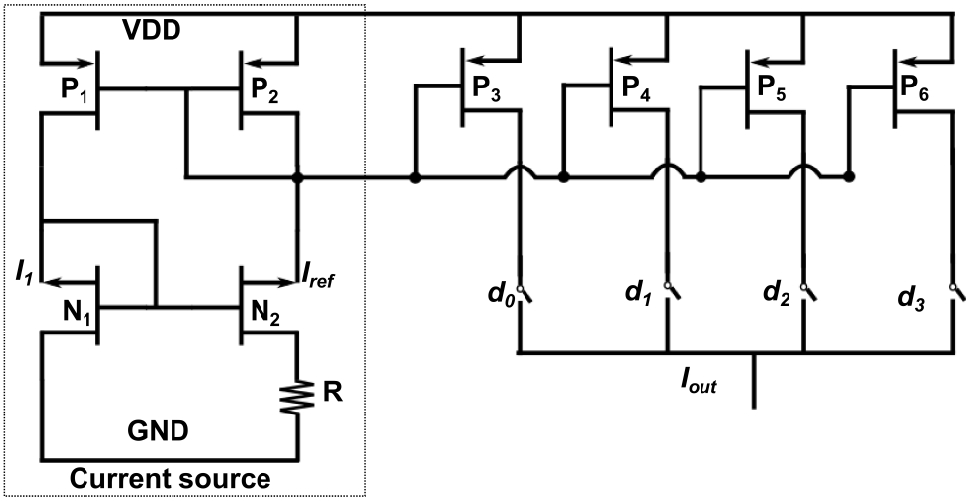


FIGURE 4.11: Schematic of 4-bit DAC

To generate the arbitrary envelope signal, the Digital to Analog Converter (DAC) is required to output the current signal. Here, we present the structure of 4 bit DAC in fig.4.11. It contains the current source and control parts. The current source is applied to provide the stable bias voltage to P_3,P_4,P_5 and P_6. Because the P_1 and P_2 use the same bias voltage, the current cross the transistor is the same.

$$I_1 = I_{ref} \tag{4.8}$$

Then we consider the V_{GS} of N_1 and N_2.

$$V_{GSN1} = V_{GSN2} + I_{ref}R \tag{4.9}$$

Assume the width of N_2 is K times of N_1. According the function (4.1), the formula can be presented as follows:

$$\sqrt{\frac{2I_1}{\beta(W/L)}} = \sqrt{\frac{2I_1}{\beta K(W/L)}} + I_{ref}R \tag{4.10}$$

Then the reference current I_{ref} can be presented as follows:

$$I_{ref} = \frac{2}{\beta(W/L)}\frac{1}{R}(1 - \frac{1}{\sqrt{K}})^2 \tag{4.11}$$

The formula reveals that the reference current $Iref$ is inverse ratio of R. Larger K will led to larger current, which required larger width W to keep balance. Thus, we take K to 2. The simulation result is present in fig.4.12. Variation trend is match the expectation.

The structure of DAC is used mirror current so that the current cross the PMOS can be presented as follows:

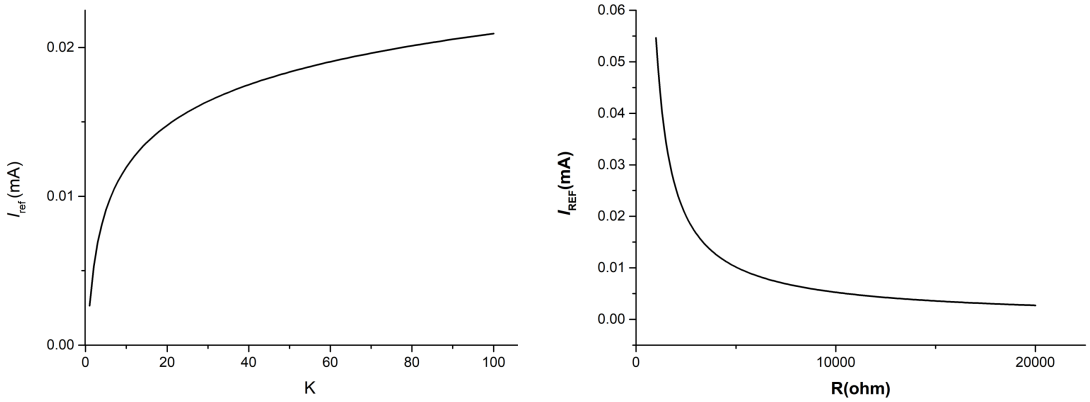


FIGURE 4.12: Relationship vs. K and R

$$I_{ref} = \beta \frac{W_{P2}}{2L_{P2}} (V_{GSP2} - V_{TH})^2 \tag{4.12}$$

$$I_{P3} = \beta \frac{W_{P3}}{2L_{P3}} (V_{GSP3} - V_{TH})^2 = \frac{W_{P2} L_{P3}}{W_{P3} L_{P2}} I_{ref} \tag{4.13}$$

Generally, we set the length of transistor (L) to the minimum to achieve the largest operation speed. Therefore, the current can be copy to the other transistors which are applied the same bias voltage. If we set the width as follows:

$$W_{P6} = 2 \times W_{P5} = 4 \times W_{P4} = 8 \times W_{P3} \tag{4.14}$$

The output current can be given as follows:

$$I_{out} = d_0 \times I_{out} + d_1 \times 2I_{out} + d_2 \times 4I_{out} + d_3 \times 8I_{out} \tag{4.15}$$

The d_0,d_1,d_2 and d_3 is the logic signal to control the switch on and off.

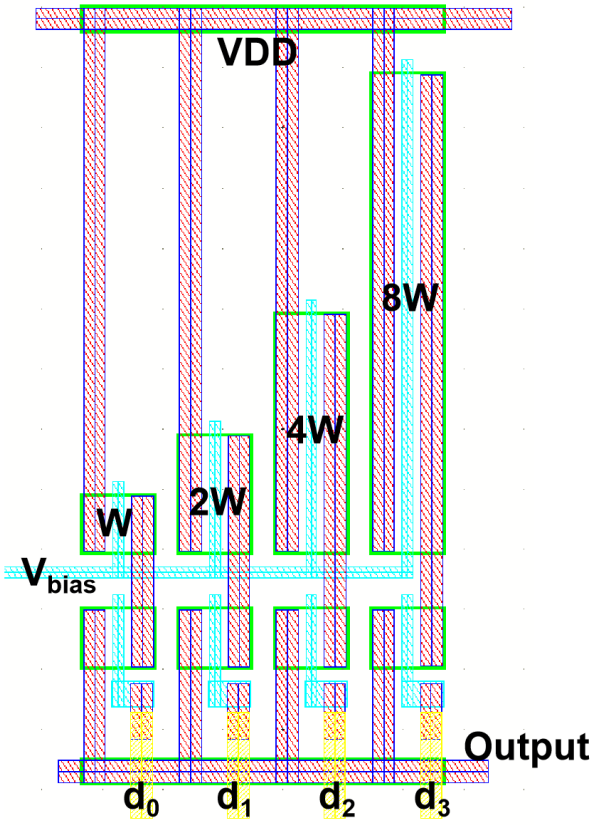


FIGURE 4.13: Version 1 of Layout of 4-bit DAC

The layout is presented in fig.4.13. However, this design will cause the parameter different on PMOS easily such as different resistances connects to PMOS. To avoid the linearity worse, we improve the layout and is given in fig .4.14. This design applies the the multiple method where it connect the M same transistor in parallel.

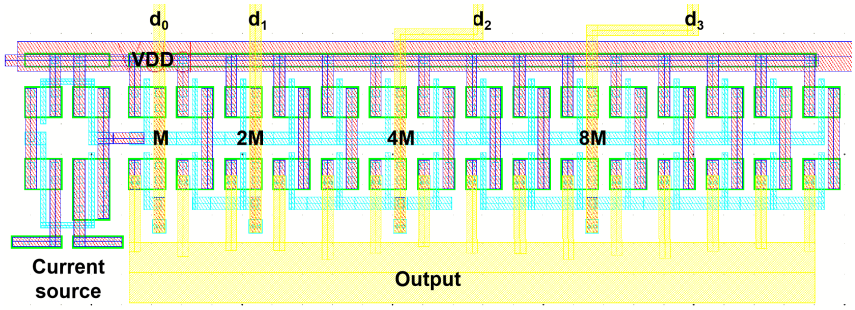


FIGURE 4.14: Version 2 of Layout of 4-bit DAC

Measurement

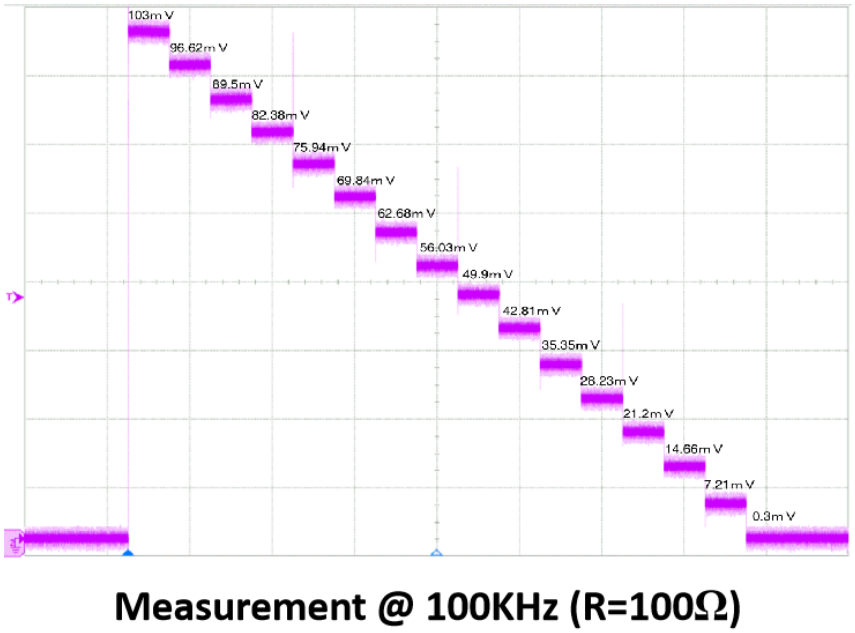


FIGURE 4.15: Measurement of 4-bit DAC @ 100 kHz

Here we give the measurement result of 4 bit DAC when clock is 100kHz. The resistance is used 100 Ω. In this experiment, the maximum value is 103 mV and the LSB is about 6.9 mV where load resistance is 50 Ω. We can calculate the differential nonlinearity (DNL) is about 0.1 LSB by using formula as follows:

$$DNL = \left| \frac{V_{D+1} - V_D}{V_{LSB} - V_{ideal}} - 1 \right| \tag{4.16}$$

We present the relationship of output voltage vs.input data. It behaves the linearity both of simulation and measurement. The measurement value is larger than simulation. On the other hand, we present the relationship of output voltage vs.connect voltage. It is match to expectation which is in fig.4.12.

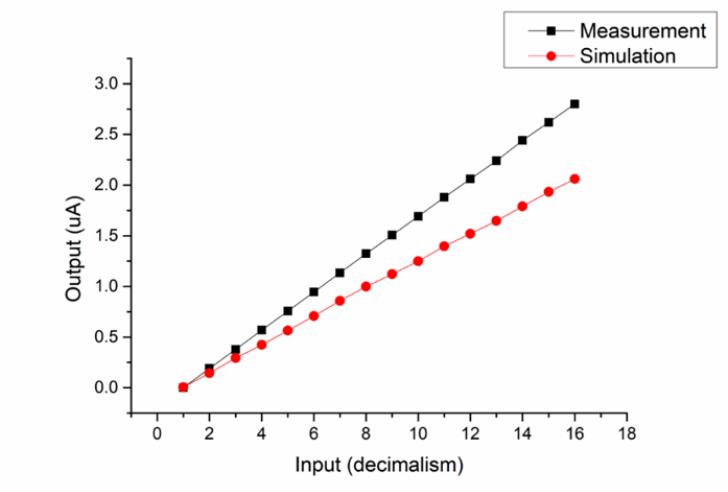


FIGURE 4.16: Measurement of 4-bit DAC @ 100 kHz

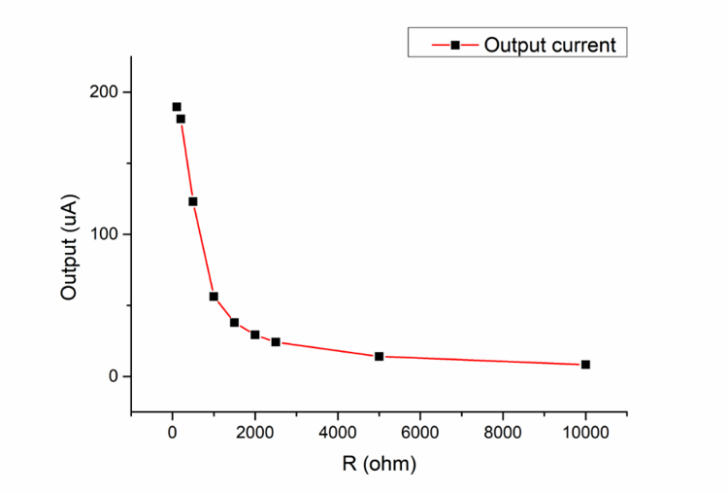


FIGURE 4.17: Measurement of 4-bit DAC @ 100 kHz

4.2 Arbitrary Envelope Signal Generator

4.2.1 Structure of System

Here, we present the system contains 8 DAC arrays and Control system which is applied to switch array. Bit line (BL) is used to control the DAC and output required current, here is 4 bit to control DAC. Confluence current will generate a signal which looks like a "pyramid". This current is smoothed though low pass filter and output required current. it reveals the potential of real time calibration according requirement because data in BL can be changed easily.

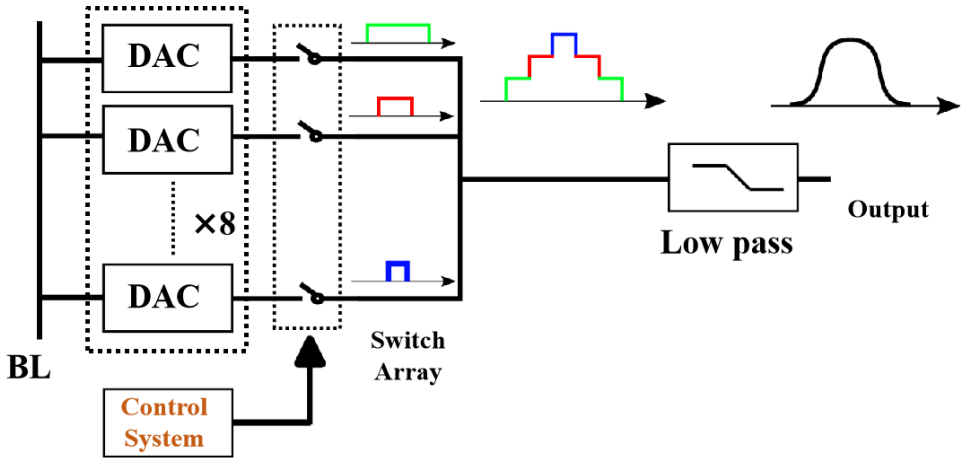


FIGURE 4.18: Arbitrary Envelope Signal Generator

Control System

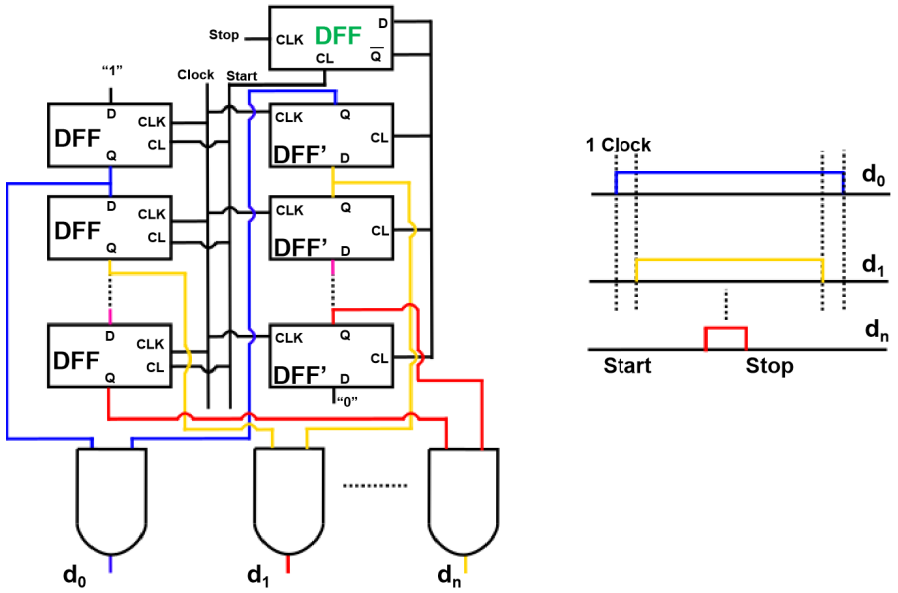


FIGURE 4.19: Control system for Switch Array

Then, the stop signal becomes logic "1" and input to DFF (green) as clock. The input D is reverse to logic 1 and $\overline{Q}$ turns to logic "0". The DFF's stop the reset state and start to work. With difference performance of DFF, the DFF's shift the signal and perform the falling edge of "pyramid". Then the next the start signal comes logic "1", the DFF (green) is reset and output of $\overline{Q}$ becomes logic "1". The "pyramid" is applied to switch array and period of "pyramid" by duration of start and stop.

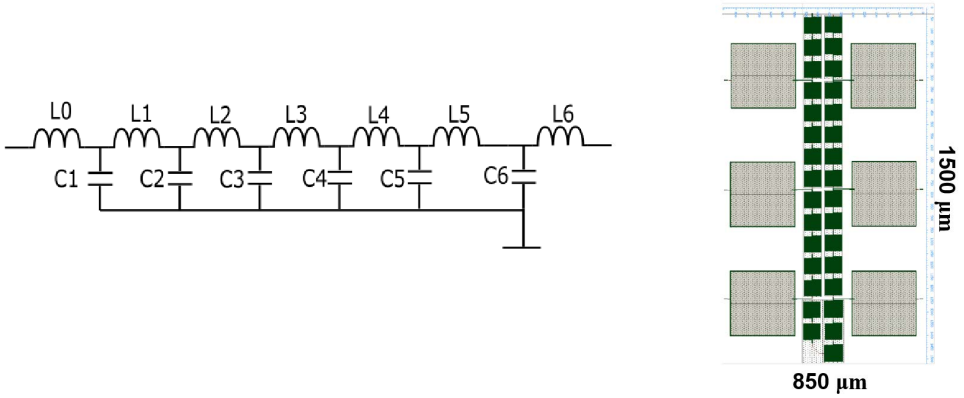


FIGURE 4.20: Low pass filter

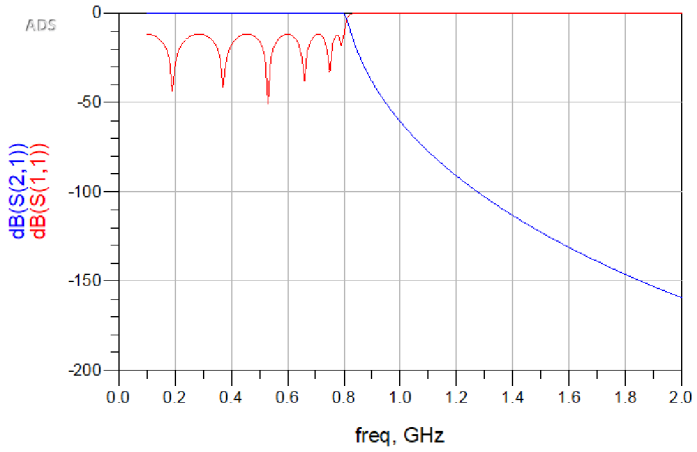


FIGURE 4.21: Low pass filter simulation

Low Pass Filter

To smooth the "pyramid" signal, the low pass filter is required. The total time for one operation is about 20 ns and fastest clock period is about 1 GHz. Thus, the cutoff frequency of filter should be larger than 0.05GHz and smaller than 0.95GHz. Here we choose the frequency is 0.8GHz. The schematic and layout is presented in fig.4.20.

Besides, we choose the Chebyshev type filter. The reason is as follows:

1.Chebyshev filter Chebyshev filters are sharper than the Butterworth filter.

2. Although they are not as sharp as the elliptic one, but they show fewer ripples over the bandwidth

3.Chebyshev filter type 2 may have better ripples than type1 but it needs more cells to realize.

The simulation result of low pass filter is presented in fig.4.21. Although 6 orders of filter require lots of area, it will achieve good performance on characteristic. The chip is fabricated by process of AIST 10 kA/cm2 Nb high-speed standard process (HSTP).

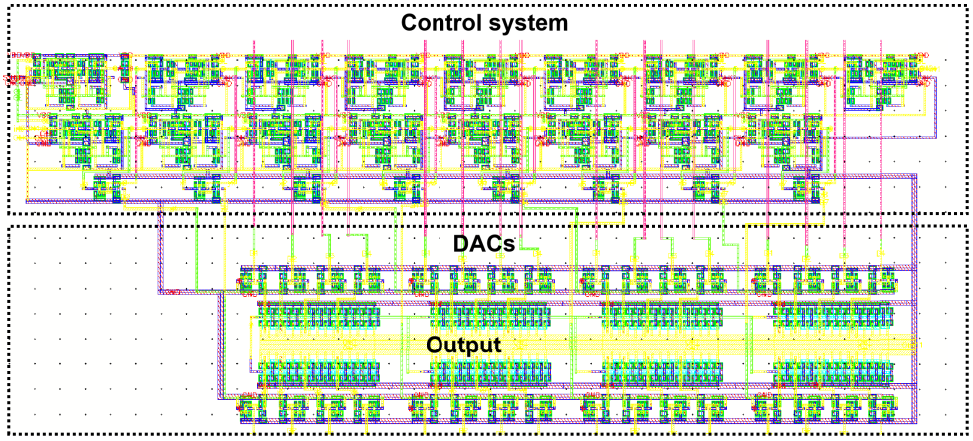


FIGURE 4.22: Chip Photograph of Arbitrary Envelope Signal Generator

4.2.2 Measurement (Without Filter)

The chip photograph of arbitrary envelope signal generator is presented in fig.4.22. Circuits area is about $100\mu m \times 200\mu m$. The power consumption is about 2.13 mW in calculation.

Then we give the measurement result presented in fig.4.23 and fig.4.24 where we can adjust different data of BL in fig.4.18. For example, it is obvious that the triangle type is available if we set the BL data to all logic "1". The operation speed of generator can arrive at 1 MHz because higher speed will lead strong reflection on the clock (CLK) signal. It can be solved by connect a 50 Ω resistance which connects to the ground in future.

On the other hand, we want to test the range of output value. Thus, we remove the current source and use the external bias voltage to provide reference current temporarily. We close the 7 DACs by set the BL all "0" of them and remain one DAC to output maximum value. Margin of single DAC is presented in fig.4.25. We list the two waveform variation trend Within temperature of 4.2 K. The measurement result is close to simulation result. The difference exists because the model parameter is different with actual fabrication. The output decreases with the bias voltage increasing. The variation trend perform Approximately linearly because the β is very small.

Then we set all DACs to output maximum value. The result is presented in fig.4.26.

1. When bias voltage is in the range of from 0.0 V to 0.5 V, the output voltage keeps a stable value both of cryogenic and room temperature. The transistor NOMS is in the saturation area in advance. This will limit the current increasing.

2. When bias voltage is in the range of from 0.5 V to 1 V, the output voltage reveals linear variation trend. In this area because the PMOS start to step to triode region. The current begins to fall up with bais voltage incrasing.

3. When the bias voltage is close to 1.2 V, the output current is very small. The threshold current of PMOS can be evaluated about 0.7 V.

We compare the result under cryogenic and room temperature. Generally, the current is smaller under room temperature because the bigger resistance. Room temperature β seems smaller than cryogenic using the fabrication process

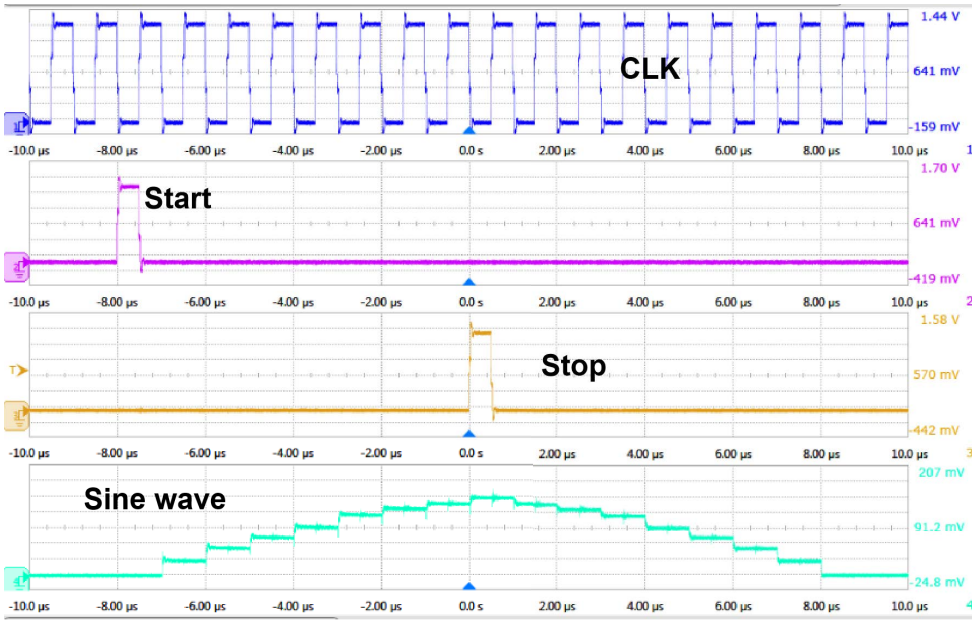


FIGURE 4.23: Measurement result of Arbitrary Envelope Signal Generator (Sine Type)

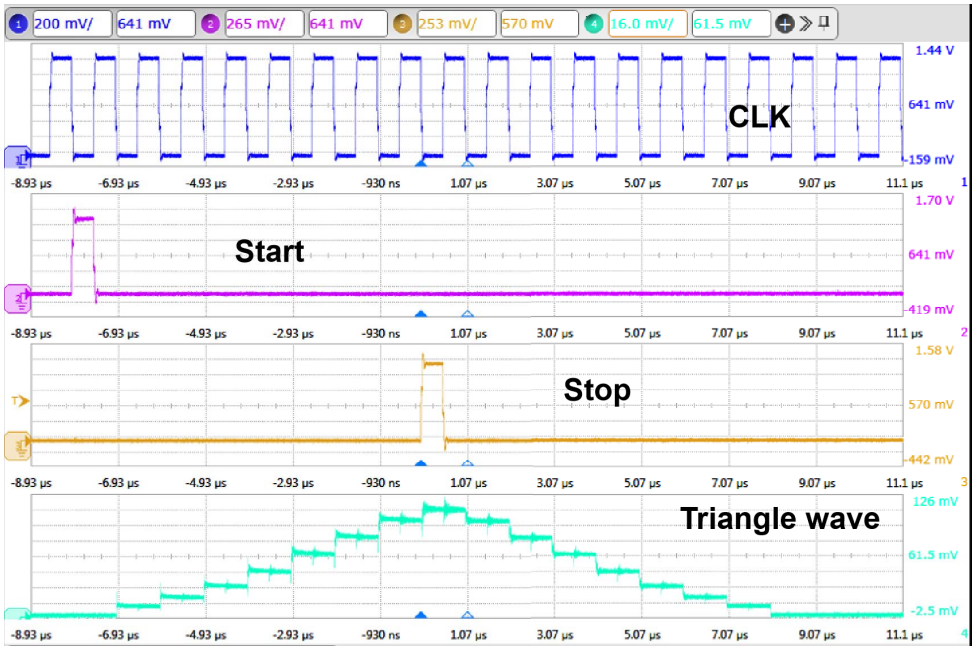


FIGURE 4.24: Chip Photograph of Arbitrary Envelope Signal Generator (Triangle Type)

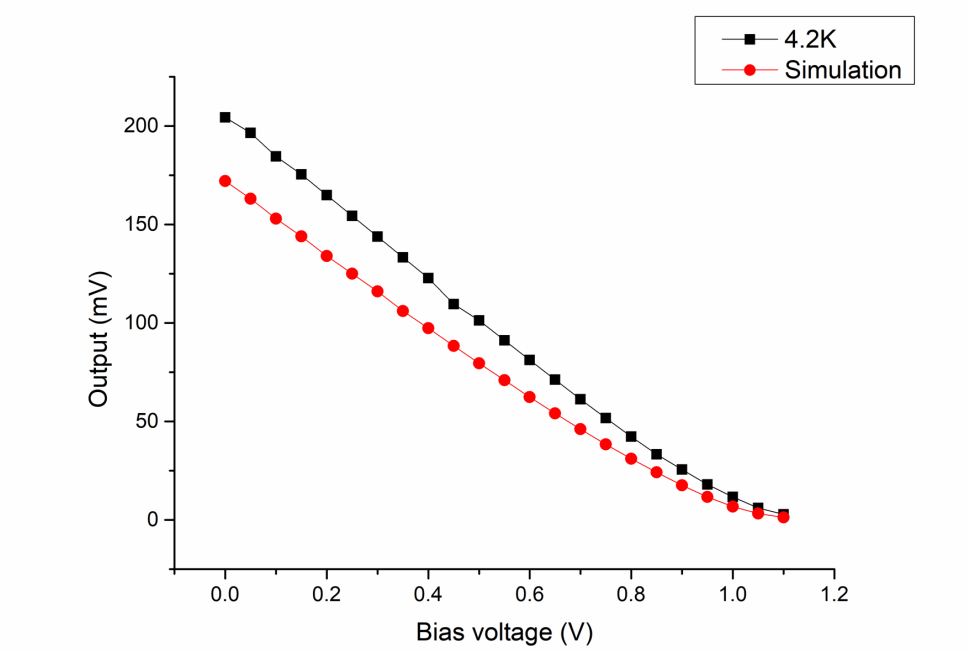


FIGURE 4.25: Single DAC Maximum Output vs.Bias Voltage

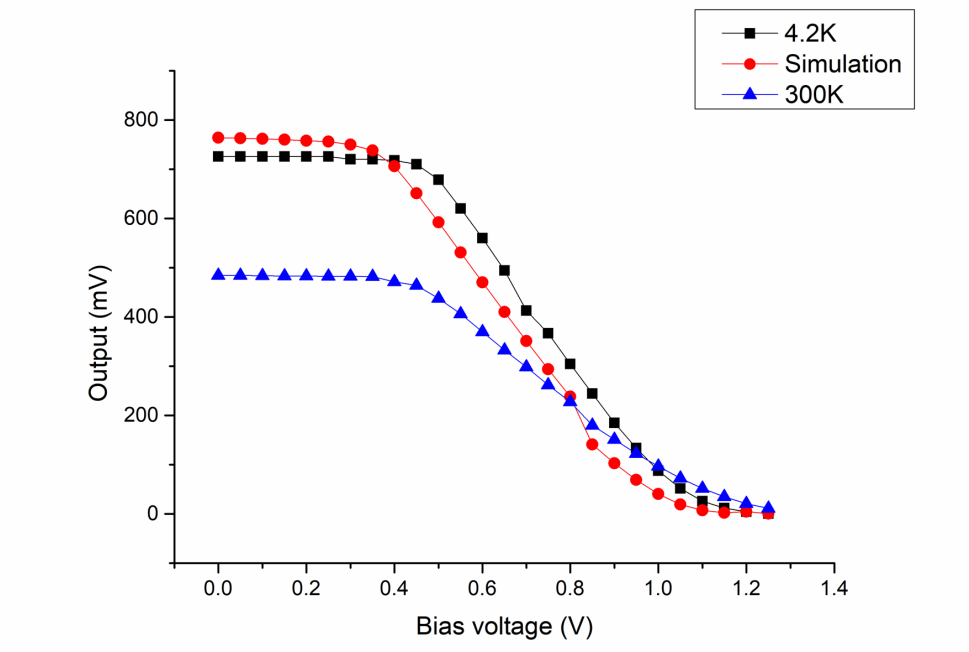


FIGURE 4.26: All DACs Maximum Output vs.Bias Voltage

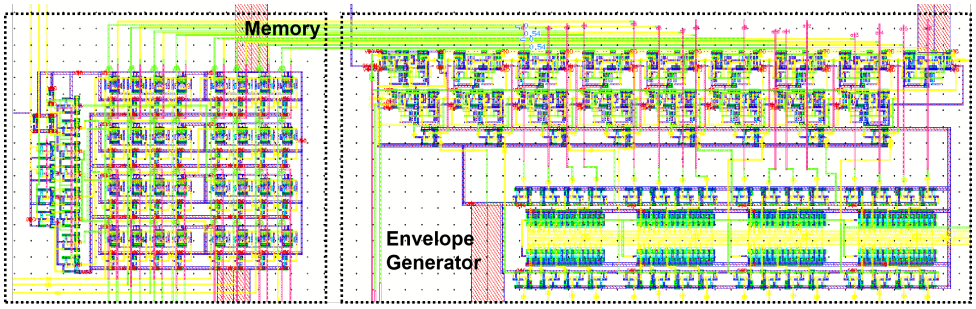


FIGURE 4.27: CMOS Memory Envelope Generator

4.3 Conclusion

We design an arbitrary envelope signal using Cyo-CMOS technology. The process is Rohm 18 μm. We confirm that it can generate different "pyramid" type signal by detecting waveform. We measure the range of output current which can be used to improve the sensitive. Several logic and analog cell with layout are designed, which will be convince for designing other circuits. Especially, the DAC cell is not only applied in CMOS circuits, but also applied in CMOS-SFQ hybrid system to control the bias current.

However, the filter has not been send before this thesis is finished. Therefore, we have not get the measurement result including the low pass filter. Although the this generator has only 8 DACs, it also has potential to improve the sensitive to increase the number of DACs. Higher sensitive will make the output signal closer to the target such as Gaussian waveform. The amount of BL is very large so we can use a memory to save this cables which is presented in fig.4.27.

Chapter 5

Improvement for Microwave Generator

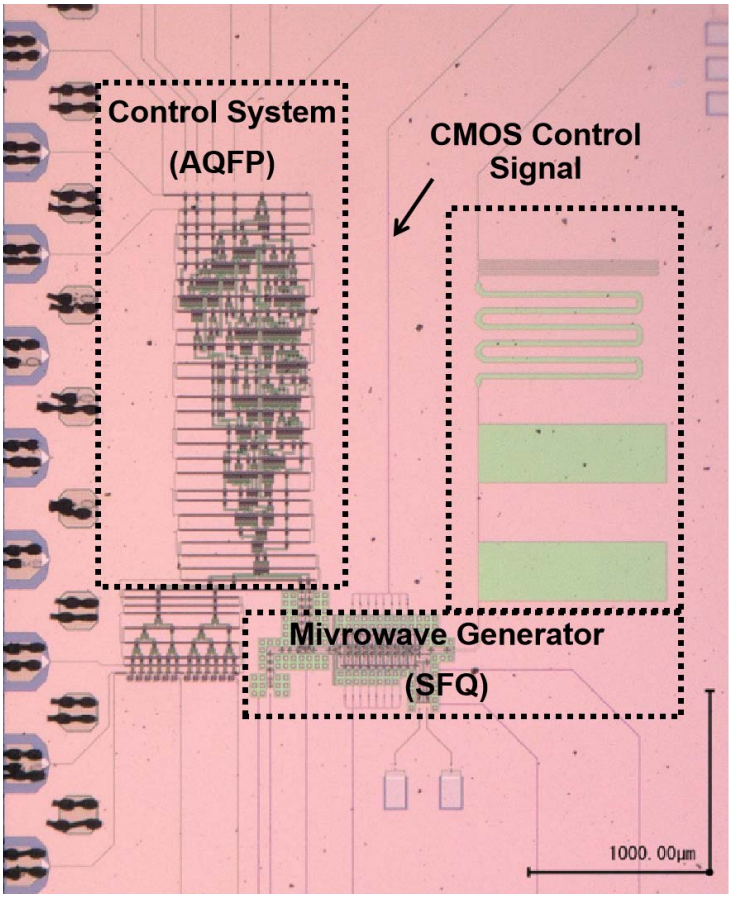


FIGURE 5.1: Photograph of pilot version

We have introduce the each parts of QEC system presented in fig.1.4. This structure can save lots of cables to connect to qubit, especially when the number of qubit increases. For example, we can apply multiple generator to control multiple qubits just need one signal generator in room temperature. Besides, we can correct several qubits by single control system. The microwave generator (SFQ) can be fabricated by low I_c Jpsephson Junction, which reveals the potential of connect to qubit in the future.

Here, we present the system photograph in fig.5.1. Because the measurement of low filter which is applied in CMOS control system has not been finished, the fig.5.1 is the pilot version of the system. The chip area is about $3000\mu m \times 2500\mu m$.

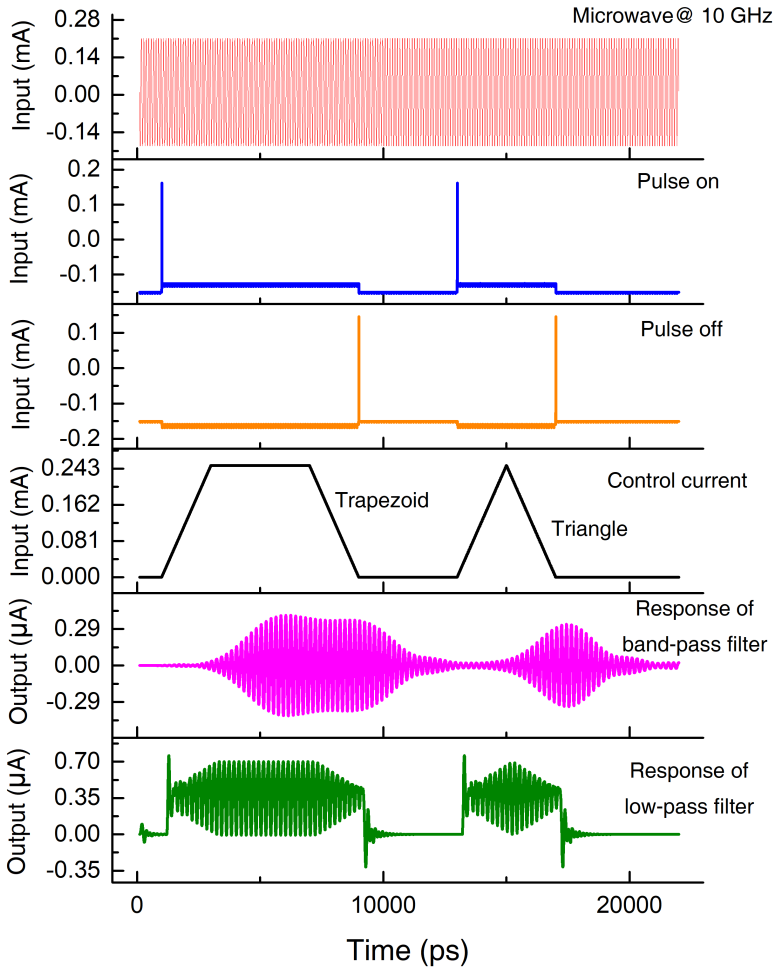


FIGURE 5.2: Simulation Result

The simulation result is presented in fig.5.2. In this simulation, we input the continues 10 GHz microwave. And we said we can adjust the duration of pulse on and pulse off though timing controller circuits. During the period of pulse on and off, the envelope signal which is determined by control current can modulate microwave shape. For example, we input the trapezoid and triangle signal at two periods. We apply two types of filter to observe the waveform. Both of band pass filter and low pass filter can achieve the modulated microwave. However, the band pass filter will make a latency of response which is mainly decided by the bandwidth. On the other hand, low pass will output waveform immediately but it owns the DC signal and pulse signal at the beginning and end.

According to the simulation result, the amplitude of microwave is about 0.35 μA both of band and low pass filter. We can calculate the thermal noise as follows :

$$V_{noise} = \sqrt{4K_bRTB} \tag{5.1}$$

Then the Signal to Noise Ratio (SNR) can be calculated as follows:

$$V_{noise} = 10lg(\frac{P_s}{P_n}) \approx 20dB \tag{5.2}$$

Here is some problems to be solved:

1. The amplitude of output microwave is small. Especially, the power will be smaller if the low critical current of Junction is applied in the future.

2. The initial phase can not be controlled. As mentioned in chapter 1, the initial phase will decide the Bloch ball rote direction. It is necessary to control this parameter for QEC in the future.

3.For high integration, it is necessary to save the area for more numbers of qubits.

Here, we give some suggestion to solve this problem. We design and fabricate the Coupled Resonator Filter to move the impedance matching circuits. We do the measurement to confirm this function. Moreover, we design and fabricate the novel microwave generator which hybrid negative and positive pulses.

5.1 Measurement of Coupled Resonator Filter

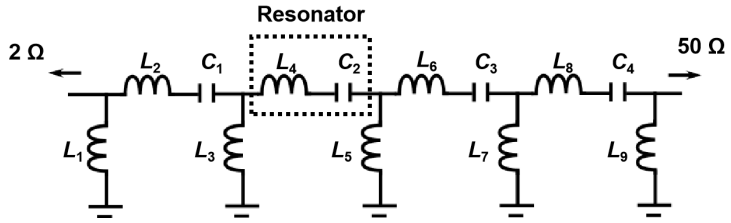


FIGURE 5.3: Coupled Resonator Filter

The filter is necessary for pulse signal for generating microwave. Although the area of filter can be optimised, the impatience matching circuits can be saved by novel type filter - Coupled Resonator Filter (CRF) which is presented in fig.5.3. CRF is applied to transform the low pass filter to band pass filter by inserting many stages resonator generally. Many researches has been done so we give the parameter directly in Tab.5.1 [1]. Because the resistance is changed by resonator, the parameter is unsymmetrical.

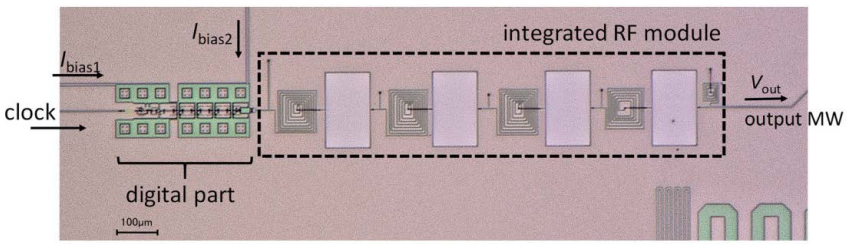


FIGURE 5.4: Chip photograph of CRF

TABLE 5.1: Circuits Margin of Measurement

No.	Parameter name	Value	Parameter name	Value
1	L_1	409.66 pH	C_1	1277.3fF
2	L_2	751.56 pH	C_2	1277.3fF
3	L_3	15.28 pH	C_3	1277.3fF
4	L_4	768.96 pH	C_4	1277.3fF
5	L_5	11.60 pH	L_8	609.3pH
6	L_6	768.96 pH	L_9	609.3pH
6	L_7	15.28 pH		

Although the chip is fabricated which is presented in , how to measure the filter becomes a problem. Once we detected the characteristic using Vector Network Analyze (VNA), the result is hard to be observe because the two ports impedance mismatch. Therefore, we apply an another method to detect the characteristic of CRF. The chip photograph is presented in fig.5.4. The biggest problem is the cross talk which will disturb the measurement result. That means we can not input 5GHz signal directly. We suggest that input 2.5 GHz pulse to detect the characteristic. However, this method will lead to loss half signal. Thus we apply the another characteristic of DC-SFQ to offset the signal., which can generate two pulse at a time.

Assume the SFQ pulse is ideal pulse signal. The infinite impulse response of a system can be present as follows:

$$f_s(t) = f(t) \bigotimes h(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_1) \bigotimes h(t) \tag{5.3}$$

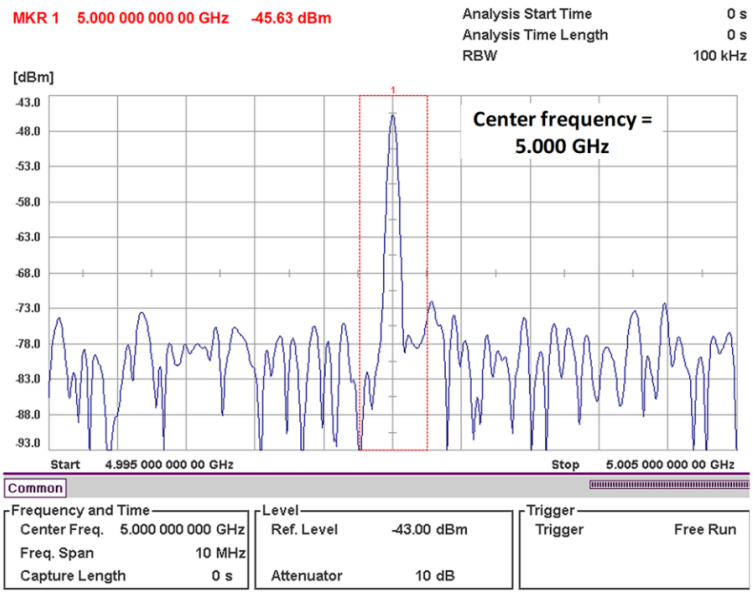
Assume the SFQ pulse is ideal pulse signal. $h(t)$ is filter system function. T_1 is period of pulse sequence. The infinite impulse response of a system can be present as follows:

$$f_s(\omega) = 2\pi(\sum_{n=-\infty}^{\infty} \delta(\omega - n\omega_1)) \times H(\omega) \tag{5.4}$$

We do duplicate the pulse time t_0 later (t_0 is very small), the formula can be presented as follows:

$$\begin{aligned} F_s(\omega) &= 2\pi(\sum_{n=-\infty}^{\infty} \delta(\omega - n\omega_1)(1 + e^{-j\omega t_0})) \times H(\omega) \\ &\approx 4\pi(\sum_{n=-\infty}^{\infty} \delta(\omega - n\omega_1)) \times H(\omega) \end{aligned} \tag{5.5}$$

(a)



(b)

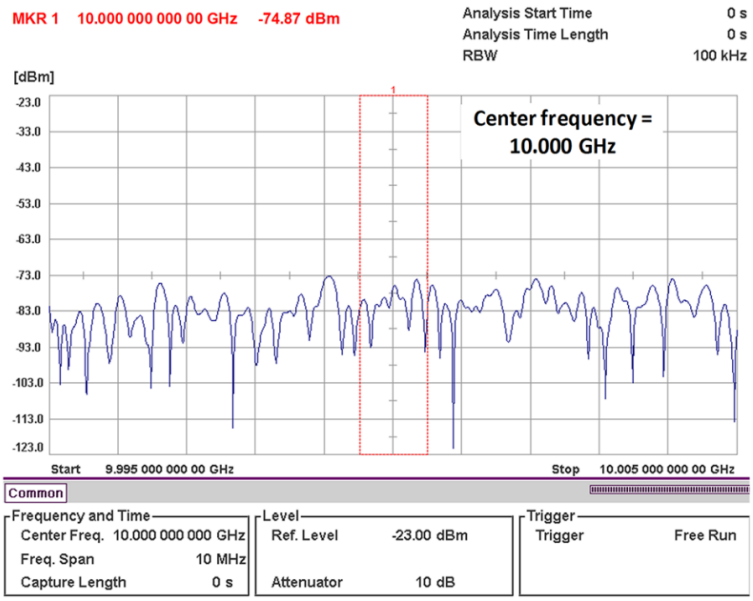


FIGURE 5.5: Measurement of Characteristic using Spectrum Analyzer

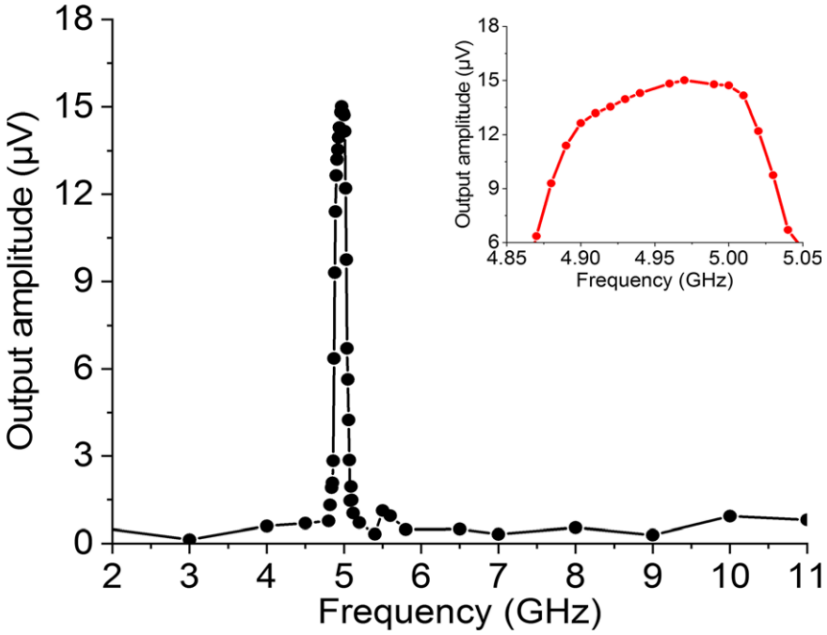


FIGURE 5.6: Summary of Characteristic

Assume the bandwidth of filter is from ω_L to ω_R, then we can adjust the period of SFQ-pulse sequence to observe the bandwidth by judging the amplitude variation. We make the summary to reveal the characteristic of band pass filter. The maximum value of output is about 1.5 μV, which is close to the simulation value. According to variation of amplitude value, we can valuate the range is about 4.85 GHz to 5.05 GHz.

5.2 Novel Microwave Generator

As mentioned, the amplitude of microwave should be amplified and initial phase should be controlled. Let us assume if there are negative pulse mixing into positive pulse, what will happen.

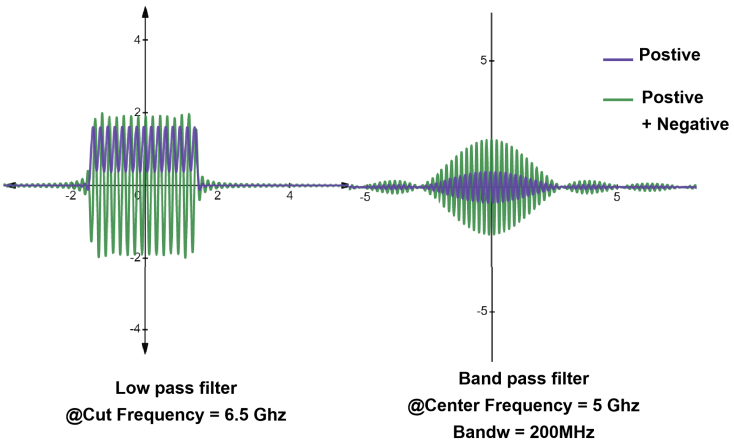


FIGURE 5.7: Negative and positive pulse hybrid

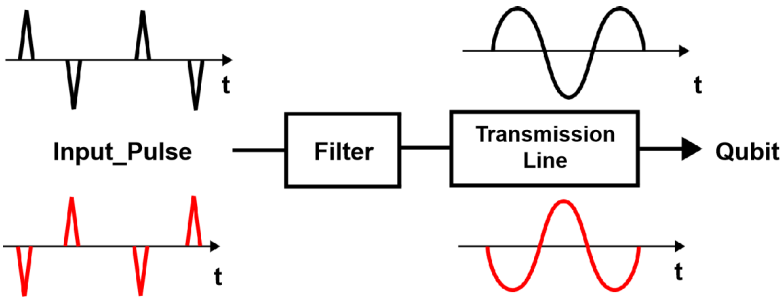


FIGURE 5.8: Hybrid negative pulse to control the phase

The do the mathematical model which is similar with function (2.23). The result of two types is presented in fig.5.7. We apply several pulses to simulate this model. The amplitude of output which hybrid the negative pulse (green) is much larger than before (purple) on both band pass and low pass filter. What is more, the dc component is disappear. More over, the initial pulse will decide the initial phase of microwave which is presented in Fig.5.8. It is obvious that if the first pulse is positive, phase of microwave is 0. On the other hand, if the pulse is negative, the phase should be π.

5.2.1 Negative Pulse Generator

So it is very important for us to design a circuit which can generate the positive pulse. The circuit is present in fig.5.9. This circuits is applied to transform one positive pulse to one negative pulse. We consider the loop which contains the J_1,J_2,J_3 and J_4. Once the pulse is input to J_1 from JTL, the phase of J_1 will turn 2π. Then, we insert two same JJ (J_2 and J_3) to let them switch at same time. Thus, the phase on the loop will turn 4 π.

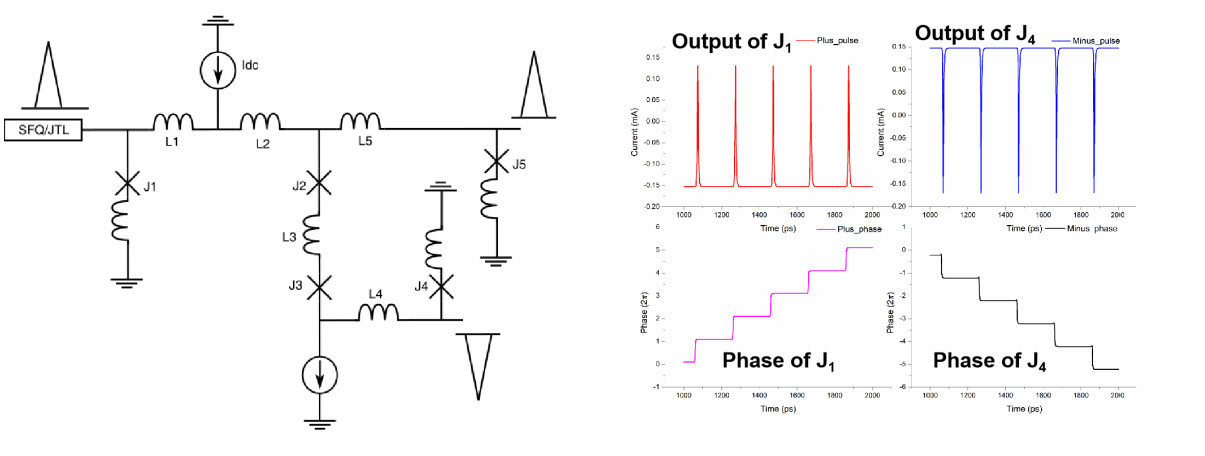


FIGURE 5.9: Negative Pulse Generator

To keep balance, the phase of J_4 has to turn -2π. According to formula (2.2), the output pulse will be negative. For keeping latency output pulse the same, we add another road to output positive pulse. The simulation is present at right of fig.5.9.

$$\phi_1 + \frac{2\pi I_1 \times L_{1+2}}{\Phi_0} + \phi_{23} = \frac{2\pi I_4 \times L_4}{\Phi_0} + \phi_4 \tag{5.6}$$

$$\phi_1 - \phi_{23} \approx \phi_4 \tag{5.7}$$

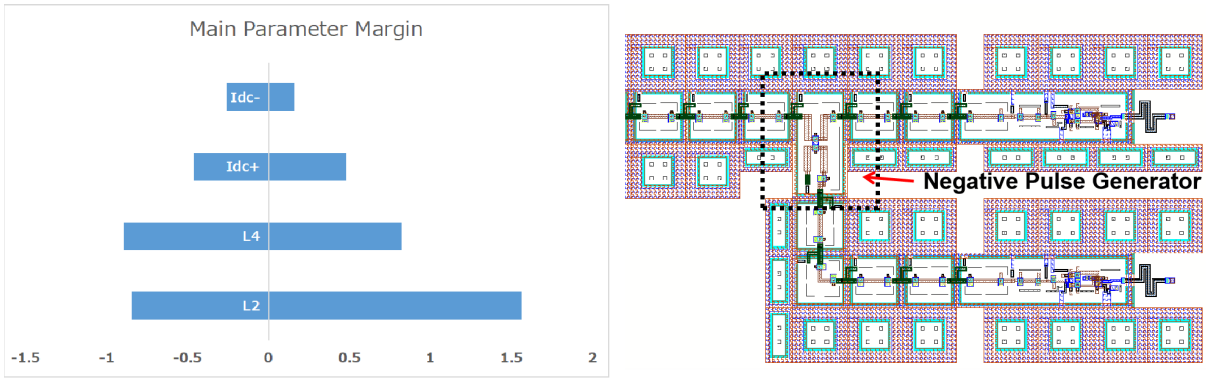


FIGURE 5.10: Margin and Layout of Negative Pulse Generator

The design margin and layout is presented in fig.5.10. Here to confirm the right operation, we should test both positive and negative pulse to ensure the signal is inverse. The margin of main parameter is almost beyond 100%. The minimum can arrive 40%.

Phase Control Circuit

With the negative pulse generator, it is possible for us to control the phase. The schematic of control circuits is presented in fig.5.11. Pulse sequence is input and the switch is applied to control the duration of it. Here we apply the splitter to separate the pulse and

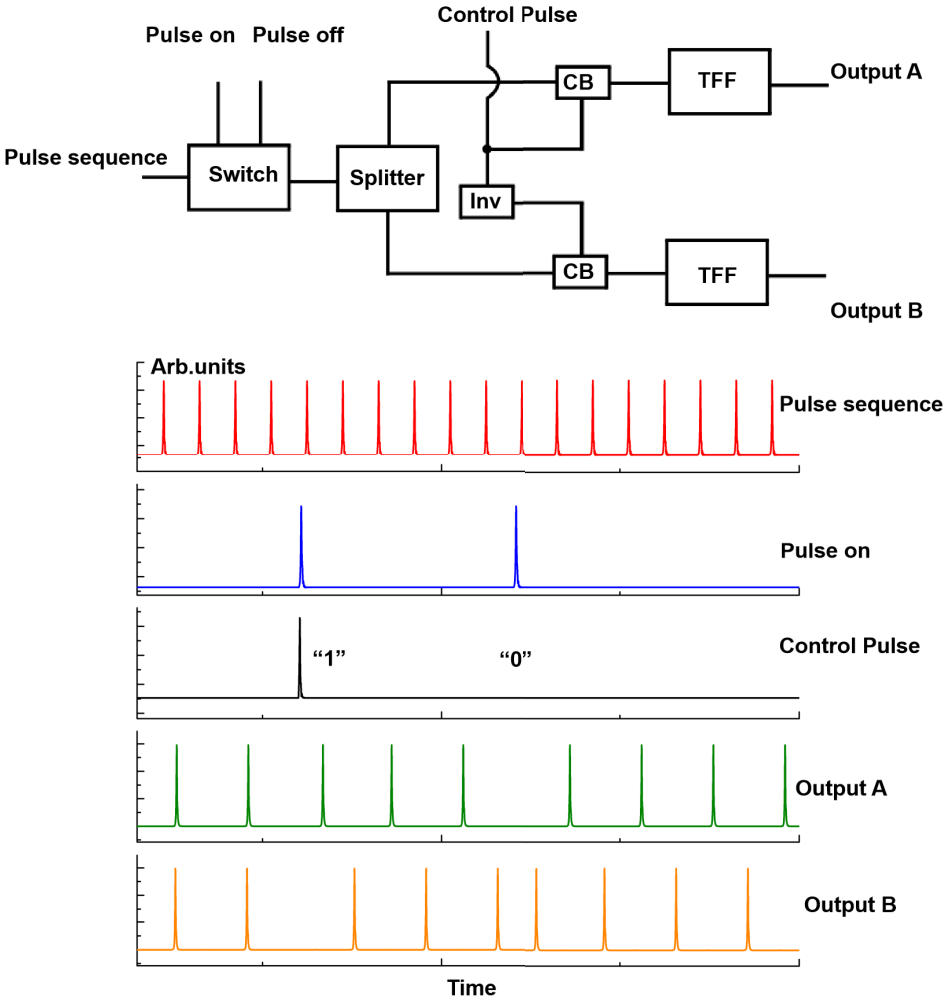


FIGURE 5.11: Phase Control circuits using SFQ

input to the two TFFs. The control pulse as external pulse input to TFF. Inverter (Inv) is applied so that the only one TFF can receive the pulse. This decided which TFF can output pulse in advance. The pulse on is the clock signal of Inv. The simulation result is presented. For example, once the control pulse is input as "1" when pulse on is input. The top TFF will receive the control pulse plus separated pulse and output the pulse at first. Output B should wait the next separated pulse. On the other when control pulse is logic "0", the output B will output pulse firstly. Based on this, we can control the phase just by inversion of pulse B which is shown as fig.5.8.

Wilkinson Power Divider

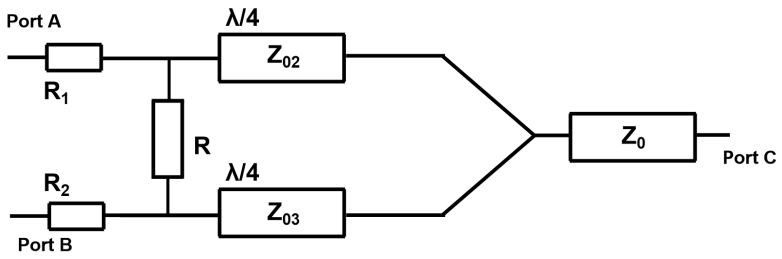


FIGURE 5.12: Principle of Wilkinson Power Divider

Although we have both negative and positive pulse, it is difficult to confluence them because the bias current of them is inverse. Thus, generally confluence buffer (CB) will not work. Consider this hybrid signal is applied to filter, we suggest using Wilkinson power divider to connect the filter. Although it is called power divider, it also can be applied to confluence the power together. The principle is presented in fig.5.12. We set the Z_{CA} is resistance where is from port C to port A and Z_{BA} is is resistance where is from port C to port B. Thus, the formulation can be presented in as follows:

$$\frac{1}{Z_0} = \frac{1}{Z_{CA}} + \frac{1}{Z_{CB}} \tag{5.8}$$

And we assume the power ratio (K) can be presented as follows:

$$k^2 = \frac{P_A}{P_B} = \frac{R_1}{R_2} \tag{5.9}$$

According $\lambda/4$ transmission theory, the formula can be presented as follows:

$$Z_{02}^2 = Z_{AC} \times R_1 \tag{5.10}$$

$$Z_{02}^2 = Z_{BC} \times R_2 \tag{5.11}$$

Assume the $R_2 = kZ_0, R_3 = Z_0/K$, the Z_{02}^2 and Z_{03}^2 can be calculated as follows:

$$Z_{02}^2 = Z_0\sqrt{k(1+k^2)} \tag{5.12}$$

$$Z_{02}^2 = Z_0\sqrt{\frac{(1+k^2)}{k^3}} \tag{5.13}$$

Generally, we set the $k = 1$ to ensure the same power from port A and port B. If we add the resistance R, it can increase the isolation of port A and port B to achieve higher bandwidth. For example if the signal reflect from A to B, it must pass though two $\lambda/4$ transmission line. Thus the phase will be inverse. On the other hand ,the signal can pass A to B though the resistance R, which does not need phase inverse. The this two

signal will offset. The resistance is presented to match impatience as follows:

$$R = Z_0(k + \frac{1}{k}) \tag{5.14}$$

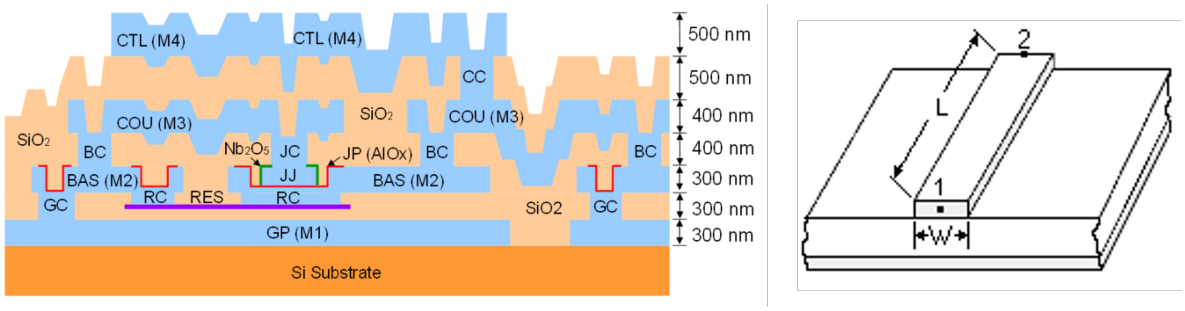


FIGURE 5.13: HSTP process

In this case, we will use HSTP process which is presented in fig.5.13. We apply the CTL layer to design transmission model in fig.5.13. The Width is decided by impatience match value, and length is decided by frequency. After calculation, the width is about 1 μ m for 70.7 Ω and 2.1 m for 50 Ω. The schematic of circuits is presented in fig.5.14 and the layout is presented in fig.5.15. The circuits area is about $1mm \times 2mm$.

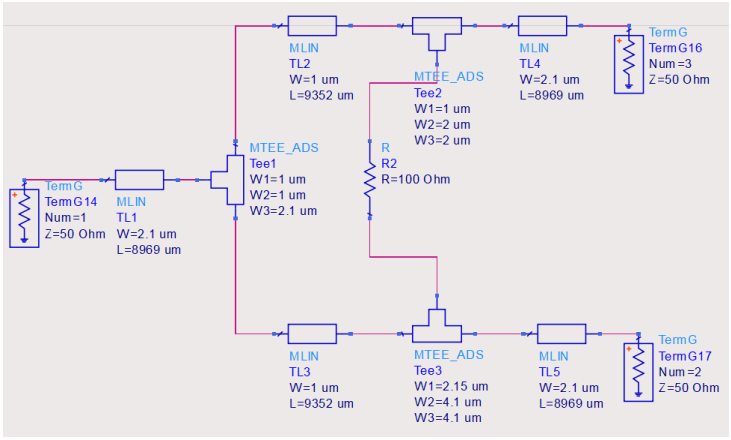


FIGURE 5.14: Schematic for Calculating the Parameter

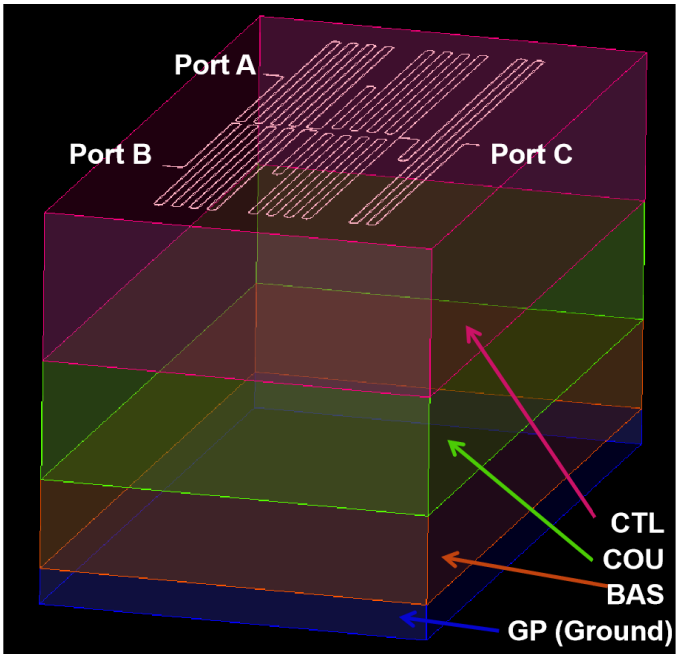


FIGURE 5.15: Layout of Wilkinson Power Divider

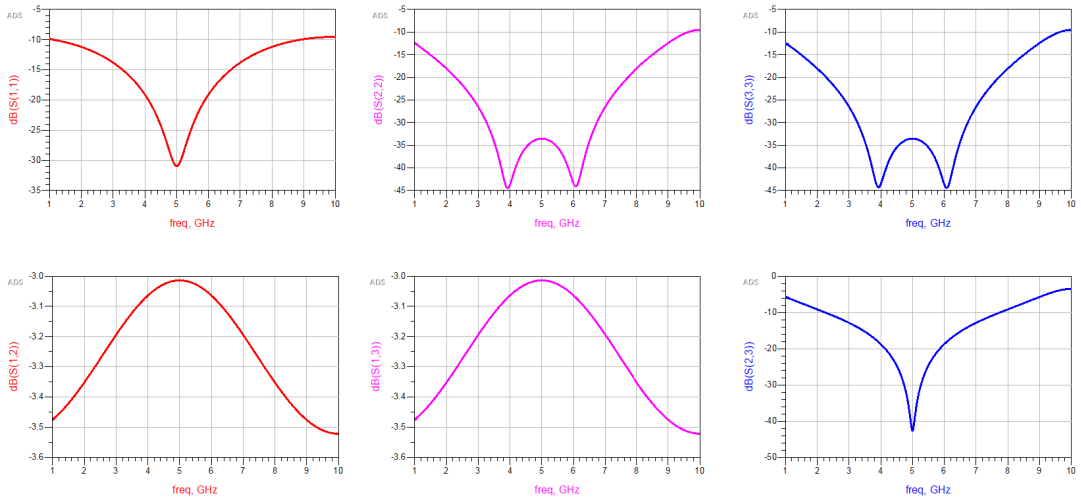


FIGURE 5.16: Simulation result of Wilkinson Power Divider

The simulation result is presented in fig.5.16. Simulator isAdvanced Design system (ADS). The reflection of eachports can be restrained below the -30dB at 5 GHz. On the other hand, the transmission parameter S_12 and S_13 is about -3dB at 5 GHz. The loss may be caused by calculation error on the layout. The S_32 is restrained below -40dB, that shows the 5 GHz signal is limited from port A to B.

5.3 Schematic and Simulation of Novel Microwave Generator

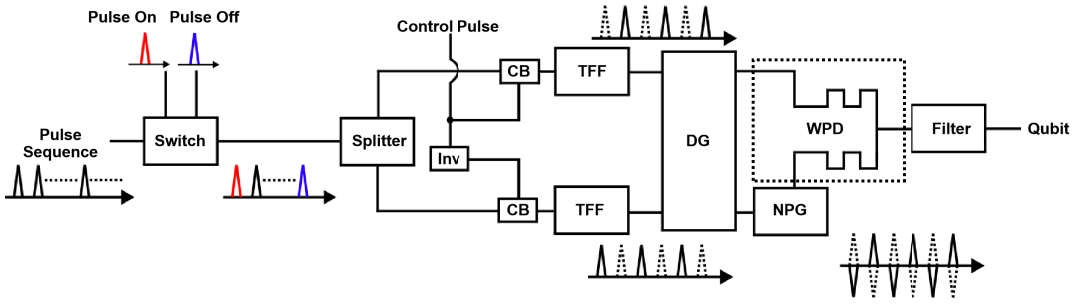


FIGURE 5.17: Schematic of Novel Microwave Generator

The schematic of novel microwave generator is presented in fig.5.17. Here the negative pulse generator (NPG) and Wilkinson power divider (WPD) are applied. Operation principle is almost the same with the traditional type. The different thing is that we add the phase control circuits to control the first pulse in the sequence. Besides, we use the NPG to inverse one side pulses. At last, we combine the pulse together using PWD. The WPD can take impedance matching theoretically which can save lots of area. But this stage we set the 50 Ω matching for measurement. Filter is applied as band pass filter where bandwidth is about 200 MHz.

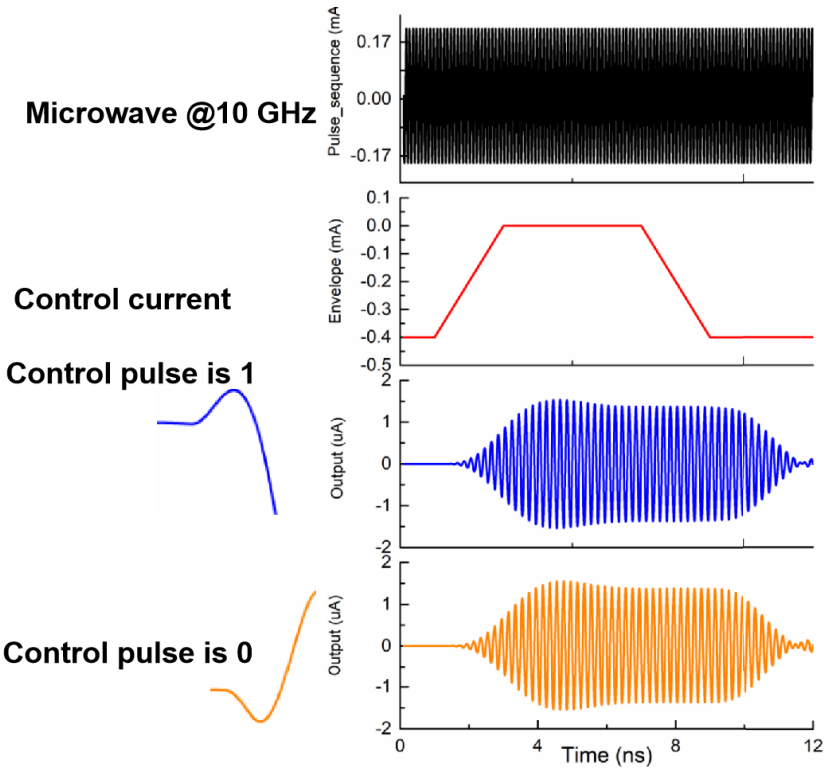


FIGURE 5.18: Simulation of Novel Pulse Generator

TABLE 5.2: Two types of microwave generator

No.	Parameter Name	Traditional	Novel
1	Chip Area	3000 μm $\times$ 3000 μm	4000 μm $\times$ 4000 μm
2	Maximum Amplitude	0.3 μA	1.5 μA
3	SNR	20 dB	34 dB
4	Initial Phase Controllable	No	Yes
5	Number of JJs	170	330
6	Bias Current (total)	20 mA	39 mA

Here, we give the simulation result in fig.5.18. We input 10 GHz microwave signal (Black). At same time we apply the trapezoid type control current to modulate the envelope the microwave as an example. We present two control situations where control pulse is logic "1" and "0". The amplitude of output signal can arrive about 1.5 μA which is five times of transitional types. Shape of output microwave shows the trapezoid because of control current.

5.4 Conclusion

In section we have do some suggest to improve the amplitude of generated microwave. Moreover, we can make the initial phase of microwave controllable. Although the power divider will be applied, but this parts can be optimised in the future.

Here is the comparison of two types of microwave generators in Tab.5.2. Compared with traditional one, WPD of novel one take a external area. The characteristic of microwave is improved in simulation. Power consumption increase with the numbers of jj which will disturb the qubit state in future. Some research about reducing the power consumption is under process such as using ERSQ instead of SFQ cells. Moreover, the phase of microwave should be calibrated by adjusting the parameter.

Chapter 6

Conclusion and Future Work

Quantum computer owns the potential to solving more problem which traditional computer can not solve. There is a problem that the error will rise easily with growing of numbers of qubit. Thus, we need a QEC system to realize the fault tolerant quantum computer. The QEC system requires the low temperature qubit control system and we suggest a structure which is supposed by superconducting circuits and cryogenic CMOS to control the qubit.

1. We design the microwave generator using SFQ circuits. The amplitude and duration of generated microwave can be controlled which is mainly influence the qubit state. We fabricate it with HSTP process and confirm the function with measurement.

2.We designed the duration timing control circuits and integrator which is applied in the JPO using AQFP circuits. AQFP circuits owns the lower power consumption than SFQ. It is possible to instead the SFQ circuits to generate microwave. On the other hand, we need JPO to read out the state of qubit. To improve the sensitive of read out system, we design the integrate to gather the data with AQFP. Both of circuits has been confirmed with measurement.

3. It is not enough that just control the duration of microwave. Therefore, we designed an arbitrary envelope generator with cryogenic CMOS technology. Although the CMOS will cost lots of energy than superconducting circuits, it can be applied within 4.2K and superconducting circuits can be applied within several mk. On the other hand, the CMOS can provide the stable current which can be applied as control current of microwave generator. This circuits has been confirmed with measurement.

4.Although the amplitude and duration of generated microwave can be controlled, the SNR is small (about 20dB). Thus, we suggest a new method to improve the signal SNR with negative pulse. On the other hand, the initial phase of microwave is also can be controlled. According the simulation, the SNR can increase to about 34 dB. Besides, we design the band pass filter which does not required the impedance matching circuits to save the area of chip.

In the future, we plan to reduce the power consumption of microwave generator where the Energy-efficient SFQ (ERSFQ) circuits may be applied. Moreover, the phase of microwave should be calibrated to ensure the center frequency is 5GHz. At least, we hope to apply the negative pulse and positive pulse in the microwave generator to control the qubit.

Bibliography

[1] Man-Hong Yung, James D. Whitfield, Sergio Boixo, David G. Tempel, and Alá n Aspuru-Guzik. Introduction to quantum algorithms for physics and chemistry. In *Advances in Chemical Physics*, pages 67–106. John Wiley & Sons, Inc., mar 2014.

[2] T. D. Ladd, F. Jelezko, R. Laflamme, Y. Nakamura, C. Monroe, and J. L. O'Brien. Quantum computers. *Nature*, 464(7285):45–53, mar 2010.

[3] P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, and W. D. Oliver. A quantum engineer's guide to superconducting qubits. *Applied Physics Reviews*, 6(2):021318, jun 2019.

[4] Oliver Morsch and Markus Oberthaler. Dynamics of bose-einstein condensates in optical lattices. *Rev. Mod. Phys.*, 78:179–215, Feb 2006.

[5] John Proos and Christof Zalka. Shor's discrete logarithm quantum algorithm for elliptic curves. 2003.

[6] Lov K. Grover. Quantum mechanics helps in searching for a needle in a haystack. *Phys. Rev. Lett.*, 79:325–328, Jul 1997.

[7] Manuel Vogel. Quantum computation and quantum information, by m.a. nielsen and i.l. chuang. *Contemporary Physics - CONTEMP PHYS*, 52:604–605, 11 2011.

[8] Joseph C. Bardin, Daniel H. Slichter, and David J. Reilly. Microwaves in quantum computing. *IEEE Journal of Microwaves*, 1(1):403–427, jan 2021.

[9] Panagiotis Giounanlis, Elena Blokhina, Krzysztof Pomorski, D. Leipold, and Robert Staszewski. Modeling of semiconductor electrostatic qubits realized through coupled quantum dots. *IEEE Access*, PP:1–1, 04 2019.

[10] R McDermott, M G Vavilov, B L T Plourde, F K Wilhelm, P J Liebermann, O A Mukhanov, and T A Ohki. Quantum–classical interface based on single flux quantum digital logic. *Quantum Science and Technology*, 3(2):024004, jan 2018.

[11] D. Vion, A. Aassime, A. Cottet, P. Joyez, H. Pothier, C. Urbina, D. Esteve, and M. H. Devoret. Manipulating the quantum state of an electrical circuit. *Science*, 296(5569):886–889, may 2002.

[12] Ethan Bernstein and Umesh Vazirani. Quantum complexity theory. *SIAM Journal on Computing*, 26(5):1411–1473, 1997.

[13] M. H. Devoret, A. Wallraff, and J. M. Martinis. Superconducting qubits: A short review, 2004.

[14] Jacob Biamonte, Peter Wittek, Nicola Pancotti, Patrick Rebentrost, Nathan Wiebe, and Seth Lloyd. Quantum machine learning. *Nature*, 549(7671):195–202, sep 2017.

[15] Shruti Puri, Christian Kraglund Andersen, Arne L. Grimsmo, and Alexandre Blais. Quantum annealing with all-to-all connected nonlinear oscillators. *Nature Communications*, 8(1), jun 2017.

[16] Ari Mizel, Daniel A. Lidar, and Morgan Mitchell. Simple proof of equivalence between adiabatic quantum computation and the circuit model. *Physical Review Letters*, 99(7), aug 2007.

[17] Dorit Aharonov, Michael Ben-Or, and Elad Eban. Interactive proofs for quantum computations, 2008.

[18] John Preskill. Fault-tolerant quantum computation, 1997.

[19] A Batra, C D Weis, J Reijonen, A Persaud, T Schenkel, S Cabrini, C C Lo, and J Bokor. Detection of low energy single ion impacts in micron scaletransistors at room temperature. *Applied Physics Letters*, 91(19), 10 2007.

[20] J. von Neumann. *Probabilistic Logics and the Synthesis of Reliable Organisms From Unreliable Components*, pages 43–98. Princeton University Press, Princeton, 1956.

[21] Péter Gács. Reliable computation with cellular automata. *Proceedings of the fifteenth annual ACM symposium on Theory of computing*, 1983.

[22] Daniel Gottesman. Theory of fault-tolerant quantum computation. *Physical Review A*, 57(1):127–137, jan 1998.

[23] A.Yu. Kitaev. Fault-tolerant quantum computation by anyons. *Annals of Physics*, 303(1):2–30, jan 2003.

[24] P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, and W. D. Oliver. A quantum engineer's guide to superconducting qubits. *Applied Physics Reviews*, 6(2):021318, jun 2019.

[25] Dorit Aharonov and Michael Ben-Or. Fault-tolerant quantum computation with constant error rate, 1999.

[26] S. B. Bravyi and A. Yu. Kitaev. Quantum codes on a lattice with boundary, 1998.

[27] Jay M. Gambetta, Jerry M. Chow, and Matthias Steffen. Building logical qubits in a superconducting quantum computing system. *npj Quantum Information*, 3(1), jan 2017.

[28] Peter W. Shor. Polynomial-time algorithms for prime factorization and discrete logarithms on a quantum computer. *SIAM Journal on Computing*, 26(5):1484–1509, oct 1997.

[29] Lov K. Grover. Quantum mechanics helps in searching for a needle in a haystack. *Phys. Rev. Lett.*, 79:325–328, Jul 1997.

[30] Easwar Magesan, Jay M. Gambetta, A. D. Córcoles, and Jerry M. Chow. Machine learning for discriminating quantum measurement trajectories and improving readout. *Phys. Rev. Lett.*, 114:200501, May 2015.

[31] M. Mehrpoo, Bishnu Patra, Jiang Gong, P. Hart, J. Dijk, H. Homulle, G. Kiene, A. Vladimirescu, Fabio Sebastiano, E. Charbon, and Masoud Babaie. Benefits and challenges of designing cryogenic cmos rf circuits for quantum computers. pages 1–5, 05 2019.

[32] Bishnu Patra, Rosario Incandela, Jeroen Dijk, Harald Homulle, Lin Song, M. Shahmohammadi, Robert Staszewski, Andrei Vladimirescu, Masoud Babaie, Fabio Sebastiano, and Edoardo Charbon. Cryo-cmos circuits and systems for quantum computing applications. *IEEE Journal of Solid-State Circuits*, PP:1–13, 09 2017.

[33] Hongxiang Shen, Naoki Takeuchi, Yuki Yamanashi, and Nobuyuki Yoshikawa. Timing controller for a superconductor microwave switch using adiabatic quantum flux parametron circuits. *IEEJ*, 142(5):197–201, 2022.

[34] Masayuki SHIRANE and Tsuyoshi YAMAMOTO. Superconducting parametric oscillators for quantum annealing. *IEEJ*, 63(3):112–116, 2020.

[35] Bishnu Patra, Jeroen P. G. van Dijk, Sushil Subramanian, Andrea Corna, Xiao Xue, Charles Jeon, Farhana Sheikh, Esdras Juarez-Hernandez, Brando Perez Esparza, Huzaifa Rampurawala, Brent Carlton, Nodar Samkharadze, Surej Ravikumar, Carlos Nieva, Sungwon Kim, Hyung-Jin Lee, Amir Sammak, Giordano Scappucci, Menno Veldhorst, Lieven M. K. Vandersypen, Masoud Babaie, Fabio Sebastiano, Edoardo Charbon, and Stefano Pellerano. 19.1 a scalable cryo-cmos 2-to-20ghz digitally intensive controller for 4×32 frequency multiplexed spin qubits/transmons in 22nm finfet technology for quantum computers. In *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, pages 304–306, 2020.

[36] D. Ristè, S. Poletto, M.-Z. Huang, A. Bruno, V. Vesterinen, O.-P. Saira, and L. DiCarlo. Detecting bit-flip errors in a logical qubit using stabilizer measurements. *Nature Communications*, 6(1), apr 2015.

[37] Fei Yan, Simon Gustavsson, Archana Kamal, Jeffrey Birenbaum, Adam P Sears, David Hover, Ted J. Gudmundsen, Danna Rosenberg, Gabriel Samach, S Weber, Jonilyn L. Yoder, Terry P. Orlando, John Clarke, Andrew J. Kerman, and William D. Oliver. The flux qubit revisited to enhance coherence and reproducibility. *Nature Communications*, 7(1), nov 2016.

[38] Naoki Takeuchi, Shuichi Nagasawa, Fumihiro China, Takumi Ando, Mutsuo Hidaka, Yuki Yamanashi, and Nobuyuki Yoshikawa. Adiabatic quantum-flux-parametron cell library designed using a 10 ka cm2 niobium fabrication process. *Superconductor Science and Technology*, 30(3):035002, jan 2017.

[39] Naoki Takeuchi, Taiki Yamae, Christopher Ayala, Hideo Suzuki, and Nobuyuki Yoshikawa. An adiabatic superconductor 8-bit adder with 24 k b t energy dissipation per junction. *Applied Physics Letters*, 114:042602, 01 2019.

[40] K.K. Likharev and V.K. Semenov. Rsfq logic/memory family: a new josephson-junction technology for sub-terahertz-clock-frequency digital systems. *IEEE Transactions on Applied Superconductivity*, 1(1):3–28, 1991.

[41] T. Yamamoto, K. Inomata, M. Watanabe, K. Matsuba, T. Miyazaki, W. D. Oliver, Y. Nakamura, and J. S. Tsai. Flux-driven josephson parametric amplifier. 2008.

[42] N. Bergeal, F. Schackert, M. Metcalfe, R. Vijay, V. E. Manucharyan, L. Frunzio, D. E. Prober, R. J. Schoelkopf, S. M. Girvin, and M. H. Devoret. Phase-preserving amplification near the quantum limit with a josephson ring modulator. *Nature*, 465(7294):64–68, may 2010.

[43] Z. R. Lin, K. Inomata, W. D. Oliver, K. Koshino, Y. Nakamura, J. S. Tsai, and T. Yamamoto. Single-shot readout of a superconducting flux qubit with a flux-driven josephson parametric amplifier. *Applied Physics Letters*, 103(13):132602, sep 2013.

[44] C. M. Wilson, T. Duty, M. Sandberg, F. Persson, V. Shumeiko, and P. Delsing. Photon generation in an electromagnetic cavity with a time-dependent boundary. *Physical Review Letters*, 105(23), dec 2010.

Publications

- Research papers

[1] HongxiangShen, et al “Design of a Timing Controller for a Superconductor Microwave Switch using Adiabatic Quantum Flux Parametron Circuits”, IEEJ.142, 197-201 (2022)
[2] Yuxing He, Hongxiang shen,et al “Compact RSFQ microwave pulse generator based on an integrated RF module for controlling superconducting qubit”, Appl. Phys. Lett. 120, 062601 (2022)

- International conferences

[1] HongxiangShen, et al “Design of a timing controller for a superconductor microwave switch using adiabatic quantum flux parametron circuits ”, in conference of the 33rd International Symposium on Superconductivity (ISS 2020)
[2] HongxiangShen, et al “Verification of variable amplitude microwave switch using single flux quantum circuits”, in conference of the 14th Superconducting SFQ VLSI Workshop conference (SSV 2021)
[3]HongxiangShen, et al “Design and demonstration of an 8-bit integrator using adiabatic quantum flux parametron (AQFP) circuits”, in conference of the 15th European Conference on Applied Superconductivity conference (EUCAS 2021)
[4]HongxiangShen, et al “Verification of reducing gray zone width using 8-bit AQFP integrator”, in conference of the 14th Superconducting SFQ VLSI Workshop conference (SSV 2022)
[5]HongxiangShen, et al “Verification of Variable Amplitude Microwave Switch Using Single Flux Quantum Circuits”, in conference of the Applied Superconductivity conference (ASC 2022)

- Domestic conferences

[1] 沈泓翔, et al “断熱量子磁束パラメトロンを用いたマイクロ波パルス長制御用時間計測回路の設計”, 2020年第81回応用物理学会秋季学術講演会
[2] 沈泓翔, et al “断熱量子磁束パラメトロンを用いた8ビット積算回路”, 2021年第68回応用物理学会春季学術講演会
[3] 沈泓翔, et al “断熱量子磁束パラメトロンとCMOSハイブリッド回路を用いた量子ビット制御システムの設計”, 2021年第82回応用物理学会秋季学術講演会
[4] 沈泓翔, et al “断熱量子磁束パラメトロンとCMOSハイブリッド回路を用いた量子ビット制御システムの設計”, 2021年電子情報通信学会ソサイエティ大会
[5] 沈泓翔, et al “SFQ正負パルスを用いてマイクロ波ジェネレータの設計”, 2022年第82回応用物理学会秋季学術講演会

- To be submitted

[1] Hongxiang Shen, et al “Amplitude-controllable microwave pulse generator using single-flux-quantum pulse pairs for qubit control”,APL
[2] Hongxiang Shen, et al “Design and fabrication of 8-bit integrator using adiabatic quantum-flux-parametron circuits”,SUST
[3] Hongxiang Shen, et al “High speed Josephson-CMOS interface circuits applied in the hybrid memory”,IEEE.