Doctoral Thesis

Reduction of DC-Link Capacitance and Improved Performance of a 5-Level Hybrid Multilevel DC-Link Inverter Using Novel PWM Schemes

by

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Declaration

I hereby declare that I am the sole author of this dissertation entitled "**Reduction of DC-Link Capacitance and Improved Performance of a 5-Level Hybrid Multilevel DC-Link Inverter Using Novel PWM Schemes**". This is a true copy of the dissertation, including any required final revisions, as accepted by my examiners.

I understand that my dissertation may be made electronically available to the public.

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Abstract

Recently, there are growing demand for power converters with high power density, reliability, and performance-to-size ratio, mainly in electrical automobiles, grids with renewable energy integration, and robotic systems. Moreover, with the growing demand for less distorted ac voltage, improved inverter efficiency, lower withstand voltage, and reduced filter size in high-power applications, multilevel inverters (MLIs) have emerged as an alternative to two-level inverters. Unfortunately, most of these MLIs include many switching devices and bulky capacitors, and many require complex control algorithms. The increased weight, cost, and limited reliability of these MLIs have hindered their industrial practicality.

The hybrid inverter topology (a case under study in this dissertation) constructed with the neutral-point clamped (NPC) and H-bridge structures has proven its superiority among the most popular MLI topologies because it requires few power devices and achieves high efficiency. However, this inverter requires bulky passive components, such as dc-link capacitors and filter inductors, and is challenged by complex algorithms to balance the capacitor voltage.

First, this thesis analyzes a two-stage single-phase hybrid multilevel dc-link (MLDCL) inverter, in which a dc-link with two capacitors is integrated into a single dc source. When controlled under the conventional modulation scheme, the MLDCL inverter synthesizes a five-level output voltage. As the capacitor-voltage balancing depends on the fundamental period, the output voltage may contain unsolicited low-order harmonics. Moreover, in the conventional scheme, this inverter requires large dc-link capacitors.

Next, to avoid the aforementioned problems, the present dissertation develops two simple modulation schemes based on redundant switching states, which control the MLDCL inverter and balance the capacitor voltage within each carrier period. The first proposed scheme is developed based on multi-carriers phase-shifted pulse-width modulation, while the second scheme is constructed based on a single carrier multi-modulation with quasi-reference voltages. The proposed modulation schemes reduce the dc-link capacitance by a factor of the frequency modulation ratio while reducing the total harmonic distortion of the output voltage and current. The reduction of the dc-link capacitance not only increases the power density but also reduces the cost and physical size of the inverter. Unlike the conventional method, the proposed schemes considerably reduce the capacitor-voltage ripples and can be regulated by increasing the carrier frequency, thereby reducing the voltage stress on the switching devices, and improving the reliability of the inverter. The feasibility of the proposed schemes over the conventional scheme is confirmed in a comparative study. Finally, the steady-state and dynamic performances of the proposed strategies are demonstrated in simulations and validated in experiments.

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"I can do all things through Him who strengthens me." Philippians 4:13

Dedication

First, I am dedicating this dissertation work to two beloved people who have meant and continue to mean so much to me even if they are no longer of this world. They are my father, Peter Kahwa, and mother, Agripina Kahwa, who was my inspiration during my doctoral studies, but she could not wait for three months to see me making this submission. You taught me the value of hard work and kindness. Thank you so much.
Second, I dedicate this work to the one I love, my family, and many friends. A special feeling of gratitude to my loving son, Alvin.

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Chapter 1

Introduction

1.1 Background

Due to the continuous increase in demand for power converters with high power density, reliability, and performance-to-size ratio, mainly in electrical automobiles, renewable energy integration systems, and robotic systems, the power converters with reduced passive components, switching devices, and direct current (DC) voltage sources have gained high interests [1], [2]. In the past, the dc voltage, such as the one from the battery, photovoltaic system, and fuel cell, was converted to alternating current (AC) voltage by using two-level inverters. Fig. 1.1 displays the schematic of the typical DC/AC power converter stage for grid-connected and stand-alone applications. In the two-level inverters, each semiconductor device withstands a total dc source voltage, consequently limiting its applications in medium-/high-voltage applications. Moreover, these inverters are susceptible to high dv/dt values and total harmonic distortion (THD) [3].

With the growing demand for less distorted ac voltage, improved inverter efficiency, lower withstand voltage, reduced filter size, and improved electromagnetic compatibility in high-power applications, multilevel inverters (MLIs) have emerged as an alternative to two-level inverters [4]− [7]. Unlike two-level inverters, MLIs can generate smoother ac voltage when the number of output voltage steps are increased using several semiconductor devices, capacitors, and small dc voltage as input [8]− [16]. However, having high numbers of voltage levels leads to complexity in the control algorithm and introduces voltage imbalance problems. The MLI topologies may include the filter circuits to reduce the harmonics in their outputs [15], [16]. Although, large filters increase the weight, size, and cost of the inverter. Thus, the trade-off among the efficiency, sizes, output waveform purity, costs, and weight of the passive and switching components of the inverter must be carefully studied.

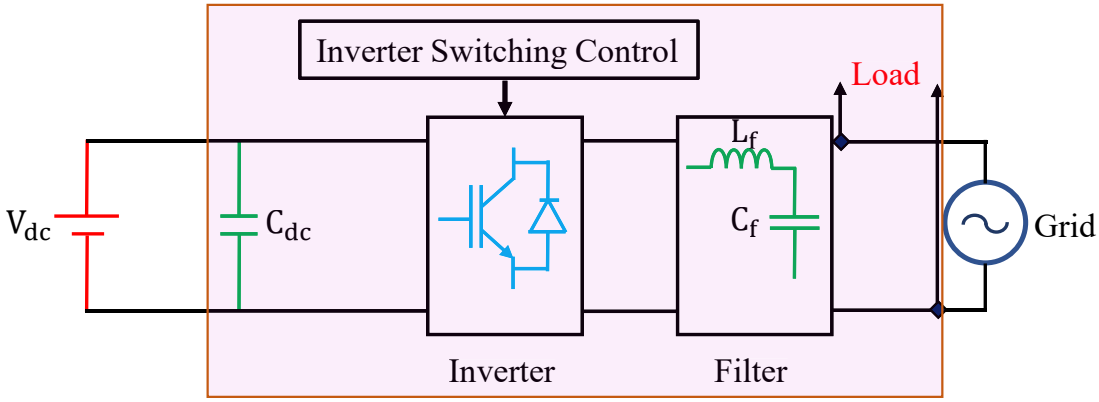


Figure 1.1: DC/AC power converter stage with *LC* filter for grid-connected and stand-alone applications.

1.1.1 Conventional Multilevel Inverters

Among the existing MLI topologies, the flying capacitor (FC), cascaded H-bridge (CHB), and neutral-point clamped (NPC) inverters are the major MLIs that have found their breakthrough into industrial applications [5]. It is worth mentioning that the hybrid inverter topology studied in this thesis was constructed with the NPC and H-bridge structures.

Flying Capacitor Multilevel Inverter

The single-phase FC inverter is one of the classical MLIs which was introduced for medium-voltage multilevel power conversion applications [17]– [19]. It is constructed with an inward nested series connection of capacitors, which clamp the voltage across switching devices to one capacitor voltage value (see Fig. 1.2). Figs. 1.2a and 1.2b display the single-phase 3-level and 5-level FC inverters, constructed with four and eight controlled-switching devices, respectively. The generated voltage levels in the FC inverter can be extended to higher levels. In this topology, for n number of generated voltage levels, $(n-1)$ dc-link capacitors, $\frac{(n-1)(n-2)}{2}$ floating capacitors, and $2(n-1)$ controlled-switching devices are required. One of the advantages of this topology is that it has switching redundancies. The availability of redundant switching states plays a vital role when balancing the capacitor voltages. However, in some applications, the FC inverter is challenged by capacitor voltage balancing control complexity and cannot pre-charge the capacitors [20]– [22]. Moreover, this inverter requires many bulky capacitors and controlled-switching devices as the voltage levels increase, which reduces the power density of the inverter, thereby limiting its industrial practicality.

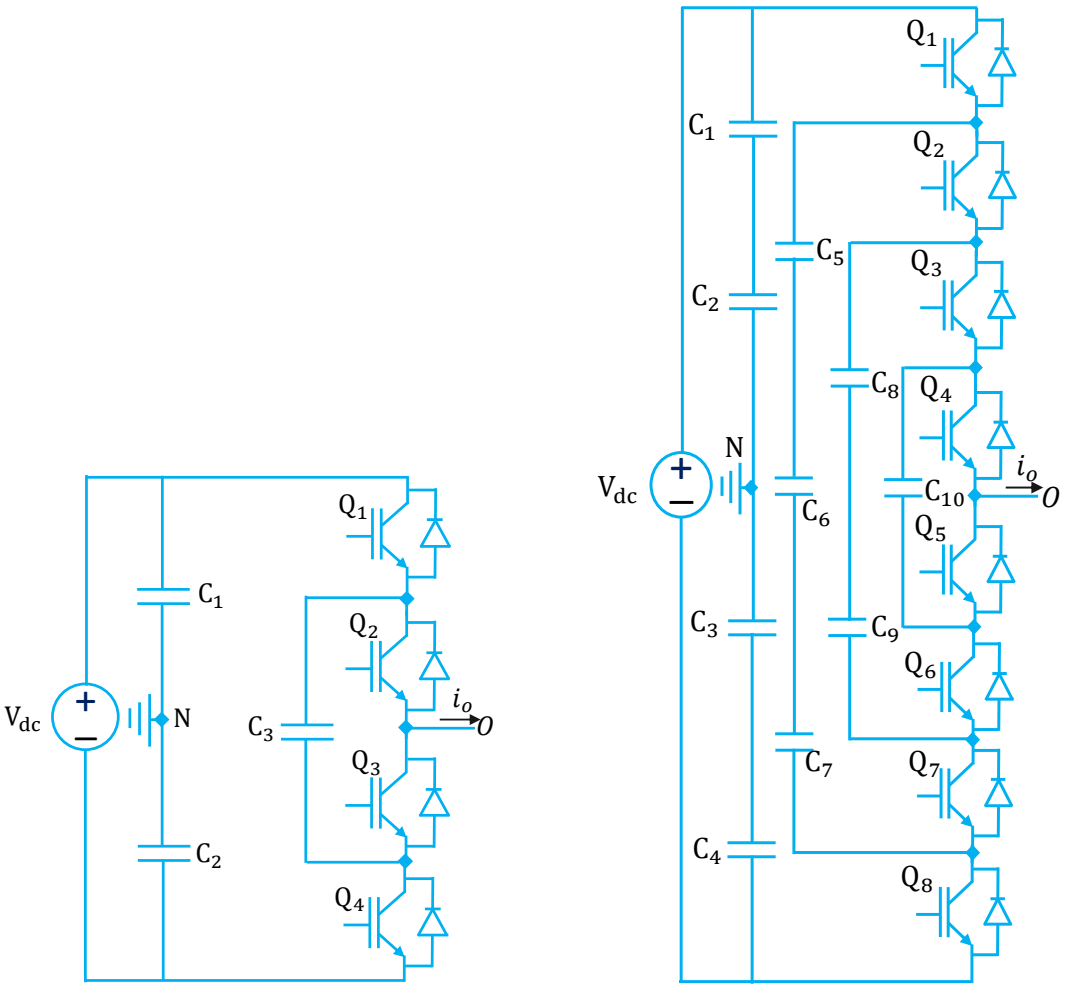


Figure 1.2: Single-phase flying capacitor multilevel inverters: (a) 3-level topology and (b) 5-level topology.

Cascaded H-bridge Multilevel Inverter

The CHB inverter is another classical MLI topology that found a breakthrough in industrial medium-voltage application [19]. The CHB inverter is constructed with the series connection of several single-phase H-bridge inverter modules (see Fig. 1.3). Fig. 1.3a shows a single-phase 3-level H-bridge inverter module. The H-bridge module integrates the dc-link with a single independent dc voltage source and consists of four controlled-switching devices in its structure.

Fig. 1.3b shows a single-phase 5-level cascaded H-bridge MLI. It is constructed with two H-bridge modules connected in series, in which each module has an isolated dc voltage

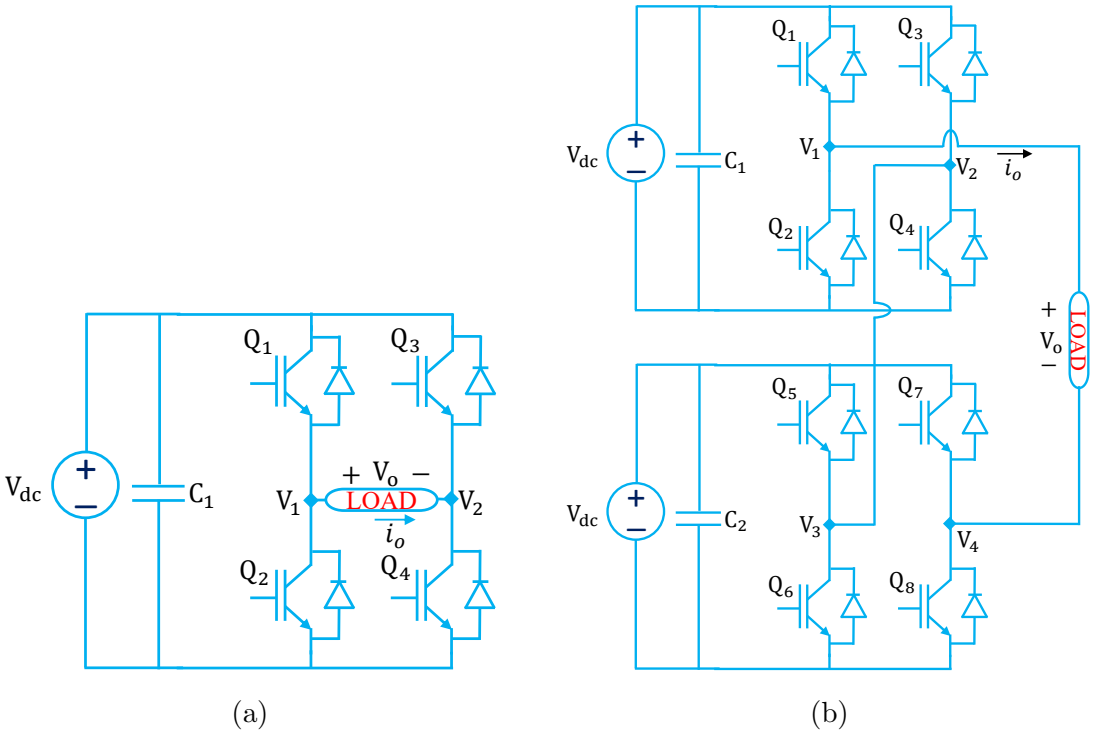


Figure 1.3: Single-phase H-bridge multilevel inverters: (a) 3-level topology and (b) 5-level cascaded H-bridge topology.

source. Unlike the FC inverter, for n number of generated voltage levels, $\frac{(n-1)}{2}$ dc-link capacitors and $2(n-1)$ controlled-switching devices are required in the CHB inverter. The CHB inverter has proven to be superior even among the classical inverter topologies by achieving high efficiency, having a modest circuit, and few power devices [23], [24]. Moreover, unlike FC and NPC inverters, the CHB is well known for high-power applications because of its modular structure and perfect utilization of the dc-link voltage source. On the downside, the CHB inverter requires many isolated dc voltage sources, which hinders its industrial applications. In an effort to minimize the number of isolated dc sources in the CHB inverter, a cascaded seven-level inverter, powered by a single dc source incorporating the switched-capacitor technique, was presented in [25]. This topology replaces all isolated dc sources with capacitors, keeping a single dc supply voltage connected to one H-bridge module, and includes two charging controlled-switches so that the capacitor charging time does not depend on the load. However, due to power loss in the capacitor charging circuit, low power efficiency is achieved compared to the CHB topology. An improved topology to eliminate the capacitor-charging circuit was proposed in [26]. However, these improvements demand a complex control algorithm to balance the capacitor voltage.

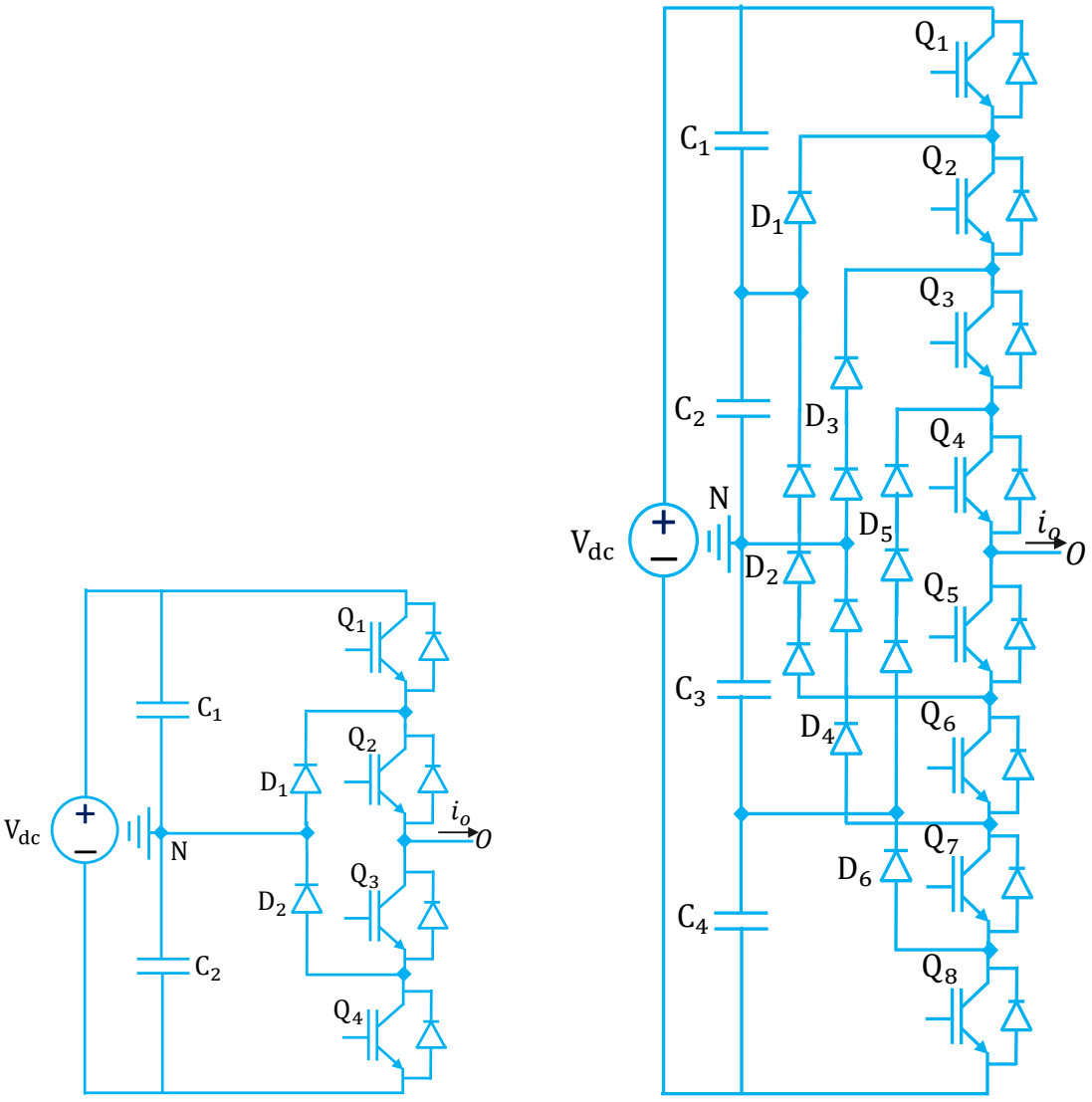


Figure 1.4: Single-phase neutral-point clamped multilevel inverters: (a) 3-level topology and (b) 5-level topology.

Neutral-Point Clamped Multilevel Inverter

The single-phase NPC inverter topology displayed in Fig. 1.4 is the first practical MLI that found a breakthrough in industrial application [3], [27]. When compared to FC inverter, the clamping diodes in the NPC inverter replace the flying capacitors. These diodes clamp the voltages of the controlled-switching devices to one capacitor voltage value, thereby ensuring low voltage stress on the switching devices [27], [28]. Fig. 1.4a shows the 3-level NPC inverter which integrates a dc-link with two series-connected capacitors C_1 and C_2.

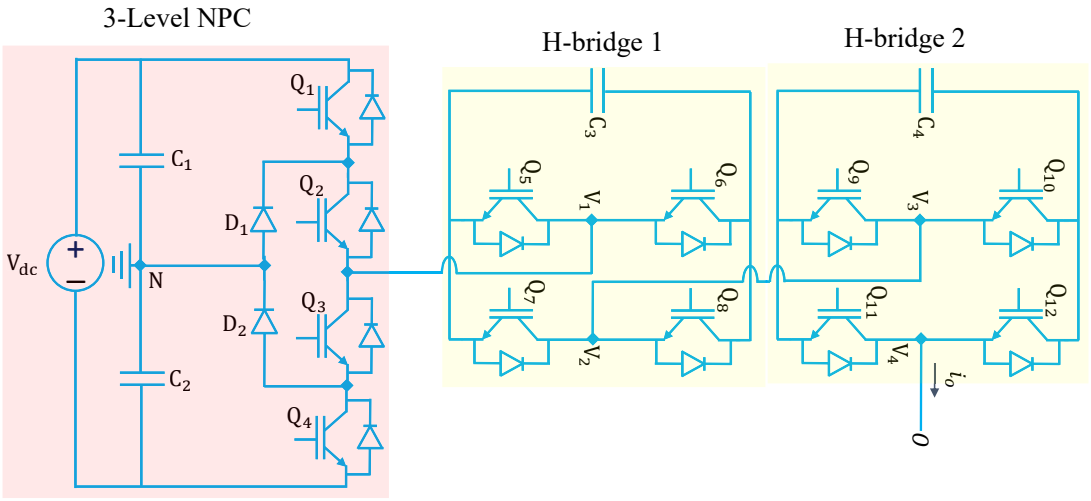


Figure 1.5: Single-phase NPC-CHB hybrid multilevel inverter.

Fig. 1.4b shows the 5-level NPC inverter and can be extended to a higher number of levels. In this topology, $(n-1)$ dc-link capacitors, $(n-1)(n-2)$ clamping diodes, and $2(n-1)$ controlled-switching devices are required. On the downside, the NPC inverter is less attractive at higher voltage levels because of high power losses and the capacitor-voltage imbalance problems. In the NPC-based inverters, large electrolytic dc-link capacitors are often required to improve the power quality and reduce the capacitor voltage ripples of the inverter. Moreover, this inverter has poor utilization of the dc source voltage because the maximum output ac voltage is one-half of the dc-link supply voltage.

1.1.2 Hybrid Multilevel Inverters

Many recently developed inverters were proposed to improve the design and control of inverters due to the drawbacks of the conventional MLIs. Among the widely studied technique is the construction of hybrid inverters, which utilize advantageous features of conventional inverters to achieve desired performance in a particular application [29]– [40]. The hybrid MLIs are constructed with combination of two or even just part of conventional and/or non-conventional inverter topologies. One of the hybrid inverter topologies which gained the attention of researchers is the NPC-CHB (a hybrid of 3-level NPC and H-bridge structures connected in series) inverter (see Fig. 1.5) [29]– [31]. This inverter eliminates the demand for several isolated voltage sources for H-bridge modules. However, the voltage balancing control for floating capacitors is highly required, consequently introducing complexity to the control system. Moreover, this inverter requires many controlled-switching devices and gate drive circuits.

The development of new MLI topologies with reduced numbers of switching devices, gate drive circuits, and low withstand voltage across the switches is an ongoing trend [34]− [40]. The authors of [34] proposed the 6-level inverter integrating the 3-level FC and two 2-level inverters structures, which minimizes the number of isolated dc sources, controlled-switching devices, and gate drive circuits. The authors of [35]− [37] proposed the two-stage (level-generation and polarity-generation stages) MLIs incorporating basic units with reduced controlled-switching devices. However, these inverters require isolated dc voltage sources and bulky dc-link capacitors. Moreover, the capacitor-voltage balancing in these inverters is realized using either multi-tap transformers or isolated dc-dc converters, consequently increasing the physical size, weight, and cost of the inverter. In an attempt to reduce the number of isolated dc sources, the two-stage hybrid (a hybrid of NPC and H-bridge structures) multilevel dc-link (MLDCL) inverter using a single dc source integrating a dc-link with two capacitors was proposed in [38]. The MLDCL inverter can achieve high efficiency, although it requires eight controlled-switching devices to generate an output voltage with five levels. An improved single-phase 5-level hybrid MLDCL inverter topology constructed with only six controlled-switching devices, two power diodes, and a single dc source was proposed in [39], [40]. When compared to the inverter in [38], this inverter reduces the number of controlled-switching devices and gate drive circuits by half in the level generation stage. However, when designing new MLIs, research has focused on reducing the number of switching devices in MLIs. Less attention has been devoted to minimizing the sizes of the passive components, such as the dc-link capacitors, floating voltage sources, and inductor filters. Bulky passive components increase the weight and size of the inverter, thereby reducing its power density. A feasible solution to reduce the passive components in the MLIs is by employing proper modulation and control schemes for the specific inverter.

1.1.3 Traditional Modulation Strategies for Multilevel Inverters

The modulation strategies for the MLIs are mainly categorized according to the applied switching frequency: the fundamental switching frequency and high-switching frequency modulation strategies [41].

Fundamental Switching Frequency Modulation Strategies

The well-known low-frequency modulation techniques for MLIs are the space vector control [41], selective harmonic elimination (SHE) [42], synchronous optimal PWM (SOP) [43], and the nearest level control [44]. The low-switching frequency modulation schemes reduce the

overall switching loss of the inverter. However, these modulation techniques increase the harmonic distortion of the output voltage and current [45]. Also, in these techniques, bulky passive components, such as dc-link capacitors, are required, and the dynamic performance of the inverter is degraded.

High-Switching Frequency Modulation Strategies

The widely studied high-switching frequency modulation techniques are the space vector PWM (SVPWM) and carrier-based sinusoidal PWM (SPWM). The SVPWM scheme provides high power-quality performance of the inverter and ensures flexible and more control freedom when selecting vectors for generating the switching signals [46]. On the downside, when compared to the SPWM, the SVPWM demands high control complexity and computational burden [46], [47]. The SPWM scheme is simple to implement by simply comparing the reference signal with carrier signals.

The well-known classic SPWM multi-carriers-based techniques in industrial multilevel power conversion applications are level-shifted PWM (LS-PWM) and phase-shifted PWM (PS-PWM) schemes. The PS-PWM scheme is superior among the high-frequency switching modulation techniques because of its capability to improve the dynamic control performance of the inverter and equal distribution of power loss among the switching devices [19], [48], [49].

1.2 Motivation

Fig. 1.6 displays the survey of failure distribution among the reliability-critical components in power electronics system [50]. Notably, the semiconductor devices and capacitors contribute more than one-half of the total failure in the system. Failures in semiconductor devices and capacitors may occur due to overcurrent and overvoltage. The latter cause is investigated in this work to reduce the voltage stress on the switching devices and dc-link capacitors by reducing the capacitor-voltage ripple.

Moreover, most of the established MLIs generate many voltage levels to reduce the number of harmonics in the generated voltage and current [15]. Unfortunately, most of these MLIs include many switching devices and bulky capacitors, and many require complex control algorithms. The increased weight, cost, and limited reliability of these MLIs have hindered their industrial practicality [16]. Reducing the sizes and numbers of the passive and electronic components in MLIs with high power density is an ongoing trend [2], [14]− [16]. However, research has focused on reducing the number of switching

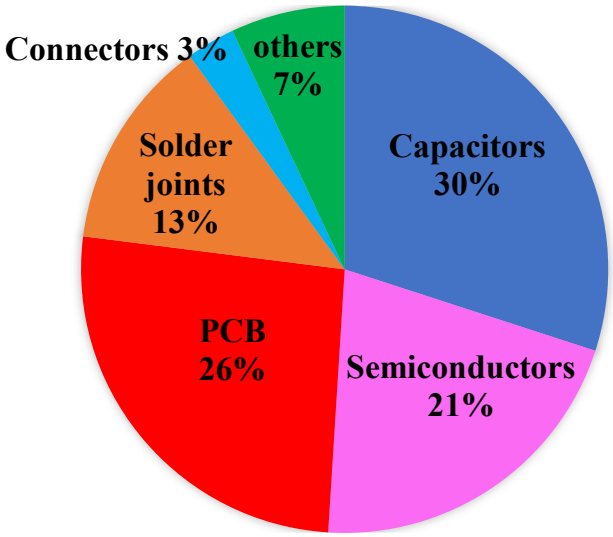


Figure 1.6: Failure distribution among reliability-critical components in the power electronics system [50]

devices in single-phase MLIs. Less attention has been devoted to minimizing the sizes of the passive components, such as the dc-link capacitors, floating voltage sources, and inductor filters. This study attempts to minimize the size of dc-link capacitors and improve the overall performance of a two-stage single-phase 5-level hybrid multilevel dc-link (MLDCL) inverter.

1.3 Research Objectives

The main focus of this work is to:

- Develop the PWM schemes to control the single-phase 5-level hybrid MLDCL inverter and balance the dc-link capacitor voltages with reduced control complexity.
- Reduce the dc-link capacitance of the single-phase 5-level hybrid MLDCL inverter with the modulation technique.
- Design and estimate the dc-link capacitors and LC filter under the proposed modulation schemes.
- Conduct a detailed performance comparison study of the conventional and proposed modulation schemes for the 5-level hybrid MLDCL inverter.
- Perform a detailed thermal analysis and power loss estimation of the single-phase 5-level hybrid MLDCL inverter.

1.4 Research Contributions

The key contributions of this work are:

- Two novel simple modulation schemes were developed based on redundant switching states, which control the MLDCL inverter and balance the capacitor voltage within each carrier period. The first proposed scheme is developed based on multi-carriers phase-shifted pulse-width modulation, while the second scheme is constructed based on a single carrier multi-modulation with quasi-reference voltages. After applying the proposed modulation schemes, the single-phase 5-level hybrid MLDCL inverter was improved in the following ways:
  - The dc-link capacitance was reduced by a factor of the frequency modulation ratio.
  - The THDs of the output voltage and current were considerably reduced.
  - The capacitor-voltage ripple was considerably reduced and can be regulated by adjusting the carrier frequency.
  - The dynamic performance of the 5-level hybrid MLDCL inverter was improved during sudden load changes and start-up of the inverter.
- Detailed theoretical, simulations, and experiments studies, were carried out to demonstrate the performance improvement of the single-phase 5-level hybrid MLDCL inverter when the proposed modulation schemes are applied.

1.5 Thesis Outlines

This Doctoral thesis is organized as follows:-

- Chapter 1:- Introduces the background, motivation, research objectives, research contributions, and outlines of the research work presented in this thesis .
- Chapter 2:- Presents the derivation of the multilevel dc-link inverters and hybrid multilevel dc-link inverters with a reduced number of controlled-switching devices. Also, it presents a brief discussion of the existing dc-link voltage balancing schemes for NPC-based inverters and their drawbacks. The detailed operating principles of the single-phase 5-level hybrid MLDCL inverter also are presented. .

- Chapter 3:- The main objective of this research begins in this chapter. It presents the novel PWM schemes for the single phase 5-level hybrid MLDCL inverter and the capacitor-voltage balancing. Moreover, it presents the detailed simulation and experimental investigations of the proposed modulation techniques.

- Chapter 4:- Presents step by step design of the dc-link capacitors, LC filter circuit and a comparative performance study of the analyzed modulation methods. Also, it presents the case study of non-unity power factors operation of the hybrid MLDCL inverter.

- Chapter 5:- In this chapter, the thermal analysis and power loss estimation are performed. Also, a comparative study of the conventional and proposed modulation schemes is conducted.

- Chapter 6:- Presents the conclusion and future perspective of this research work.

Results were obtained, analyzed, and summarized from Chapter 3 to Chapter 5.

Chapter 2

Multilevel DC-Link Inverters

This chapter describes the derivation of the multilevel dc-link inverters and hybrid multilevel dc-link inverters with a reduced number of controlled-switching devices. Additionally, it presents a state-of-the-art overview of the existing dc-link voltage balancing schemes and voltage ripple reduction for NPC-based converters and their drawbacks. Next, the operating principles of the single-phase 5-level hybrid MLDCL inverter are deduced and discussed in detail. Finally, the prototype of the single-phase 5-level hybrid MLDCL inverter was constructed and presented in this chapter.

2.1 Derivation of Multilevel DC-Link Inverters

The multilevel dc-link inverter (MLDCL) with the H-bridge module was proposed to reduce the number of switches, clamping diodes, and capacitors in the conventional MLIs [51]. An MLDCL inverter can be constructed with the flying-capacitor, neutral-point clamped or cascaded half-bridges structures integrating a H-bridge module (see Fig. 2.1 and 2.2). This inverter generates an output voltage with a unity voltage gain attributed to the use of the H-bridge module.

Fig. 2.1a shows the two-stage single-phase 5-level MLDCL inverter constructed with the 3-level FC and H-bridge structures. The first stage of this inverter is the level-generation stage (with four IGBTs ($Q_5 - Q_8$) and one floating capacitor C_3), which generates the stepped dc voltage, and the second stage is the polarity-generation stage. The polarity-generation stage consists of the conventional H-bridge module using four IGBTs ($Q_1 - Q_4$).

Fig. 2.1b shows the two-stage single-phase 5-level MLDCL inverter constructed with the 3-level NPC and H-bridge structures. The first stage of this inverter is the level-generation stage (with four IGBTs ($Q_5 - Q_8$) and two clamping diodes D_1 and D_2), which generates

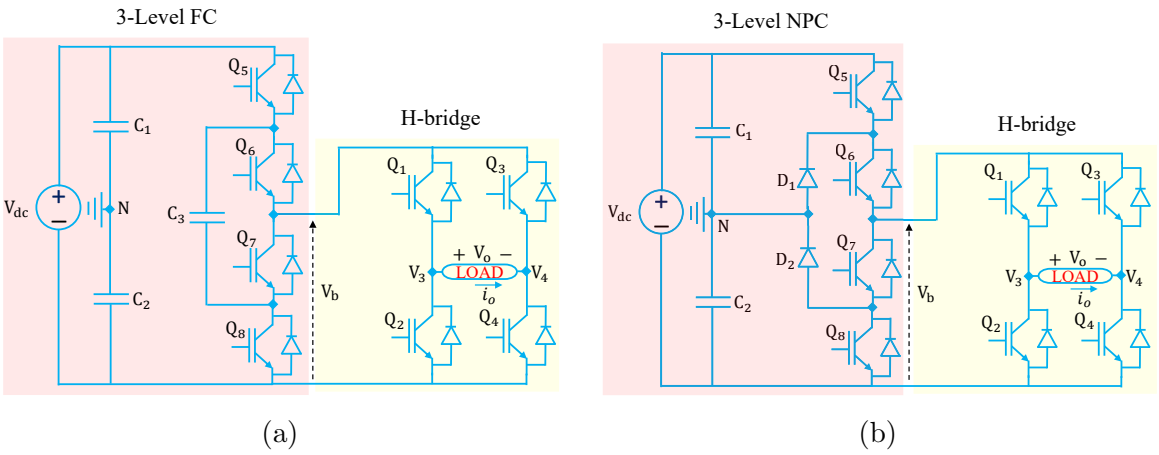


Figure 2.1: Single-phase 5-level MLDCL inverters: (a) FC-based with H-bridge module and (b) NPC-based with H-bridge module.

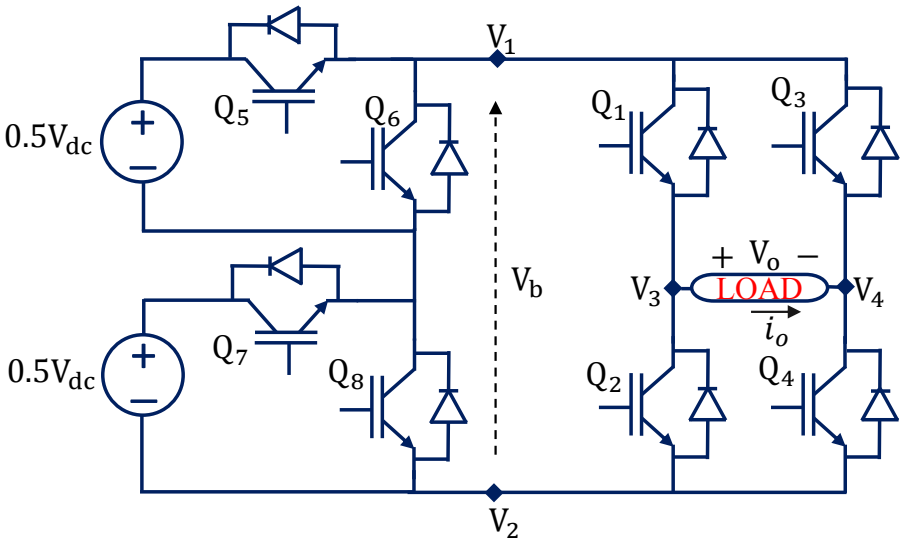


Figure 2.2: Cascaded Half-bridge-based single-phase 5-level MLDCL inverter.

the stepped dc voltage. The second stage is constructed with the H-bridge module for generating the bipolar voltage at the load. The hybrid MLDCL inverter under study in this research work derives from the cascaded half-bridge module with independent dc voltage sources, as discussed in Section 2.1.1.

2.1.1 A Cascaded Half-bridges-Based MLDCL Inverter

The two-stage single-phase 5-level hybrid MLDCL inverter derives from the generalized two-stage inverter topology presented in [51]. Its name reflects its two-stage architecture:

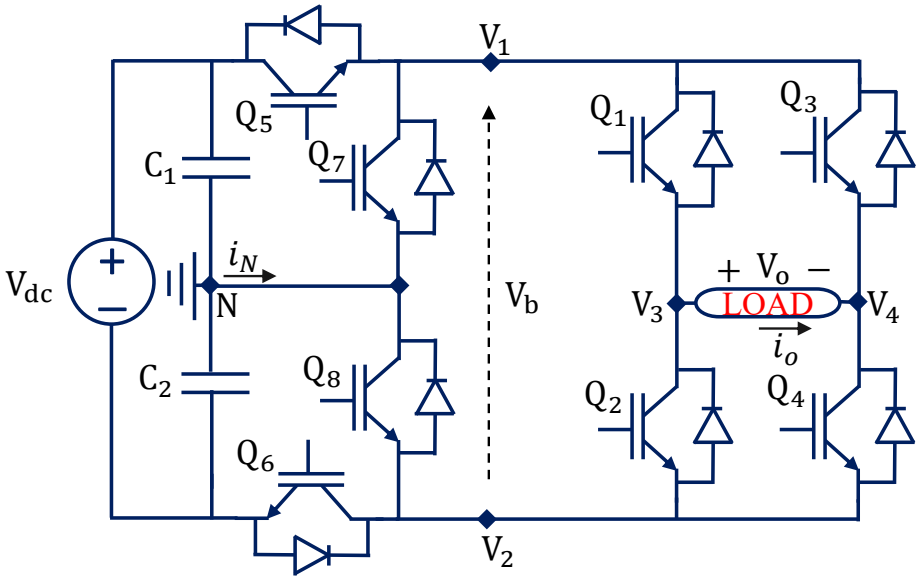


Figure 2.3: Circuit diagram of the single-phase 5-level hybrid MLDCL inverter (H8 topology).

cascaded half-bridges with independent dc voltage sources and an H-bridge unit (Fig. 2.2). To generate five voltage levels with magnitudes of $-V_{dc}$, $-\frac{V_{dc}}{2}$, 0, $\frac{V_{dc}}{2}$, and V_{dc}, the MLDCL inverter topology uses eight controlled-switching devices and two independent dc sources, each of magnitude $\frac{V_{dc}}{2}$ [52], [53]. The MLDCL inverter is easily controlled due to its modular structure and can achieve very high efficiency. On the downside, it includes many isolated dc power sources and switching devices.

2.1.2 A Single-Phase 5-Level Hybrid MLDCL Inverter

By cascading the main modules and integrating a dc-link with two capacitors and a single dc source, the MLI topology that enables four-quadrant operation minimizes the number of independent dc sources in the MLDCL inverter (see Fig. 2.3) [38]. Moreover, the authors of [38] proposed a modulation strategy based on phase-shifted pulse-width modulation (PS-PWM), which balances the dc-link capacitor voltage during the fundamental period. However, the large capacitor (1000 μF) in their study increased the physical size, cost, and weight of the inverter.

As an improvement to the 5-level hybrid MLDCL inverter (H8 topology), the authors of [39] and [40] proposed a two-stage single-phase 5-level hybrid (a hybrid of neutral-point-clamped (NPC) and H-bridge structures) MLDCL inverter with only six controlled-switching devices, two power diodes, and a single dc source integrating a dc-link with two capacitors. The topology shown in Fig. 2.4 is designed to operate at a unity power factor,

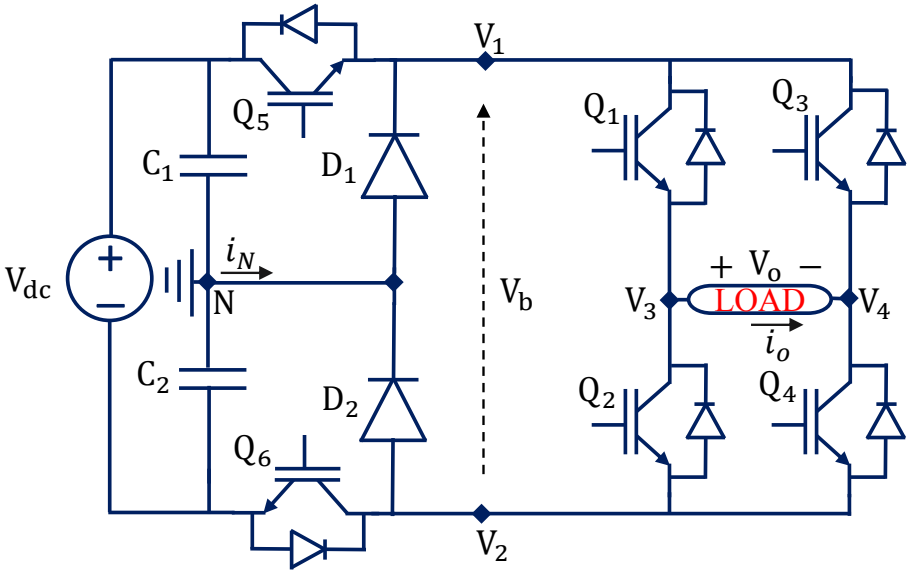


Figure 2.4: Circuit diagram of the single-phase 5-level hybrid multilevel dc link (MLDCL) inverter.

such as in grid-connected and stand-alone applications in which unity power operations are recommended. At non-unity power factors, the power diodes D_1 and D_2 tend to block the reverse inductive current, which causes a voltage spike at the zero-voltage level [39, 54]. The voltage spike reduces the reliability of the inverter and increases the voltage distortion. However, if the voltage drop across the inductive load causes a small shift of the power factor from unity, the inverter operation is unaffected. The working principle of this 5-level hybrid inverter was analyzed in the above scenario, but a 3-level inverter with the same topology (H6D2) admits power factors other than unity and generates a constant common-mode voltage with high efficiency and a low output current ripple [55]. In this work, both H8 (Fig. 2.3) and H6D2 (Fig. 2.4) topologies operated to generate five voltage levels, are analyzed and their advantages and disadvantage are highlighted. Notably, the H8 topology was analyzed for the case of non-unity power factor operations when demonstrating additional advantages of the proposed modulation schemes.

To improve the total harmonic distortion (THD) of the generated output voltage, the authors of [39] proposed a 5-level solution to the H6D2 inverter and its conventional modulation scheme based on level-shifted PWM (LS-PWM). The conventional PWM method reduces the switching loss in the inverter. A complex and sensor-based voltage-balancing scheme that depends on the fundamental period of the voltage also was established in [39]. This scheme uses a proportional-integral (PI) controller and acknowledges that the additional voltage levels are obtained from the charging/discharging of the dc-link capacitors. However, the conventional method cannot regulate the voltage ripple in the capacitors un-

der heavy loading. High voltage ripple reduces the overall reliability of the inverter and can even break the switching devices. Moreover, as the capacitor-voltage balance depends on the fundamental frequency, the generated output voltage may contain unsolicited low-order harmonics, and the inverter requires bulky electrolytic capacitors. Low-order harmonics degrade the power quality, and the bulky capacitors increase the cost and weight of the inverter. In the present thesis, the conventional method in [39] is adopted as the benchmark for comparison with the proposed modulation strategies. Other PWM methods that depend on the fundamental frequency similarly cannot reduce the dc-link capacitance, voltage ripple, and THD of the voltage generated by a 5-level hybrid MLDCL inverter [56], [57].

2.2 State-of-the-Art Overview of the DC-Link Voltage Balancing for NPC-Based Inverters

DC-link capacitor-voltage balancing is an ongoing challenge for the proper operation of NPC-based converters. The authors of [58] presented the dc-link voltage balancing scheme that uses a standard PWM modulator with an objective function that is optimized to reduce the switching losses in the inverter. Because the proposed scheme adopted the standard PWM modulator, high capacitor voltage ripples are experienced and bulky capacitors are required in [58]. The authors of [59] and [60] presented carrier-based PWM schemes to balance the dc-link capacitor voltages in a single-phase converter. The authors of [59] injected an offset voltage in the reference voltage that depends on the differential voltage of the two capacitors, whereas the authors of [60] injected a differential voltage of the dc source and modified grid voltage. In [59], by maximizing the offset voltage, voltage balancing achieved a fast dynamic response with reduced switching loss. In addition, the authors of [61] presented model-predictive controllers that guarantee a fast dynamic response in balancing the capacitor voltages through a cost function with weighting factors. The drawback of these schemes is that they are complex and include many measurements, and the capacitor-voltage ripples depend on the low-fundamental frequency component. Moreover, the bulky capacitors (4400 [59], 8800 [60], and 1000 μF [61]) in their studies increased the weight, cost, and physical size of the inverter. The author of [62] presented an auxiliary resistive–inductive–capacitive (RLC) balancing circuit that naturally balances the capacitor voltages without any measurements. The RLC circuit ensures a fast response in balancing the capacitor voltages; however, this technique increases the weight, cost, and power loss, thereby reducing the efficiency of the inverter by 1%. Thus, minimizing the dc-link capacitance and the complexity to balance the capacitor voltages remains necessary.

Modulation schemes that reduce the capacitor size are well-known in some MLI topolo-

gies. The examples are the open-loop control [63], and the closed-loop control with a proportional controller [64], which use PS-PWM to reduce capacitor size of flying-capacitor based MLI. The authors of [65] presented an open-loop sensor-less modulation strategy based on LS-PWM, which minimizes the capacitor size in a 5-level packed U-cell (PUC5) converter. In these schemes, the low-fundamental frequency component was eliminated in the voltage ripple of the flying capacitor, thereby reducing the capacitor voltage ripple.

2.2.1 An Overview of the Strategies for Reducing the DC-Link Voltage Ripple

The dc-link capacitor size depends on the capacitor voltage ripple, frequency, and operating peak current. Modulation techniques attempting to reduce the capacitor voltage ripple and thereby reducing the dc-link capacitance are in continuous demand because of the high demand for high performance-to-size ratio, cost-effectiveness, reliability, and power density of the inverter. Several techniques have been proposed for three-phase 3-level (3L) NPC-based and T-type converters. The authors of [66] proposed the SVPWM strategy for NPC converter that reduces the switching loss and capacitor voltage ripple. The proposed strategy eliminated the low-fundamental frequency components of the capacitor voltage during the operation of the converter in the full range of power factors (PFs) [66]. However, this strategy is complex, requires many measurements that exert a high computational burden, and increases the THD of output voltage. The authors of [67] proposed the nearest-vector SVPWM strategy and the hybrid SVPWM strategy in [68]. Both strategies reduce the low-fundamental frequency component of the capacitor voltages and THD of the output voltage of the NPC inverter [67], [68]. On the downside, these strategies can only eliminate the low-fundamental frequency component of the capacitor voltage at high PFs above 0.5 and operate similarly to the conventional strategy at low PFs. Moreover, these schemes are complex and require many measurements. The authors of [69] proposed the LS-PWM-based strategy to reduce the low-fundamental frequency voltage oscillations by injecting the optimal compensation values in the phase-reference voltages. The proposed scheme eliminates the low-fundamental frequency voltage oscillations at high PF and specific low modulation index [69]. For example, when the PF decreases below 0.6 and the modulation index is higher than 0.7, this strategy does not eliminate the low-frequency voltage ripple. Moreover, the proposed strategy in [69] slightly increases the THD of the output voltage and requires phase and neutral-point current measurements, thereby increasing the control complexity. Similarly, the authors of [70] presented the SVPWM scheme to reduce the low-frequency dc-link capacitor voltage oscillation in the 3L-NPC/T-type inverter by injecting the time offsets in the phase-reference voltages. In this approach, the low-fundamental

frequency component of the capacitor voltage remains and is higher at low PFs close to zero [70]. Additionally, this scheme increases the THD of the output voltage and requires a complex control algorithm. The authors of [71] proposed a hybrid (LS-PWM and PS-PWM) modulation strategy for a 5L-FCNPC converter to reduce the dc-link capacitor voltage ripple by injecting the compensation value. This strategy considerably reduces the dc-link capacitor voltage ripple and THD of the output voltage at unity power factor despite increasing the equivalent switching frequency to three times the carrier frequency [71]. On the downside, this scheme increases the switching loss, and the low-frequency voltage oscillations remain. Thus, except for the modulation strategy in [66], the bulky dc-link capacitors are required when the above strategies are implemented in applications when the full range of power factors is recommended because these schemes can partially eliminate the low-fundamental frequency voltage oscillations. Also, it is worth mentioning that the reduction of the dc-link voltage ripple has been well-studied in three-phase converters, but only a few studies for the single-phase converters.

The authors of [72] and [73] proposed the simple carrier-based PWM strategy to reduce the dc-link voltage ripple in the single-phase T-type inverter. The proposed scheme reduces the capacitor voltage ripple by swapping the quarter-wave switching sequence from the conventional LS-PWM, and it achieves power loss balance among the switching devices. However, the low-frequency component of the capacitor voltage remains. Thus, the bulky dc-link capacitors remain necessary when this scheme is applied.

To improve the power-density, reliability, and overall performance while reducing the physical size and cost of the 5-level hybrid MLDCL inverter, this thesis proposes two simple modulation strategies based on redundant switching states. The proposed modulation schemes controls the inverter and balance the dc-link capacitor voltage during each carrier cycle. The presented modulation schemes moderately regulate the duty cycles associated with the switching devices in the level-generation stage, eliminating the demand for a complex control algorithm.

2.3 Description and Analysis of the Single-Phase 5-Level Hybrid MLDCL Inverter

2.3.1 Description of the Inverter Topology

The two-stage single-phase 5-level hybrid MLDCL inverter requires only six controlled-switching devices: six insulated-gate bipolar transistors (IGBTs) and two power diodes

(see Fig. 2.4). The inverter is powered by a single constant dc source of magnitude V_{dc} that integrates the dc-link split by two series-connected capacitors, C_1 and C_2. The mid-point N of the two capacitors is a neutral-potential point. Each capacitor maintains an average voltage of approximately one-half the dc source voltage, i.e., $\frac{V_{dc}}{2}$ in a balanced and optimal dc-link. The current i_N flows to and from the neutral-potential point.

Fig. 2.4 depicts the hybrid inverter with a level-generation stage and a polarity-generation stage. In the level-generation stage, two IGBTs (Q_5 and Q_6), and two power diodes (D_1 and D_2) are connected to a dc-link. The polarity-generation stage consists of the conventional H-bridge module using four IGBTs (Q_1–Q_4). The output voltage waveform V_b before the H-bridge in the level-generation stage is the stepped dc voltage with three levels (0, $\frac{V_{dc}}{2}$, and V_{dc}) of unipolar voltages. At the H-bridge, the three-level unipolar voltage waveform is converted into a stepped ac voltage waveform across the load V_o, which has five levels ($-V_{dc}$, $-\frac{V_{dc}}{2}$, 0, $\frac{V_{dc}}{2}$, and V_{dc}) of bipolar voltages. Therefore, the stepped dc voltage V_b is related to the stepped ac voltage across the load V_o as

$$V_b = |V_o|. \tag{2.1}$$

The controlled-switching devices of the H-bridge module can be operated at the fundamental frequency or a higher frequency depending on the desired switching loss and harmonic content [38, 51, 52]. In [39] and the proposed schemes in this article, the IGBTs Q_1 and Q_4, and Q_2 and Q_3 in the H-bridge module are operated as complementary pairs at the fundamental frequency (f_o) over half a period of the output voltage and are switched OFF during the remaining half period (see Table 2.1). Operating the H-bridge module at f_o reduces the switching loss in the inverter. The switching devices in the level-generation stage are operated at high frequency to achieve the desired harmonic content. Thus, this topology can mitigate both the switching losses and harmonic distortion.

2.3.2 Analysis of Synthesized Voltage Levels

The single-phase 5-level hybrid MLDCL inverter synthesizes a 5-level bipolar output voltage across the load using eight switching modes. Table 2.1 summarizes the switching modes (modes 1 through 8) and their effects on the current flowing through the dc-link capacitors. This subsection describes the positive voltage states generated by the hybrid MLI during the half-cycle operation.

Fig. 2.5(a)–(d) show the modes of operation of the single-phase 5-level hybrid MLDCL inverter during the generation of positive states. The conduction paths of the active connections and devices are also shown. Throughout the positive half-cycle operation, IGBT pair Q_1 and Q_4 are kept ON while Q_2 and Q_3 are kept OFF.

Table 2.1:
Switching, Voltages, Capacitors, and Current States of a 5-Level Hybrid MLDCL Inverter Under the Proposed Schemes

Mode	*switches						Voltage states			Cap. states		Current state
	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	V_1	V_2	V_o	C_1	C_2	i_N
1	1	0	0	1	0	0	0	0	0	►	►	0
2	1	0	0	1	1	0	$V_{dc}/2$	0	$V_{dc}/2$	▼	▲	$-i_o$
3	1	0	0	1	0	1	0	$-V_{dc}/2$	$V_{dc}/2$	▲	▼	i_o
4	1	0	0	1	1	1	$V_{dc}/2$	$-V_{dc}/2$	V_{dc}	►	►	0
5	0	1	1	0	0	0	0	0	0	►	►	0
6	0	1	1	0	1	0	$V_{dc}/2$	0	$-V_{dc}/2$	▼	▲	i_o
7	0	1	1	0	0	1	0	$-V_{dc}/2$	$-V_{dc}/2$	▲	▼	$-i_o$
8	0	1	1	0	1	1	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}$	►	►	0

*switches: 1 = ON state and 0 = OFF state, ►= holding, ▼= discharging, and ▲= charging states.

1. Mode 1: In this voltage state, the capacitors C_1 and C_2 are charged to their nominal voltage and are held in this state by simply connecting to the dc supply (see Fig. 2.5(a)). With Q_5 and Q_6 switched OFF, the voltage across the capacitors is $V_{C1} = V_{C2} = \frac{V_{dc}}{2}$, where V_{C1} and V_{C2} are the voltages across C_1 and C_2, respectively. The node voltages are $V_1 = V_2 = V_3 = V_4 = 0$. Thus, the output voltage $V_o = 0$ is the potential difference between V_3 and V_4.

2. Mode 2: In this voltage state, Q_5 and Q_6 are switched ON and OFF, respectively, and diodes D_1 and D_2 are reverse and forward biased, respectively (see Fig. 2.5(b)). Consequently, capacitor C_1 discharges and C_2 (being connected directly to the dc source) charges to its peak voltage. The node voltages are $V_1 = V_3 = \frac{V_{dc}}{2}$ and $V_2 = V_4 = 0$. Thus, the output voltage $V_o = \frac{V_{dc}}{2}$.

3. Mode 3: In this voltage state, Q_6 and Q_5 are switched ON and OFF, respectively, and diodes D_2 and D_1 are reverse and forward biased, respectively (see Fig. 2.5(b)). Consequently, capacitor C_2 discharges and C_1 (being connected directly to the dc source) charges to its peak voltage. The node voltages are $V_1 = V_3 = 0$ and $V_2 = V_4 = -\frac{V_{dc}}{2}$. Thus, the output voltage $V_o = \frac{V_{dc}}{2}$.

4. Mode 4: In this voltage state, both Q_5 and Q_6 are switched ON and diodes D_1 and D_2 are both reverse biased. Consequently, the total dc source voltage is evenly blocked

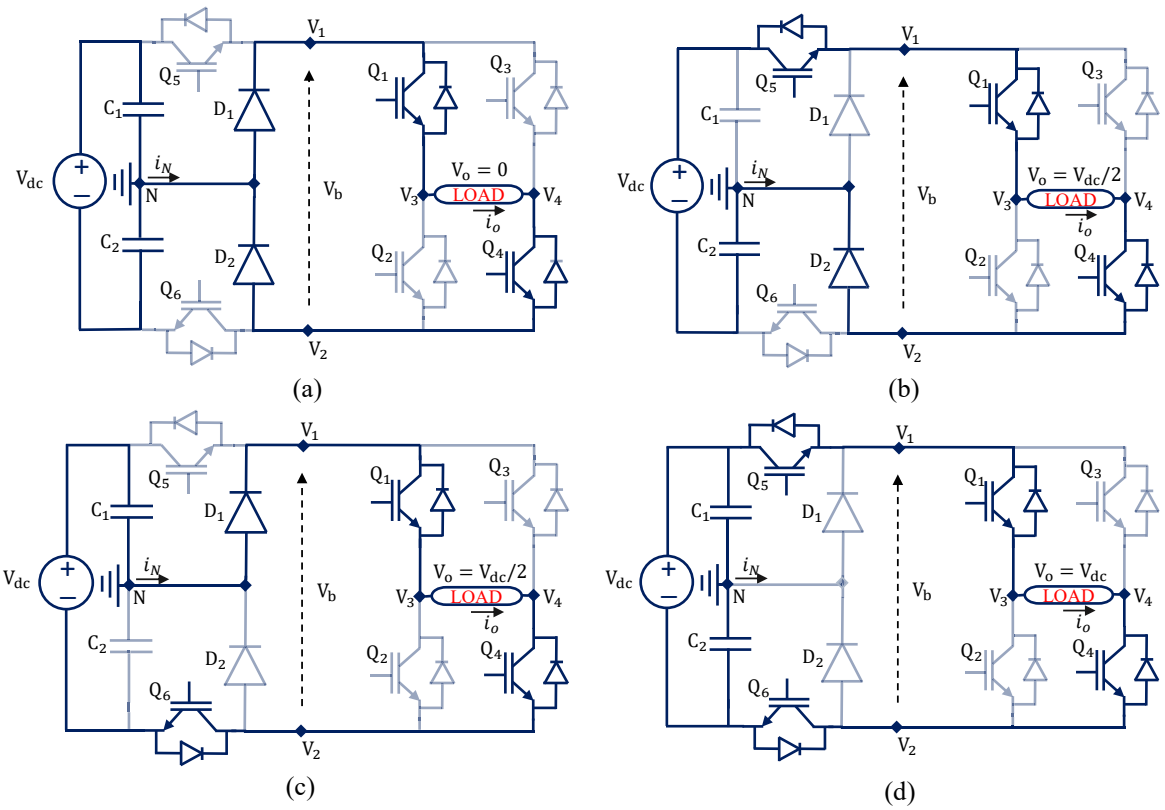


Figure 2.5: Operation of the 5-level hybrid MLDCL inverter showing positive voltage states: (a) Mode 1, (b) mode 2, (c) mode 3, and (d) mode 4 (the faint lines on the capacitors denote their discharging paths.)

as shown in Fig. 2.5(d), and capacitors C_1 and C_2 maintain their maximum voltage by being connected directly to the power supply. The node voltages are $V_1 = V_3 = \frac{V_{dc}}{2}$ and $V_2 = V_4 = -\frac{V_{dc}}{2}$. Thus, the output voltage $V_o = V_{dc}$.

During the negative half-cycle operation of the 5-level hybrid MLDCL inverter, IGBTs Q_2 and Q_3 in the H-bridge module are switched ON while Q_1 and Q_4 are switched OFF to generate negative voltage states. The switches in the level-generation stage are switched similarly to those in the positive half-cycle but considering the effect of the output current direction on the capacitor-voltage balancing when $V_o = -\frac{V_{dc}}{2}$.

Fig. 2.6 precises the total standing voltage (TSV) and voltage stress in the proposed hybrid inverter across every switching device on the respective voltage level generated across the load. Notably, each of the controlled-switching devices and power diodes in the first conversion stage withstand a maximum voltage across one capacitor, i.e., $\frac{V_{dc}}{2}$. Moreover, the H-bridge module's switching devices withstand the total dc source voltage, i.e., V_{dc}.

By Kirchhoff's voltage law and the synthesized voltage levels in the inverter topology

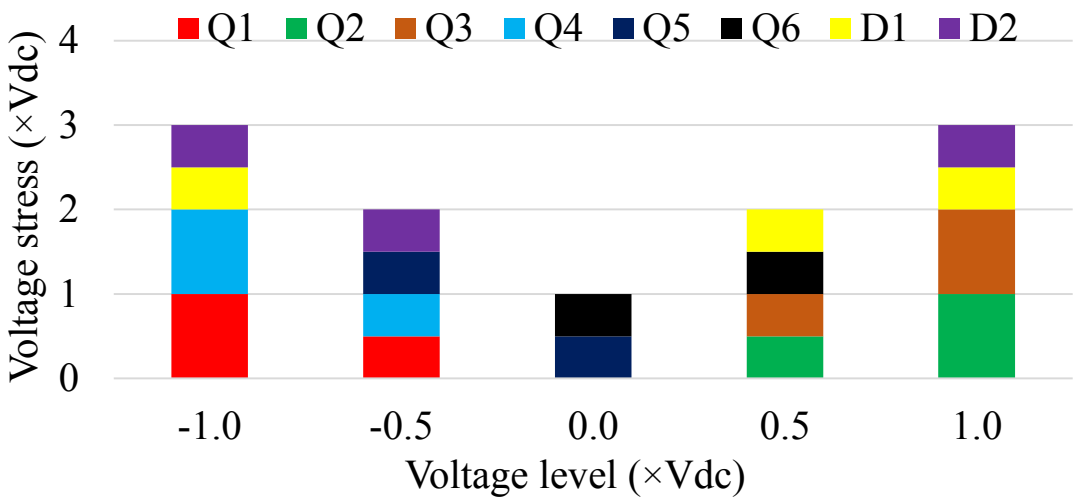


Figure 2.6: Withstand voltage for each switching device during all voltage levels of the 5-level hybrid MLDCL inverter.

Table 2.2:
Simulation and Experimental Parameters

Parameter	Symbol	Value
DC-link voltage	V_{dc}	200 V
DC-link capacitance	$C_1 = C_2$	100 μF
Carrier frequency	f_c	5 kHz
Modulation index	m	0.98
Fundamental frequency	f_o	50 Hz
Load condition	R	48, 148 Ω
	L	5 mH

of Fig. 2.4, the instantaneous stepped dc output voltage V_b can be expressed as

$$V_b = (S_{Q6} + S_{Q5})\frac{V_{dc}}{2}. \tag{2.2}$$

Here, S_{Q5} and S_{Q6} denote the switching signal functions of the switching devices Q_5 and Q_6, respectively (the switching signal functions of switching devices $Q1$–$Q4$ are similarly defined as S_{Q1}–S_{Q4}). From (2.1) and (2.2), the instantaneous output voltage across the load V_o of the hybrid inverter is then given as

$$V_o = \pm(S_{Q6} + S_{Q5})\frac{V_{dc}}{2}. \tag{2.3}$$

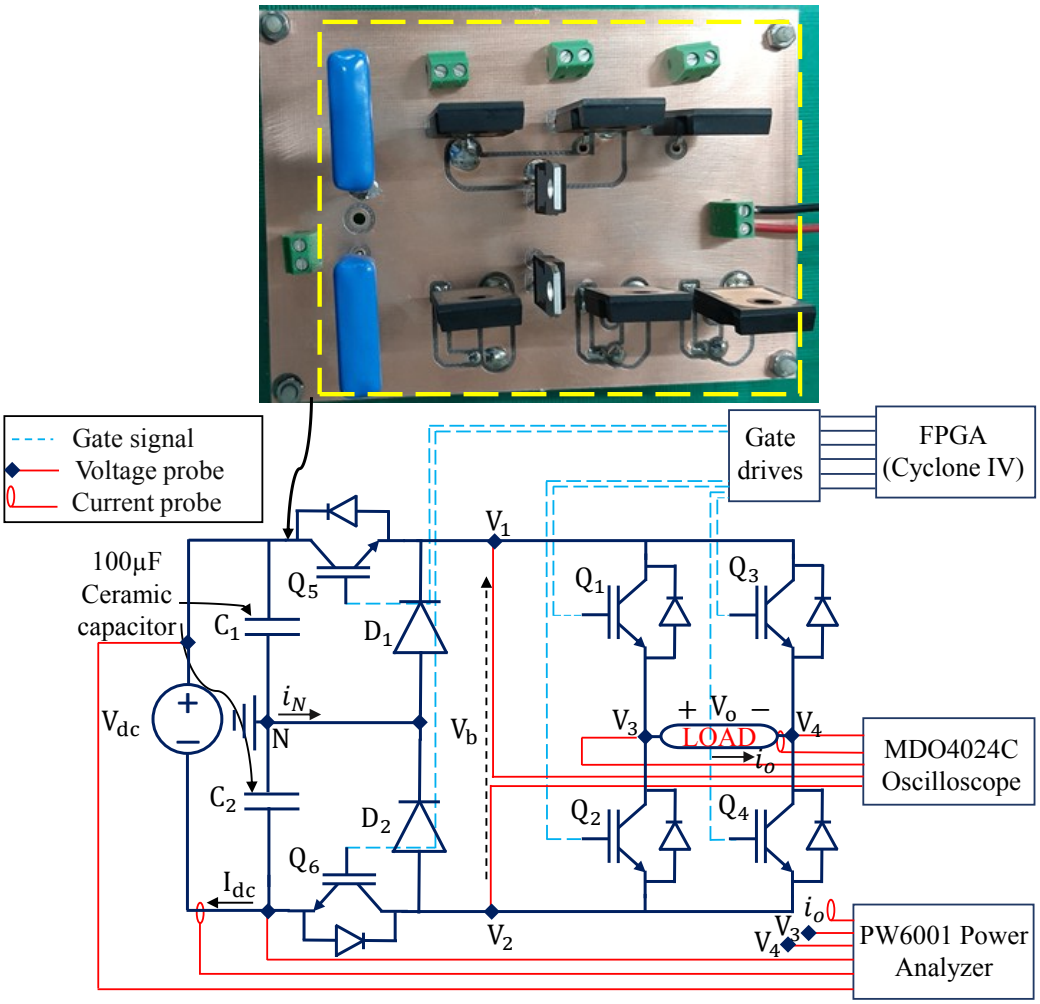


Figure 2.7: Experimental setup of the 5-level hybrid MLDCL inverter: photograph (top) and schematic (bottom).

2.4 Prototype

2.4.1 Construction of the Main Experimental Setup

A 380-W experimental prototype with the topology shown in Fig. 2.4 was built to validate the simulation study and demonstrate the merits of the proposed PWM schemes over the conventional method. The experimental setup is shown in Fig. 2.7. The prototype was constructed from six IGBTs (STGW20H60DF), two power diodes (STPSC20065Y), and two ceramic capacitors (KTD101B107M99A0B00). The inverter testing parameters were those listed in Table 2.2 except for the load inductor, which was changed to 10 mH for the experiments. Both the conventional and the proposed PWM schemes were implemented on a Cyclone IV E Altera DE0-Nano field-programmable gate array (FPGA)

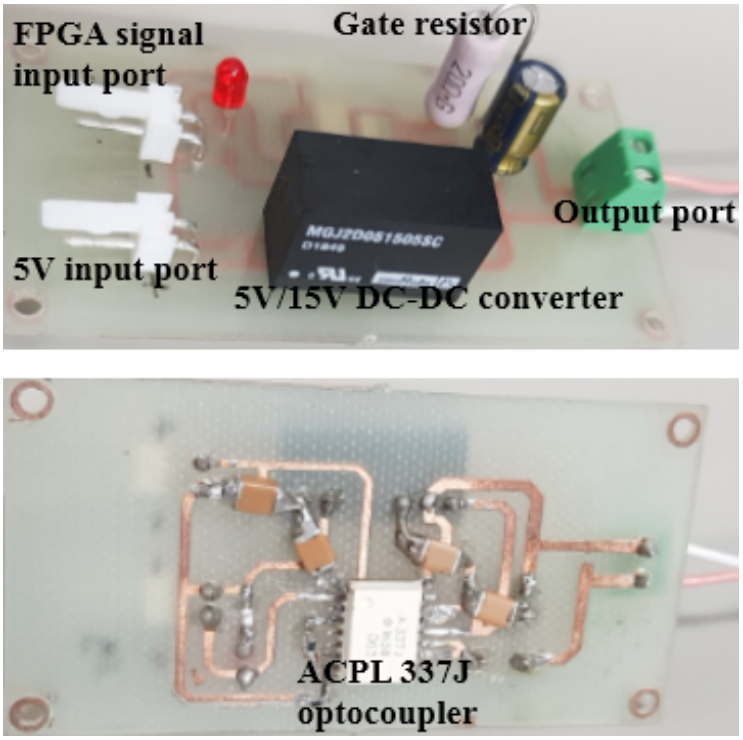


Figure 2.8: PCB of an IGBT gate drive circuit

board (EP4CE22F17C6N). All results of the following tests were observed on a mixed-domain oscilloscope (MDO4024C) and the power quality was investigated using a HIOKI (PW6001) power analyzer.

2.4.2 Design and Fabrication of an IGBT Gate Drive Circuit

The gate drive circuit is designed to synthesize PWM signals generated from FPGA kit by increasing the voltage level enough to fire the IGBT's gate. Secondly, it provides power solation between low voltage side (FPGA kit's side) and high voltage side (inverter's side). It also, provides isolated signal ground for each IGBT. The gate drive circuit is implemented by using ACPL 337J optocoupler, gate drive DC/DC converter (Murata MGJ2D051505SC 5/15 V) with isolated output ground, gate resistor of 20Ω, optocoupler input protection resistor of 150 Ω, and output shunt capacitor of 4.5 μF. The printed circuit board (PCB) of the gate drive circuit was designed in Design spark PCB software and manufacturing of the circuit was performed by using an MIT Lab prototyping machine. The PCB circuit is shown in Fig. 2.8. Each IGBT in a single-phase 5-level hybrid MLDCL inverter is controlled by one gate drive circuit. This means a total of six similar gate drive circuits were constructed.

2.5 Summary

In this chapter, the multilevel dc-link (MLDCL) inverters and hybrid MLDCL inverters were described and their detailed operating principles were presented. The discussion was briefly extended to the dc-link voltage-balancing in the NPC-based converters and the challenges facing the existing techniques for proper operation of the converter with high power density. Moreover, the description and analysis of the synthesized voltage levels in the single-phase 5-level hybrid MLDCL inverter were provided. Finally, the prototype of the single-phase 5-level hybrid MLDCL inverter was constructed and presented in this chapter.

Chapter 3

Modulation Schemes and Capacitor-Voltage Balancing

This chapter describes the conventional modulation strategy, the operating principle of the hybrid multilevel dc-link (MLDCL) inverter under the conventional method, and its impact on the dc-link capacitor voltages ripple. Moreover, detailed modeling, analysis, and verification of the proposed modulation strategies are provided. Detailed performance experimental validations and comparative investigations of the proposed schemes over the conventional method are provided in this chapter.

3.1 Conventional Modulation Scheme for the Single-Phase 5-Level Hybrid MLDCL Inverter

Note that in both the conventional and proposed modulation strategies, the bipolar reference modulation voltage v_{ref} was compared with zero voltage to generate the switching signals S_{Q1}–S_{Q4} at the fundamental frequency. The main difference between the two modulation strategies is the generation of S_{Q5} and S_{Q6}. Thus, the switching signal functions S_{Q1} through S_{Q4} can be expressed as

$$S_{Q1} = S_{Q4} = \begin{cases} 1, & \text{for } 0 \leq v_{ref} \leq 1. \\ 0, & \text{for } -1 \leq v_{ref} < 0. \end{cases} \tag{3.1}$$

$$S_{Q2} = S_{Q3} = \begin{cases} 0, & \text{for } 0 \leq v_{ref} \leq 1. \\ 1, & \text{for } -1 \leq v_{ref} < 0. \end{cases} \tag{3.2}$$

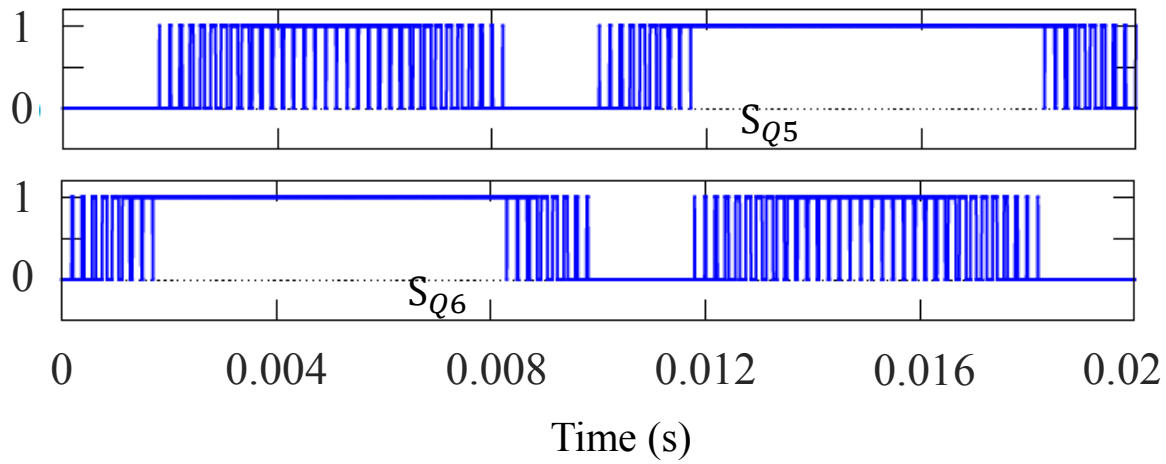


Figure 3.1: Conventional PWM switching signals of the switching devices in the level-generation stage during one fundamental period [39].

Fig. 3.1 shows the PWM switching signals of the switching devices in the level-generation stage at a carrier frequency of $f_c = 5$ kHz. In the conventional modulation strategy adopted here, only one switching device can commutate at high frequency at each moment. Additionally, the switching times of S_{Q5} and S_{Q5} are symmetric after each fundamental period.

3.2 Analysis of DC-Link Capacitor Voltage Using the Conventional Method

If the capacitance of the dc-link capacitors are assumed equal, i.e., $C_1 = C_2 = C$, the nominal voltages across the capacitors are also equal, i.e., $V_{C1} = V_{C2} = \frac{V_{dc}}{2}$. However, under normal operation, the voltages of the dc-link capacitors shift from their nominal voltage because they are influenced by the charging–discharging current flowing through the capacitors [74, 75]. This voltage difference must be minimized to ensure voltage balancing of the capacitors. As seen in Fig. 2.5, the capacitor voltage balancing is influenced by the switching devices in the level-generation stage, i.e., by Q_5 and Q_6. A necessary condition for balancing the dc-link voltage of the capacitors is equalizing the switching times of Q_5 and Q_6.

Fig. 3.2 shows the simulated voltages of the dc-link capacitors and the output voltage of the single-phase 5-level hybrid MLDCL inverter in the conventional method with $V_{dc} = 200$ V, $C_1 = C_2 = 1000$ μF, $f_c = 5$ kHz, and $f_o = 50$ Hz, loaded with $R = 48$ Ω and $L = 5$ mH. As the conventional method employs bulky dc-link capacitors, a small peak-

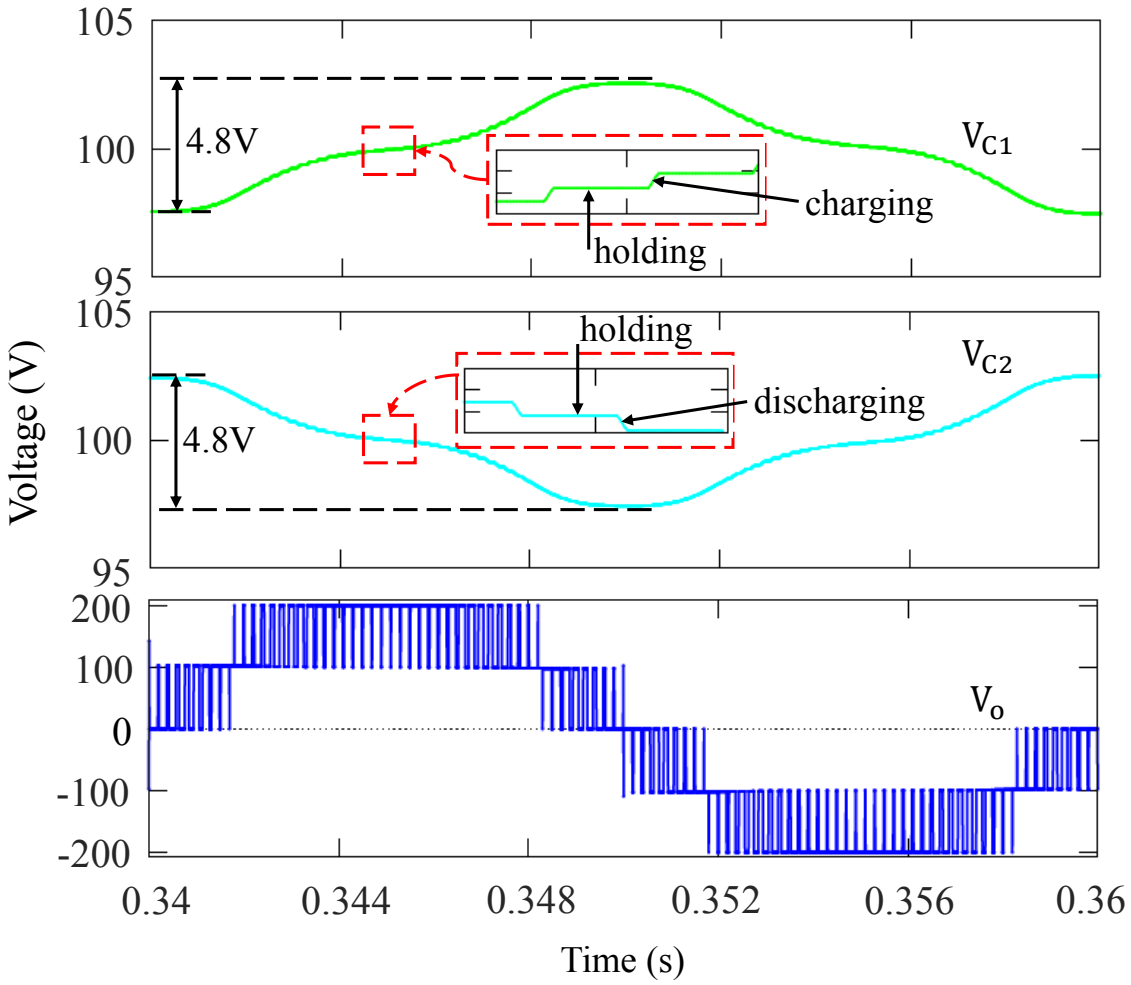


Figure 3.2: Simulated capacitor voltages and output voltage of the 5-level hybrid MLDCL inverter in the conventional method with $C_1 = C_2 = 1000$ μF during one fundamental period.

to-peak capacitor-voltage ripple of 4.8 V appeared but exerted no significant effect on the output voltage waveform. Note also that during the positive and negative half-cycles of the fundamental period, C_1 charged and discharged, respectively, while C_2 discharged and charged, respectively. In this approach, the current i_N contains the fundamental frequency and switching frequency components. Therefore, in the conventional method, the voltage balancing and sizing of the dc-link capacitors depend on the fundamental period. The dc-link capacitance in the conventional method is obtained as

$$C = \frac{I_{om}}{2\Delta V_{Cm} f_o} \tag{3.3}$$

where I_{om} and ΔV_{Cm} are the maximum output load current and maximum allowable voltage ripple in the capacitor, respectively. As the capacitor-voltage balancing depends on the fundamental period, the generated output voltage may contain undesired low-order

Table 3.1:
Switching, Voltages, Capacitors, and Current States of a 5-Level Hybrid MLDCL Inverter Under the PWM method in [40]

Mode	*switches						Voltage states			Cap. states		Current state
	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	V_1	V_2	V_o	C_1	C_2	i_N
1	1	0	1	0	*	*	0	0	0	►	►	0
2	1	0	0	1	1	0	$V_{dc}/2$	0	$V_{dc}/2$	▼	▲	$-i_o$
3	1	0	0	1	0	1	0	$-V_{dc}/2$	$V_{dc}/2$	▲	▼	i_o
4	1	0	0	1	1	1	$V_{dc}/2$	$-V_{dc}/2$	V_{dc}	►	►	0
5	0	1	0	1	*	*	0	0	0	►	►	0
6	0	1	1	0	1	0	$V_{dc}/2$	0	$-V_{dc}/2$	▼	▲	i_o
7	0	1	1	0	0	1	0	$-V_{dc}/2$	$-V_{dc}/2$	▲	▼	$-i_o$
8	0	1	1	0	1	1	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}$	►	►	0

*switches: *= ON/OFF states, ►= holding, ▼= discharging, and ▲= charging states.

harmonics [63]. This approach increases the THD of the generated voltage and reduces the overall performance of the inverter.

3.3 Operation of the Hybrid MLDCL Inverter Using the Recently Developed PWM Method

Under the recently developed PS-PWM scheme presented in [40], all the semiconductor switching devices in the hybrid MLDCL inverter are operated at high switching frequency. For one period of operation, the hybrid 5-level MLDCL inverter generates five output voltage levels synthesized through eight switching modes, as shown in Table 3.1. There are four distinctive switching modes in both positive and negative voltage polarity.

For the half period operation of the topology, the power components are switched such that in mode 1; the first voltage $V_o = 0$ is generated, in mode 2; the first $V_o = \frac{V_{dc}}{2}$ is produced, in mode 3; the second $V_o = \frac{V_{dc}}{2}$ is produced, in mode 4; a voltage $V_o = V_{dc}$ is generated, as demonstrated in Fig. 3.3. This switching sequence generates positive voltage states. By taking the same effort, the negative voltage states can also be generated as depicted in Table 3.1.

Based on Fig. 3.3 and Table 3.1, it can be noticed that during normal operation in

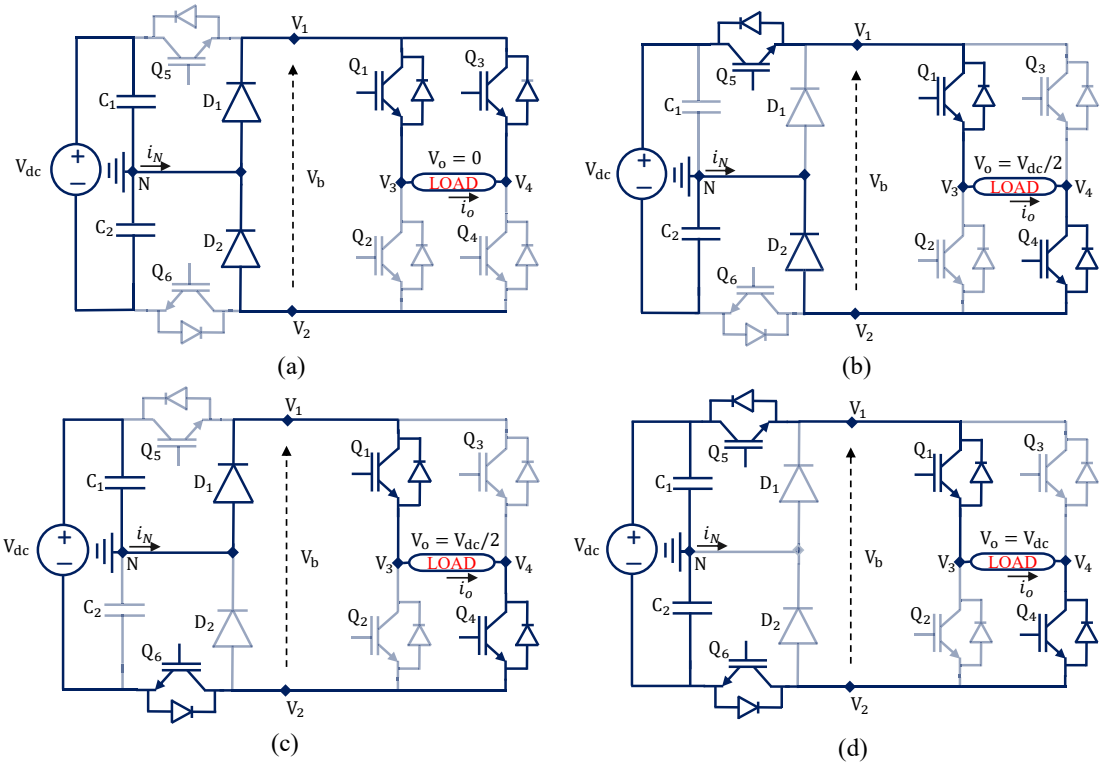


Figure 3.3: Half-cycle operation of the 5-level hybrid inverter showing positive voltage states under the method in [40]: (a) Mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

modes 1 and 4 in a positive semiperiod, the output load current does not influence the dc-link capacitor charge balance because both capacitors are in direct connection to a power supply. The capacitor voltage deviates from the nominal value when the voltages $V_o = \frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$ are generated across the load. The redundant switching states during the generation of half-full voltage have been utilized to balance the dc-link capacitor voltage by employing a proper voltage balancing algorithm which ensures symmetric switching time in a carrier period for the controlled-switching devices in the level-generation stage.

3.4 Recently Developed PS-PWM Scheme

For the analyzed hybrid MLDCL inverter, the recently developed PS-PWM scheme, in this thesis identified as PS-PWM1 presented in [40] has been applied to generate the switching signals for devices Q_1 to Q_6. In this scheme, four triangular carriers each of frequency f_c and peak amplitude A_c placed at an angular shift of 90° between adjacent carriers are compared with a sinusoidal reference voltage v_{ref} having a fundamental frequency f_o and peak amplitude A_r. The modulation index m ranging in the interval $[0, 1]$ has been

calculated as

$$m = \frac{A_r}{A_c}. \tag{3.4}$$

A step-by-step modulation of the reference voltage signal was logically modeled so that all possible voltage levels can be generated across the load with reduced harmonics. Moreover, this modulation strategy guarantees no-switching of the freewheel diodes of the controlled-switching devices in the level-generation stage, thereby reducing the power loss [75].

3.4.1 Generation of the Switching Signals Under PS-PWM1

Based on Table 3.1, the switching signals for the controlled-switching devices were generated by considering four cases. In all cases; V_{cr1}, V_{cr2}, V_{cr3} and V_{cr4} denotes carrier1, carrier2, carrier3, and carrier4, respectively. During the synthesis of the switching logical functions in the modulation strategies, let A be defined as an arbitrary switching logical function composed of inequality conditions, such that

$$A = \begin{cases} \text{True}, & \text{if inequalities hold.} \\ \text{False}, & \text{otherwise.} \end{cases} \tag{3.5}$$

The logical function description in (3.5) was considered in all of the following modulation techniques.

First Case

In this condition, the switching signals of controlled-switching devices considering the current flowing through them in mode 1, mode 5, mode 2, and mode 3 are deduced. According to Fig. 3.4, the logical functions in state (b) of mode 2 and 3 can be determined as follows:

$$S_{2or3b} = (0 \leq v_{ref} < \frac{1}{2}) \wedge (((v_{ref} \geq V_{cr1}) \wedge (v_{ref} \geq V_{cr3})) \vee ((v_{ref} \geq V_{cr2}) \wedge (v_{ref} \geq V_{cr4}))). \tag{3.6}$$

It is shown in (3.6) that modes 2 and 3 in the state (b) can be achieved when at least one joint-set of the carrier signals, which are 180° out-of-phase is less or equal to a reference signal and the limiting voltage reference signal ranges from 0 to $\frac{1}{2}$. In order to balance the charging and discharging of the capacitors C_1 and C_2, from (3.6), modes 2 and 3 must be derived as

$$S_{2b} = (0 \leq v_{ref} < \frac{1}{2}) \wedge ((v_{ref} \geq V_{cr1}) \wedge (v_{ref} \geq V_{cr3})), \tag{3.7}$$

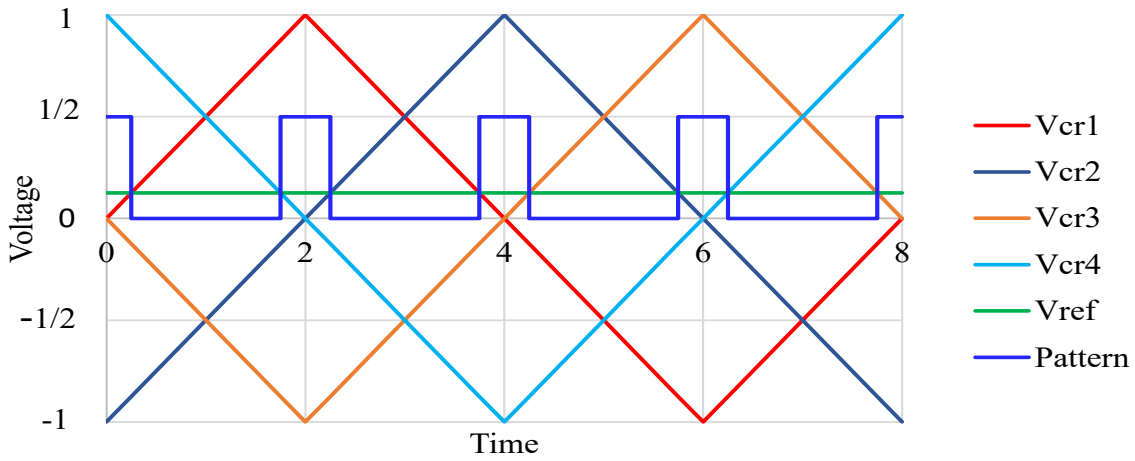


Figure 3.4: Reference signal and carriers for generation of switching signal under the first case in the PS-PWM1 method.

$$S_{3b} = (0 \leq v_{ref} < \frac{1}{2}) \wedge ((v_{ref} \geq V_{cr2}) \wedge (v_{ref} \geq V_{cr4})) \tag{3.8}$$

Also, modes 1 and 5 have two distinct operation states, as shown in Table 3.1, their logical functions in the state (a) are as follows:

$$S_{1or5a} = (0 \leq v_{ref} < \frac{1}{2}) \wedge (((v_{ref} < V_{cr1}) \vee (v_{ref} < V_{cr3})) \wedge ((v_{ref} < V_{cr2}) \vee (v_{ref} < V_{cr4}))). \tag{3.9}$$

Or mode 1 and 5 in state (a) can be derived in another form, since;

$$\begin{aligned} S_{1or5a} = (0 \leq v_{ref} < \frac{1}{2}) \wedge (((v_{ref} < V_{cr1}) \wedge (v_{ref} < V_{cr2})) \vee ((v_{ref} < V_{cr1}) \wedge (V_{ref} < V_{cr4})) \\ \vee ((V_{ref} < V_{cr3}) \wedge (v_{ref} < V_{cr2})) \vee ((v_{ref} < V_{cr3}) \wedge (V_{ref} < V_{cr4}))) \end{aligned} \tag{3.10}$$

Then, the switching logical function signal in (3.10) must be distributed to modes 1 and 5 as follows:

$$S_{1a} = (0 \leq v_{ref} < \frac{1}{2}) \wedge (((v_{ref} < V_{cr1}) \wedge (v_{ref} < V_{cr2})) \vee ((v_{ref} < V_{cr3}) \wedge (v_{ref} < V_{cr4}))) \tag{3.11}$$

$$S_{5a} = (0 \leq v_{ref} < \frac{1}{2}) \wedge (((v_{ref} < V_{cr1}) \wedge (v_{ref} < V_{cr4})) \vee ((v_{ref} < V_{cr2}) \wedge (v_{ref} < V_{cr3}))). \tag{3.12}$$

Second Case

The switching signals of controlled-switching devices in the 5-level hybrid MLDCL taking account of the current flowing through them in modes 4, 2, and 3 were deduced in this

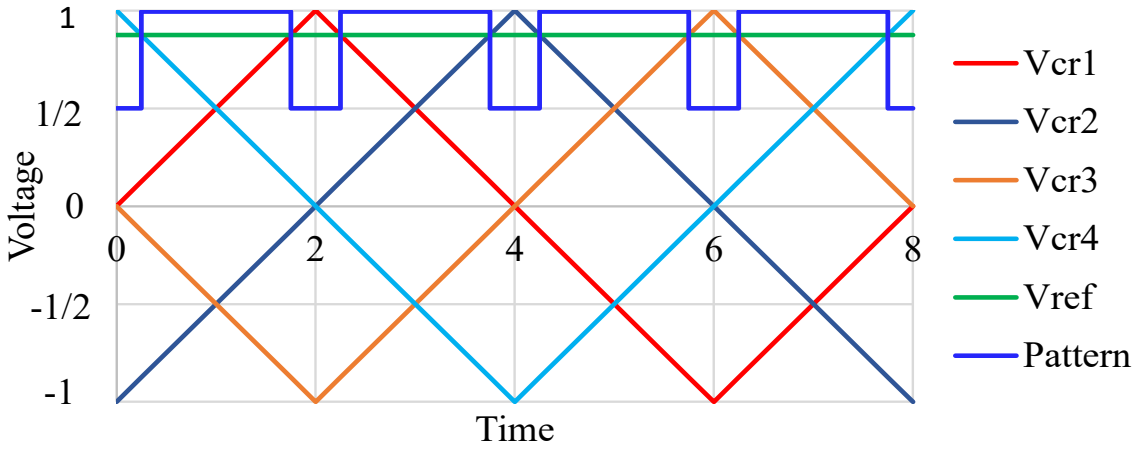


Figure 3.5: Reference signal and carriers for generation of switching signal under the second case in the PS-PWM1 method.

subsection. The logical function for mode 4 (see Fig. 3.5) is deduced as follows:

$$S_1 = (\frac{1}{2} \leq V_{ref} \leq 1) \wedge ((V_{ref} \geq V_{c1}) \wedge (V_{ref} \geq V_{c2}) \wedge (V_{ref} \geq V_{c3}) \wedge (V_{ref} \geq V_{c4})) \quad (3.13)$$

Equation (3.13) shows that the current flow and voltage in mode 1 can only be obtained when the reference signal is greater or equal to all carrier signals and the limiting reference voltage signal ranges from $\frac{1}{2}$ to 1. To achieve modes 2 and 3 operation of the inverter topology, there are two distinct states as shown in Table 3.1 which are necessary to balance the dc-link capacitor voltages. Therefore, in state (a), their logical functions can be given as follows:

$$S_{2or3a} = (\frac{1}{2} \leq v_{ref} \leq 1) \wedge ((v_{ref} < V_{cr1}) \vee (v_{ref} < v_{cr2}) \vee (v_{ref} < V_{cr3}) \vee (v_{ref} < V_{cr4})) \quad (3.14)$$

As shown in (3.14), modes 2 and 3 operation in state (a) can be achieved when at least one of the carrier signal has a magnitude larger than a reference signal and the limiting reference voltage signal ranges from $\frac{1}{2}$ to 1.

Proper selection of switching states is ensured in order to balance the charging and discharging of the capacitors C_1 and C_2. Therefore from (3.14), modes 2 and 3 must be derived as

$$S_{2a} = (\frac{1}{2} \leq v_{ref} \leq 1) \wedge ((v_{ref} < V_{cr1}) \vee (v_{ref} < V_{cr3})), \quad (3.15)$$

$$S_{3a} = (\frac{1}{2} \leq v_{ref} \leq 1) \wedge ((v_{ref} < V_{cr2}) \vee (v_{ref} < V_{cr4})). \quad (3.16)$$

Third Case

In this subsection, the switching signals of the controlled-switching devices considering the current flowing through them in modes 1, 5, 6, and 7 are determined. From Fig. 3.6,

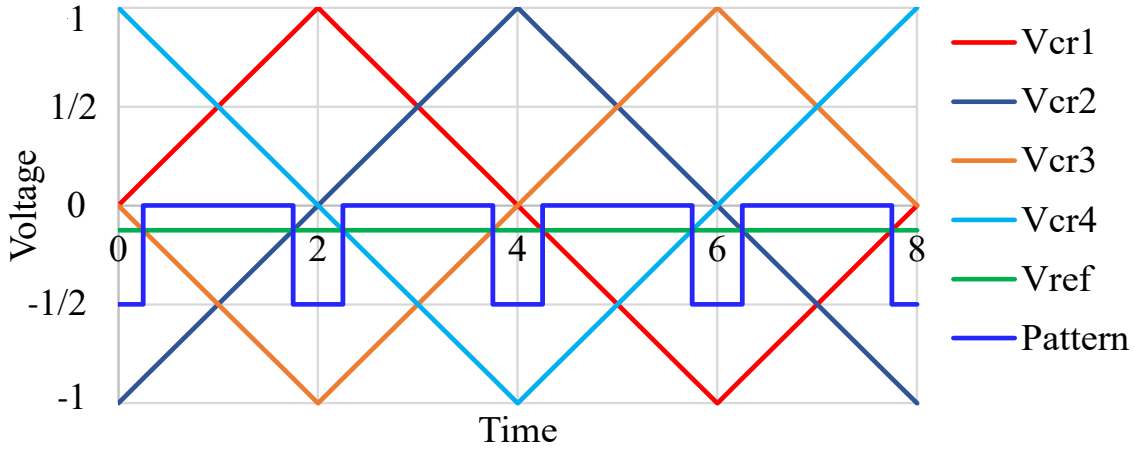


Figure 3.6: Reference signal and carriers for generation of switching signal under the third case in the PS-PWM1 method.

achieving modes 6 and 7 operation of the hybrid MLDCL inverter, there are two distinct states as shown in Table 3.1 which are necessary to balance the dc-link capacitor voltages. Therefore, in state (a), their logical functions can be derived as follows:

$$S_{6or7a} = (\frac{-1}{2} < v_{ref} \leq 0) \wedge (((v_{ref} \leq V_{cr1}) \wedge (v_{ref} \leq V_{cr3})) \vee ((v_{ref} \leq V_{cr2}) \wedge (v_{ref} \leq V_{cr4}))) \tag{3.17}$$

From equation (3.17), in order to balance the charging and discharging of the capacitors C_1 and C_2 in state (a) , modes 6 and 7 can be deduced as

$$S_{6a} = (\frac{-1}{2} < v_{ref} \leq 0) \wedge ((v_{ref} \leq V_{cr1}) \wedge (v_{ref} \leq V_{cr3})) \tag{3.18}$$

$$S_{7a} = (\frac{-1}{2} < v_{ref} \leq 0) \wedge ((v_{ref} \leq V_{cr2}) \wedge (v_{ref} \leq V_{cr4})) \tag{3.19}$$

Also, since modes 1 and 5 have two distinct states, their logical function in state (b) can given as

$$S_{1or5b} = (\frac{-1}{2} < v_{ref} \leq 0) \wedge (((v_{ref} > V_{cr1}) \vee (v_{ref} > V_{cr3})) \wedge ((v_{ref} > V_{cr2}) \vee (v_{ref} > V_{cr4}))) \tag{3.20}$$

Or since;

$$S_{1or5b} = (\frac{-1}{2} < v_{ref} \leq 0) \wedge (((v_{ref} > V_{cr1}) \wedge (v_{ref} > V_{cr2})) \vee ((v_{ref} > V_{cr1}) \wedge (v_{ref} > V_{cr4})) \vee ((v_{ref} > V_{cr3}) \wedge (v_{ref} > V_{cr2})) \vee ((v_{ref} > V_{cr3}) \wedge (v_{ref} > V_{cr4}))) \tag{3.21}$$

Then, the pattern in equation(3.21) must be distributed to mode 1 and 5 as follows:

$$S_{1b} = (\frac{-1}{2} < v_{ref} \leq 0) \wedge (((v_{ref} > V_{cr1}) \wedge (v_{ref} > V_{cr2})) \vee ((v_{ref} > V_{cr3}) \wedge (v_{ref} > V_{cr4}))) \tag{3.22}$$

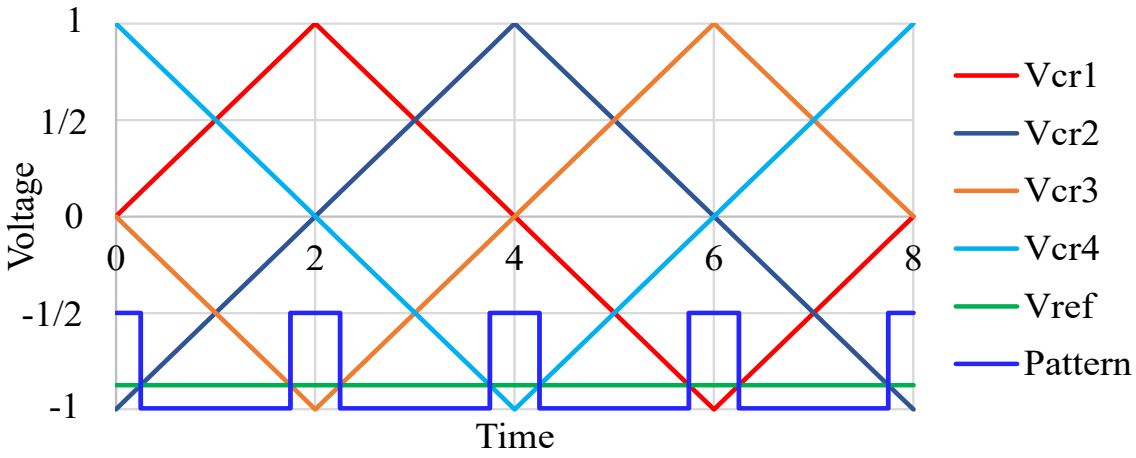


Figure 3.7: Reference signal and carriers for generation of switching signal under the fourth case in the PS-PWM1 method.

$$S_{5b} = (\frac{-1}{2} < v_{ref} \leq 0) \wedge (((v_{ref} > V_{cr1}) \wedge (v_{ref} > V_{cr4})) \vee ((v_{ref} > V_{cr2}) \wedge (v_{ref} > V_{cr3}))) \tag{3.23}$$

Fourth Case

In this subsection, the switching signals of the controlled-switching devices considering current flowing through them in modes 6, 7, and 8 are determined. From Fig. 3.7, the logical function for mode 8 can be derived as

$$S_8 = (-1 \leq v_{ref} \leq \frac{-1}{2}) \wedge ((v_{ref} \leq V_{cr1}) \wedge (v_{ref} \leq V_{cr2}) \wedge (v_{ref} \leq V_{cr3}) \wedge (v_{ref} \leq V_{cr4})) \tag{3.24}$$

Equation (3.24) shows that in mode 8, current flow and voltage can only be obtained when the reference signal is less or equal to all carrier signals and the limiting reference voltage signal ranges from -1 to $-\frac{1}{2}$.

To achieve modes 6 and 7 in state (b), their logical functions can be derived as

$$S_{6or7b} = (-1 \leq v_{ref} \leq \frac{-1}{2}) \wedge ((v_{ref} > V_{cr1}) \vee (v_{ref} > V_{cr2}) \vee (v_{ref} > V_{cr3}) \vee (v_{ref} > V_{cr4})) \tag{3.25}$$

As shown in equation (3.25), modes 6 and 7 operation in state (b) can be achieved when at least one of the carrier signal has a magnitude less than a reference signal and it ranges from -1 to $-\frac{1}{2}$. The selection of switching states is made in order to balance the charging and discharging of the capacitors C_1 and C_2 of the hybrid MLDCL inverter. Therefore from (3.25), mode 6 and 7 must be derived as

$$S_{6b} = (-1 \leq v_{ref} \leq \frac{-1}{2}) \wedge ((v_{ref} > V_{cr1}) \vee (v_{ref} > V_{cr3})), \tag{3.26}$$

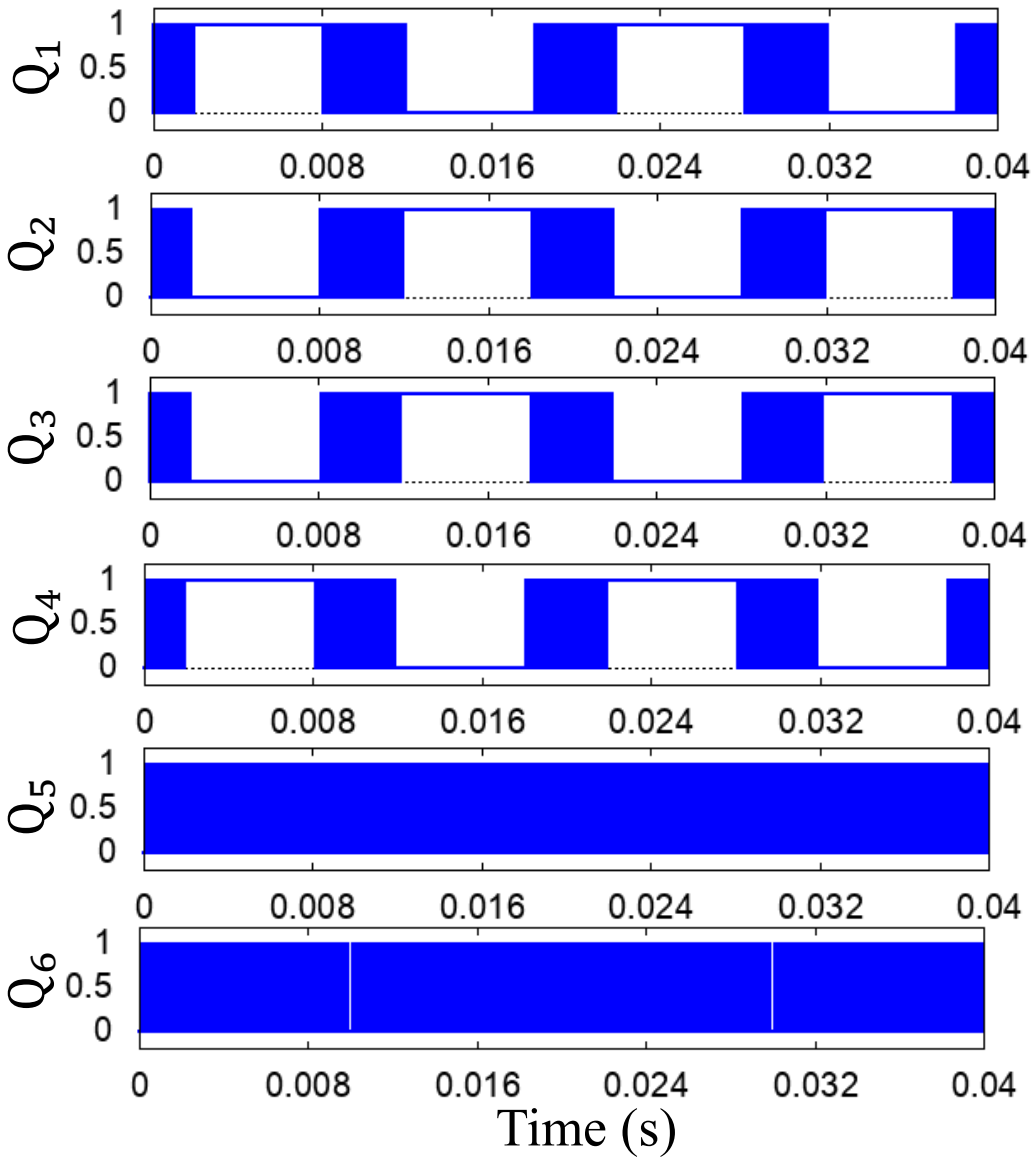


Figure 3.8: Switching signals of the 5-level hybrid MLDCL inverter synthesized by the PS-PWM1 scheme in [40].

$$S_{7b} = (-1 \leq v_{ref} \leq \frac{-1}{2}) \wedge ((v_{ref} > V_{cr2}) \vee (v_{ref} > V_{cr4})). \tag{3.27}$$

The complete logical switching functions of Q_1 through Q_6 were obtained by merging their corresponding logical switching functions (deduced above) into a single logical switching function for each controlled-switching device. From Table 3.1, the logical function for each controlled-switching device is given as follows;

$$Q_1 = S_{1a} \vee S_{1b} \vee S_{2a} \vee S_{2b} \vee S_{3a} \vee S_{3b} \vee S_4 \tag{3.28}$$

$$Q_2 = \neg Q_1 \tag{3.29}$$

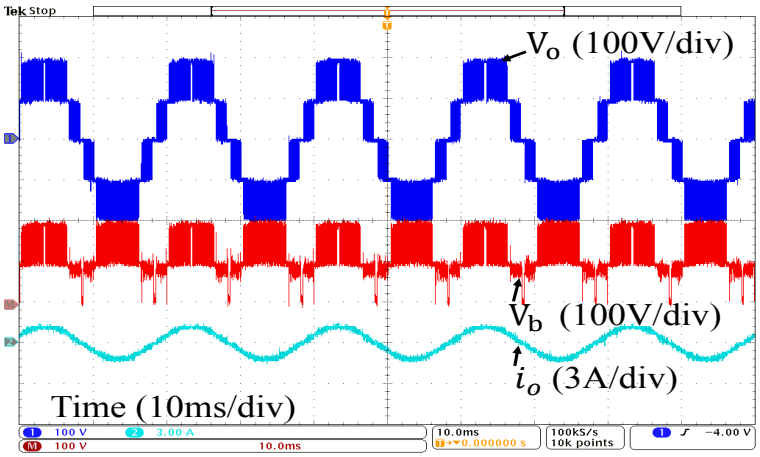


Figure 3.9: Experimental results showing output load voltage V_o, output voltage of the first stage V_b, and load current i_o when an R-L load (148Ω, 10mH) is used .

$$Q_3 = S_{1a} \vee S_{1b} \vee S_{6a} \vee S_{6b} \vee S_{7a} \vee y_{7b} \vee S_8 \tag{3.30}$$

$$Q_4 = \neg Q_3 \tag{3.31}$$

$$Q_5 = S_4 \vee S_8 \vee S_{2a} \vee S_{2b} \vee S_{6a} \vee S_{6b} \tag{3.32}$$

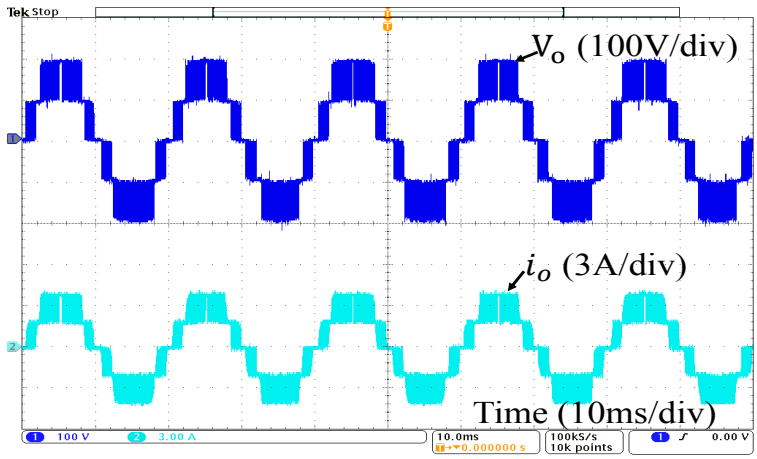
$$Q_6 = S_4 \vee S_8 \vee S_{3a} \vee S_{3b} \vee S_{7a} \vee S_{7b} \tag{3.33}$$

The generated PWM switching signals for all IGBTs as a result of merging all modeled logic functions are shown in Fig. 3.8. The PWM signals are applied to the gates of each IGBT in the single-phase hybrid MLDCL inverter to generate the desired voltage at the load. In this PWM strategy, all switching devices are operated at a high switching frequency. Thus, in this approach, the switching loss increases considerably in the 5-level hybrid MLDCL inverter.

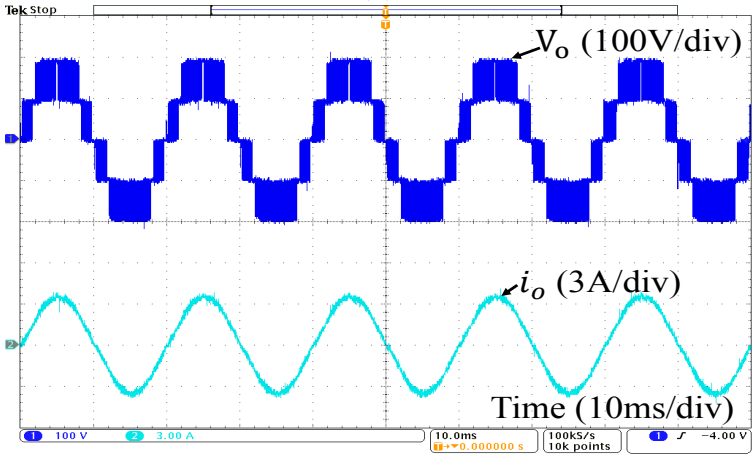
3.4.2 Experimental Results Obtained by the PS-PWM1 Scheme

A low-power (380W) single-phase hybrid MLDCL inverter prototype has been constructed to verify the performance of the topology presented in Fig. 2.4. The PS-PWM1 strategy has been implemented using the Cyclone IV E FPGA board. The gate drive circuit has been implemented using an ACPL 337J optocoupler. The parameters of the inverter are shown in Table 2.2.

Figs. 3.9-3.10 show the steady-state performance of the 5-level hybrid inverter under different loading conditions. Fig. 3.9 shows the generated voltages and current when the inverter supply a resistive-inductive (R-L) load with a light inductive component. As demonstrated in Fig. 3.10(a), the generated output current has the same number of levels



(a)

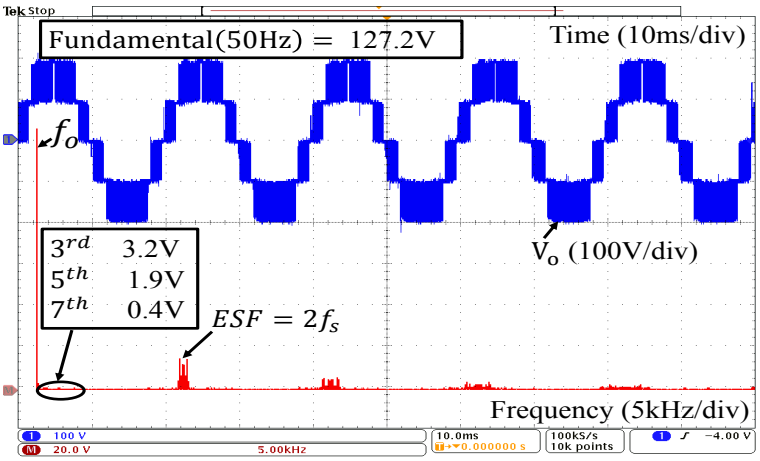


(b)

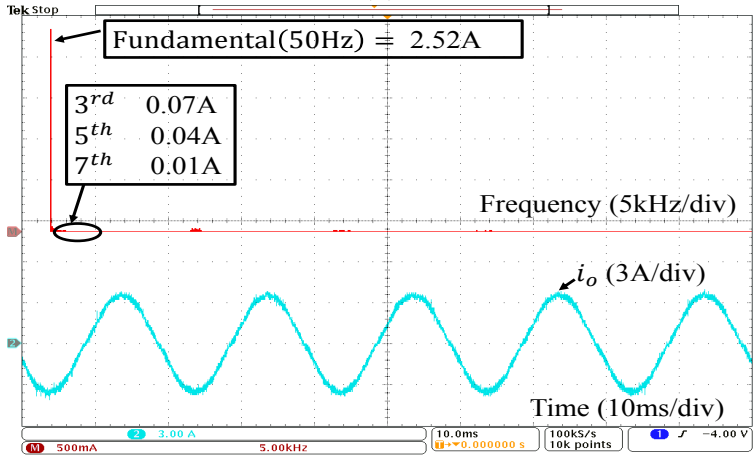
Figure 3.10: Experimental results showing output voltage V_o, and current i_o (a) when supplying $R = 48\Omega$ load (b) when supplying R-L load (48Ω, 10mH).

as the output voltage without any noticeable voltage spike when an inverter is connected to a resistive load. The generated output voltage in Fig. 3.10(b) has a small spike (distortion) at a zero voltage when the inverter supplies an R-L load with low power factor due to a heavy inductive component. This distortion becomes severe as the inductive component dominates the load, resulting in reducing the overall inverter's reliability or destroying the switching devices.

The generated output voltage and current have been analyzed using fast Fourier transforms (FFT) to validate the performance of the adopted modulation strategy on the presented hybrid inverter, and their results are shown in Fig. 3.11(a) and Fig. 3.11(b), respectively. Also, by using HIOKI PW6001 power analyzer, we observed that the generated output voltage and current have a total harmonic distortion (THD) of 30.4% and



(a)



(b)

Figure 3.11: Experimental results showing (a) output voltage V_o and its corresponding harmonic spectra (20V/div) and (b) output current i_o and its corresponding harmonic spectra (500mA/div).

3.45%, respectively. However, if only the first 50^{th} harmonics are considered, then output voltage has a THD of 3.52%. Therefore, a smaller voltage filter will be required to achieve THD within IEEE 519 std compared to the two-level inverter. An additional merit of the presented topology has been verified at an output power of 265W, at which efficiency of 97.3% has been measured.

The hybrid inverter has been experimented on with the sudden varying loads to verify the dynamic response of modulation and voltage balancing, as demonstrated in Fig. 3.12. It is noticeable that the inverter generated all voltage levels without noticeable distortion despite varying load conditions, which verifies the feasibility of the modulation strategy.

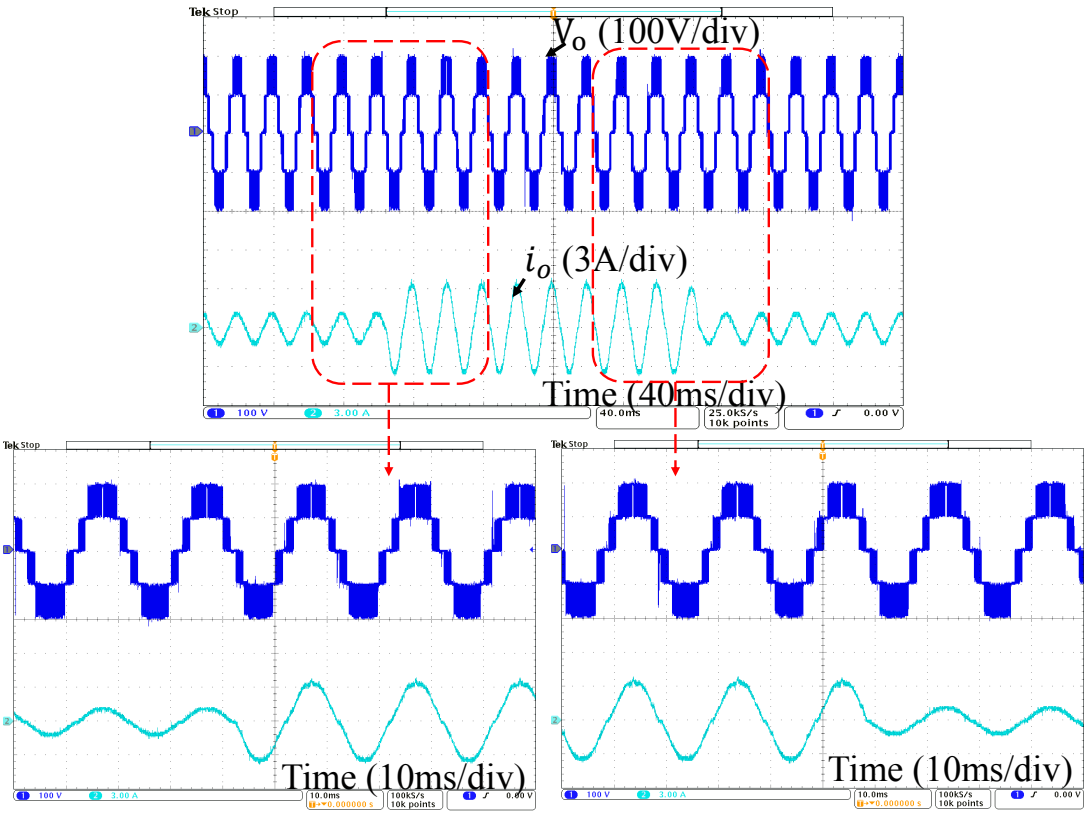


Figure 3.12: Experimental transient results showing output load voltage V_o and load current i_o when the load suddenly changes from (148Ω, 10mH) to (48Ω, 10mH) and back again to (148Ω, 10mH).

3.5 Proposed PS-PWM Strategy

Based on Table 2.1 and Fig. 2.5, the PS-PWM scheme was designed to generate switching signals for the IGBTs in the level-generation stage. When S_{Q6} and S_{Q5} were generated in the proposed PS-PWM, two triangular carriers v_{cr1} and v_{cr2}, each of frequency f_c and peak amplitude A_c but phase-shifted by 180°, were compared with the unipolar reference voltage v_{refb}, which exhibited two peaks at the fundamental frequency with a peak amplitude of A_r (see Fig. 3.13). The modulation index m ranges over the interval $[0, 1]$ and was determined as $m = \frac{A_r}{A_c}$.

The triangular carriers for S_{Q6} and S_{Q5} were selected by considering the limiting conditions of the reference voltage: $0 \leq v_{refb} \leq \frac{1}{2}$ and $\frac{1}{2} \leq v_{refb} \leq 1$. This approach ensures proper charge balance of the dc-link capacitors. Fig. 3.14 illustrates the selection of carriers and the switching signals generated during two carrier periods under the aforementioned limiting conditions. Under the first limiting condition (see Fig. 3.14(a)), the triangular

carriers are associated with the generation of two voltage levels as follows:

$$S_0 = \left(0 \leq v_{refb} \leq \frac{1}{2}\right) \wedge [(v_{refb} \geq v_{cr1}) \wedge (v_{refb} \geq v_{cr2})], \tag{3.34}$$

where S_0 is the logical switching signal function of Q_6 and Q_5 for generating a zero voltage. The zero voltage level is obtained in the first limiting condition by selecting all carriers when they are simultaneously less or equal to the unipolar sinusoidal reference voltage signal, and the reference voltage signal ranges from 0 to $\frac{1}{2}$, as denoted in (3.34).
To obtain the first $V_b = \frac{V_{dc}}{2}$, the carriers can be selected as

$$S_{\frac{1}{2}-1} = \left(0 \leq v_{refb} \leq \frac{1}{2}\right) \wedge [(v_{refb} \geq v_{cr1}) \vee (v_{refb} \geq v_{cr2})] \tag{3.35}$$

where $S_{\frac{1}{2}-1}$ is the logical switching signal function of Q_6 and Q_5 generating the first half-full voltage. Equation (3.35) denotes that the half-full dc voltage in the first limiting condition can be obtained by selecting either v_{cr1} or v_{cr2} when they are less or equal to the unipolar sinusoidal reference voltage signal, and the reference voltage signal ranges from 0 to $\frac{1}{2}$. To ensure dc-link capacitor voltage balancing, (3.35) must be evenly distributed among all IGBTs in the level-generation stage as follows:

$$S_{Q5-1} = \left(0 \leq v_{refb} \leq \frac{1}{2}\right) \wedge (v_{refb} \geq v_{cr1}), \tag{3.36}$$

$$S_{Q6-1} = \left(0 \leq v_{refb} \leq \frac{1}{2}\right) \wedge (v_{refb} \geq v_{cr2}) \tag{3.37}$$

where S_{Q5-1} and S_{Q6-1} are the logical switching signal functions of Q_5 and Q_6, respectively for generating the first half-full voltage.

Under the second limiting condition ($\frac{1}{2} \leq v_{refb} \leq 1$ in Fig. 3.14(b)), the selection of the carriers for S_{Q6} and S_{Q5} was deduced as detailed below. To obtain $V_b = \frac{V_{dc}}{2}$ under the second limiting condition, the carriers can be selected as

$$S_{\frac{1}{2}-2} = \left(\frac{1}{2} \leq v_{refb} \leq 1\right) \wedge [(v_{refb} < v_{cr1}) \vee (v_{refb} < v_{cr2})] \tag{3.38}$$

where $S_{\frac{1}{2}-2}$ is the logical switching signal function of Q_6 and Q_5 generating the second half-full voltage. Equation (3.38) denotes that the half-full dc voltage in the second limiting condition can be achieved by selecting either v_{cr1} or v_{cr2} when they are greater than the unipolar sinusoidal reference voltage signal, and the reference voltage signal ranges from $\frac{1}{2}$ to 1. To account for dc-link capacitor voltage balancing, (3.38) must be evenly distributed among all IGBTs in the level-generation stage as follows:

$$S_{Q5-2} = \left(\frac{1}{2} \leq v_{refb} \leq 1\right) \wedge (v_{refb} < v_{cr1}), \tag{3.39}$$

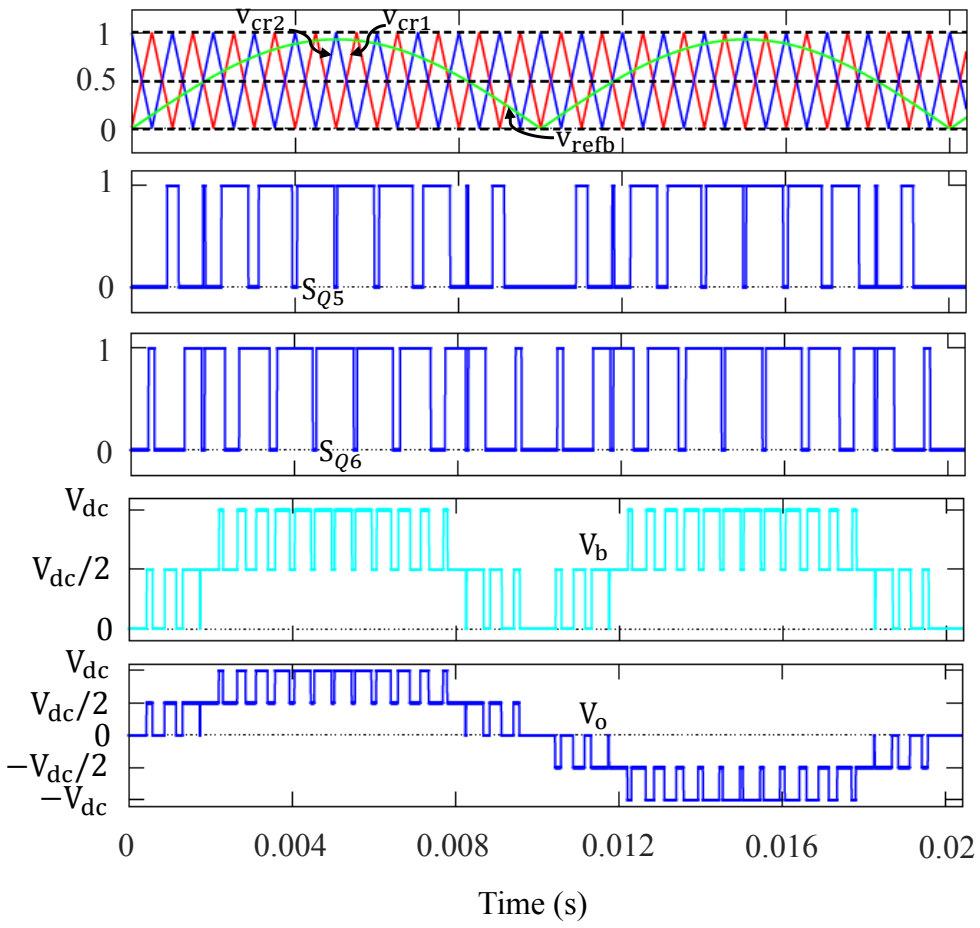


Figure 3.13: Proposed PS-PWM scheme and fundamental voltage of the 5-level hybrid MLDCL inverter at $f_c = 1$ kHz.

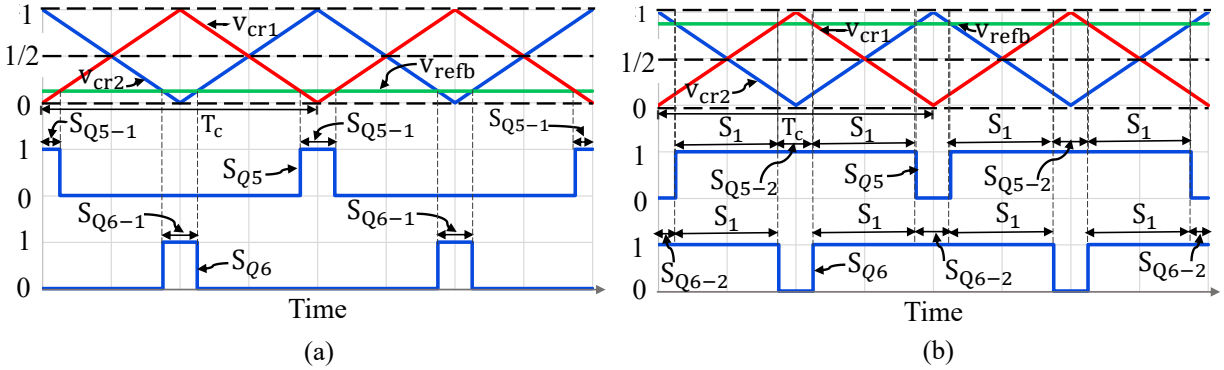


Figure 3.14: Selection of carriers and sequence of switching signals in the proposed phase-shifted PWM scheme: (a) $0 \leq v_{refb} \leq \frac{1}{2}$ and (b) $\frac{1}{2} \leq v_{refb} \leq 1$, where v_{refb} is the unipolar sinusoidal reference voltage.

$$S_{Q6-2} = \left(\frac{1}{2} \leq v_{refb} \leq 1\right) \wedge (v_{refb} < v_{cr2}) \tag{3.40}$$

where S_{Q5-2} and S_{Q6-2} are the logical switching signal functions of Q_5 and Q_6, respectively for generating the second half-full voltage. To generate $V_b = V_{dc}$, the triangular carriers can be selected as

$$S_1 = \left(\frac{1}{2} \leq v_{refb} \leq 1\right) \wedge [(v_{refb} \geq v_{cr1}) \wedge (v_{refb} \geq v_{cr2})] \tag{3.41}$$

where S_1 is the logical switching signal function of Q_5 and Q_6 for generating V_{dc}. Equation (3.41) shows that the full dc voltage in mode 4 can only be achieved by selecting all carriers when they are simultaneously less or equal to the unipolar sinusoidal reference voltage signal, and the reference voltage signal ranges from $\frac{1}{2}$ to 1.

The complete logical switching functions of Q_5 and Q_6 were obtained by merging (using OR gate) their corresponding logical switching functions (deduced above) into a single logical switching function for each controlled-switching device. S_{Q5} and S_{Q6} are then described by (3.42) and (3.43), respectively.

$$S_{Q5} = S_0 \vee S_{Q5-1} \vee S_{Q5-2} \vee S_1. \tag{3.42}$$

$$S_{Q6} = S_0 \vee S_{Q6-1} \vee S_{Q6-2} \vee S_1. \tag{3.43}$$

In the proposed PS-PWM strategy, the equivalent switching frequency (ESF) of the output voltage is $2f_c$. Hence, the first switching harmonic cluster of the output voltage has a frequency of $2f_c$ and other high-frequency harmonic clusters occur at integer multiples of ESF. Therefore, the proposed modulation strategy eliminates harmonics at odd integer multiples of the carrier frequency.

3.6 DC-Link Capacitor Voltage Balancing

3.6.1 Impacts of Capacitor-voltage Deviation

Moderating the capacitor-voltage deviation is essential for proper operation of the 5-level hybrid MLDCL inverter. Fig. 3.15 shows the impact of capacitor-voltage deviation when generating an output voltage $V_b = \frac{V_{dc}}{2}$. For example, if V_{C2} exceeds the average value (see Fig. 3.15(a)), the generated output voltage will be lower than $\frac{V_{dc}}{2}$. Conversely, if V_{C2} is below the average value, the generated output voltage will exceed $\frac{V_{dc}}{2}$. Similarly, if V_{C1} exceeds the average value (see Fig. 3.15(b)), the generated voltage will be lower than $\frac{V_{dc}}{2}$. Conversely, if V_{C1} is below the average value, the generated voltage will exceed $\frac{V_{dc}}{2}$. Such

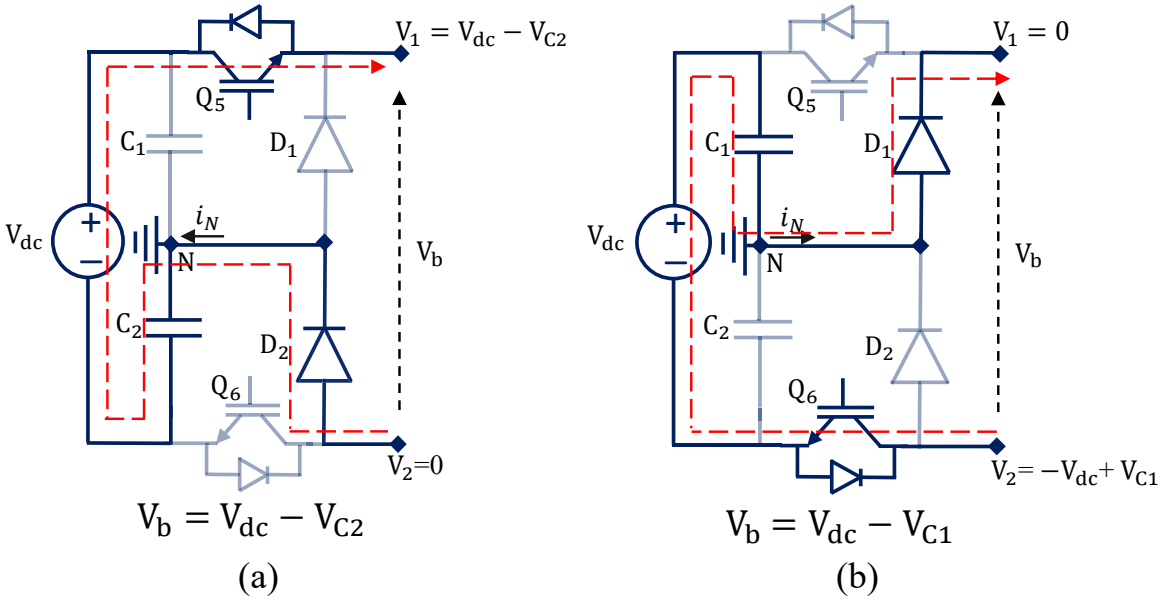


Figure 3.15: Impact of capacitor-voltage deviation on the output voltage.

voltage deviation in the dc-link capacitors can increase the distortion in the output voltage waveforms. Furthermore, a high capacitor-voltage deviation increases the voltage stress on the switching devices and reduces the overall reliability of the inverter.

It is essential to note that not every switching state in the 5-level hybrid MLDCL inverter contributes to voltage deviation in the dc-link capacitor voltage (see Table 2.1). The capacitor voltage deviates from the nominal value when voltages $V_o = \frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$ are generated across the load [54]. The two redundant switching states of these voltage states are available for balancing the capacitor voltage.

3.6.2 Modeling of the DC-Link Capacitor Voltage

The instantaneous voltage across the capacitor (V_C) during one carrier period is given as

$$V_C = V_{Cnom} \pm \Delta V_C \tag{3.44}$$

where V_{Cnom} is the nominal capacitor voltage and ΔV_C is the capacitor-voltage deviation. Clearly, ΔV_C influences the capacitor voltage fluctuations and must be minimized. The average capacitor voltage deviation ($\Delta \overline{V}_C$) during the carrier period T_c is given as

$$\Delta \overline{V}_C = \frac{\bar{i}_N}{2C} T_c \tag{3.45}$$

where $\bar{i}_N$ is the discharging/charging current averaged over the carrier period. From (3.45), the capacitor-voltage deviation can evidently be regulated by controlling the current flow into the neutral-potential point during each carrier period.

3.6.3 Modeling of the DC-Link Current

Applying Kirchhoff's current law at the neutral-potential point N in Fig. 2.4, the instantaneous discharging/charging current i_N is given by

$$i_N = (S_{Q6} - S_{Q5})i_o. \tag{3.46}$$

Similarly, the average discharging/charging current $\bar{i}_N$ is given as

$$\bar{i}_N = (d_{Q6} - d_{Q5})\bar{i}_o \tag{3.47}$$

where $\bar{i}_o$ is the average output current during the carrier period, and d_{Q6} and d_{Q5} are the initial duty cycles of S_{Q6} and S_{Q5}, respectively, before adjusting the duty cycle. Equation (3.47) clarifies that the discharging/charging current can be monitored by controlling the duty cycles of S_{Q6} and S_{Q5}. Moreover, if the carrier frequency is sufficiently higher than the fundamental frequency, the reference voltage v_{refb} can be assumed as constant throughout the carrier cycle [76, 78]. The initial duty cycle is then expressed as

$$d_{Q6} = d_{Q5} = v_{refb}. \tag{3.48}$$

3.6.4 Balancing the Neutral-Point Potential

The voltages of the dc-link capacitors can be balanced by slightly adjusting the duty cycles associated with the redundant switching states (modes 2 and 3 if the voltage polarity is positive; modes 6 and 7 if the voltage polarity is negative). This mechanism considers only the controlled-switching devices in the level-generation stage. To balance the capacitor voltages, consider a scenario in which the voltage $V_{C1} > \frac{V_{dc}}{2}$ and the current $i_o > 0$. The dc-link capacitor C_1 must discharge under the two reference limiting conditions ($0 \leq v_{refb} \leq \frac{1}{2}$ and $\frac{1}{2} \leq v_{refb} \leq 1$). If the capacitor voltage deviates under either of these conditions, the duty cycles of S_{Q6} and S_{Q5} will be slightly adjusted by an amount Δd during the carrier period. Thus, d_{Q6} and d_{Q5} must be decreased and increased by Δd, respectively. The duty cycle adjustment does not compromise the quality of the output voltage.

Then, $\bar{i}_N$ in (3.47) can be improved as

$$\bar{i}_N = (d_{Q6} - d_{Q5} - 2\Delta d)\bar{i}_o. \tag{3.49}$$

In this scenario, the current $\bar{i}_N$ during the carrier period is negative and given by

$$\bar{i}_N = -2\bar{i}_o\Delta d. \tag{3.50}$$

During the positive half-cycle, $\bar{i}_N$ will be positive if the capacitor voltage V_{C1} is below the nominal voltage.

Δd is easily obtained using a digital limit window comparator. The capacitor-voltage balancing scheme acquires similar information to logical switching but without sampling the dc-link capacitor voltage. Consequently, this scheme lowers the control complexity of balancing the dc-link capacitor voltage. As an additional advantage, this voltage balancing scheme requires no sensor measurements of the current i_N; instead, i_N is predicted in the PWM operation. Moreover, as the capacitor-voltage balancing in the proposed method depends on the carrier frequency, it considerably reduces the low-order harmonics of the output voltage.

3.7 Simulation Results by the Proposed PS-PWM: A Comparative Investigation

The 5-level hybrid MLDCL inverter with the proposed modulation scheme presented in Section 3.5 was simulated in the PSIM/PLECS software environment. The conventional method was also simulated as a benchmark. The circuit parameters are listed in Table 2.2. In the simulation, the inverter was connected to a single-phase resistive–inductive (R–L) load connected in series.

The output load voltages, the output voltages of the level-generation stage, and output currents of the 5-level hybrid MLDCL inverter were obtained under the conventional method (Fig. 3.16(a)–(c)) and the proposed method (Fig. 3.16(d)–(f)) with $C = 100$ μF. In both methods, the output load voltage was bipolar (c.f. Fig. 3.16(a) and (d)) and the output voltage of the level-generation stage was unipolar (c.f. Fig. 3.16(b) and (e)), thus satisfying the analysis of (2.1–2.3). Under the conventional method, the generated output load voltage and output voltage of the level-generation stage (Fig. 3.16(a) and (b), respectively) were distorted by high fluctuations of the dc-link capacitor voltage. After applying the proposed method, both voltages were free of these distortions (Fig. 3.16(d) and (e)). Moreover, the output current of the proposed method exhibited small ripples and was more purely sinusoidal than the output current of the conventional method (c.f. Fig. 3.16(c) and (f)). Therefore, the proposed modulation method reduced the distortion in the output voltage and current while minimizing the current ripple, despite its small dc-link capacitance.

To confirm the higher performance of the proposed PS-PWM method than the conventional method in the 5-level hybrid MLDCL inverter, a fast Fourier transform (FFT)

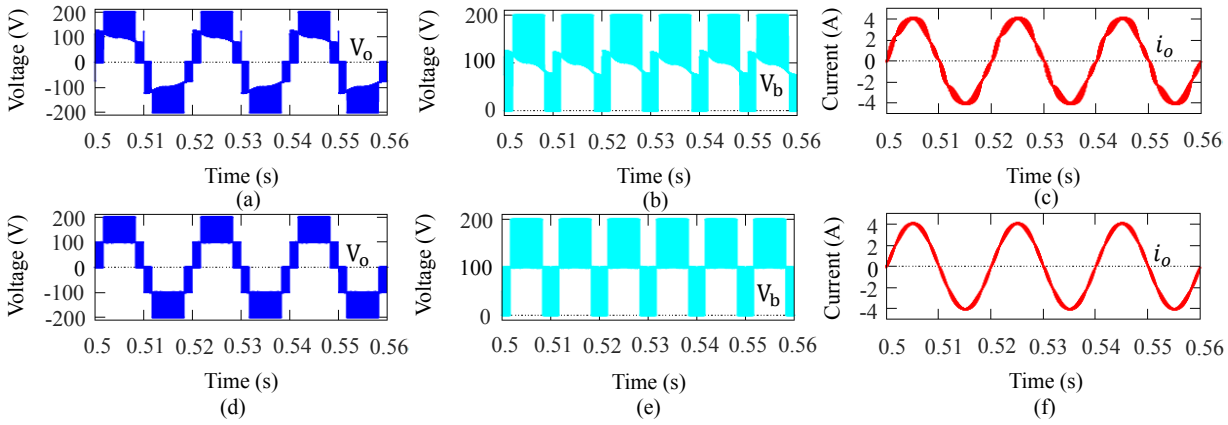


Figure 3.16: Simulated output voltage, voltage at the level-generation stage, and output current over three fundamental periods ($C_1 = C_2 = 100$ μF and $f_c = 5$ kHz): (a), (b), and (c) the conventional method, and (d), (e), and (f) the proposed method.

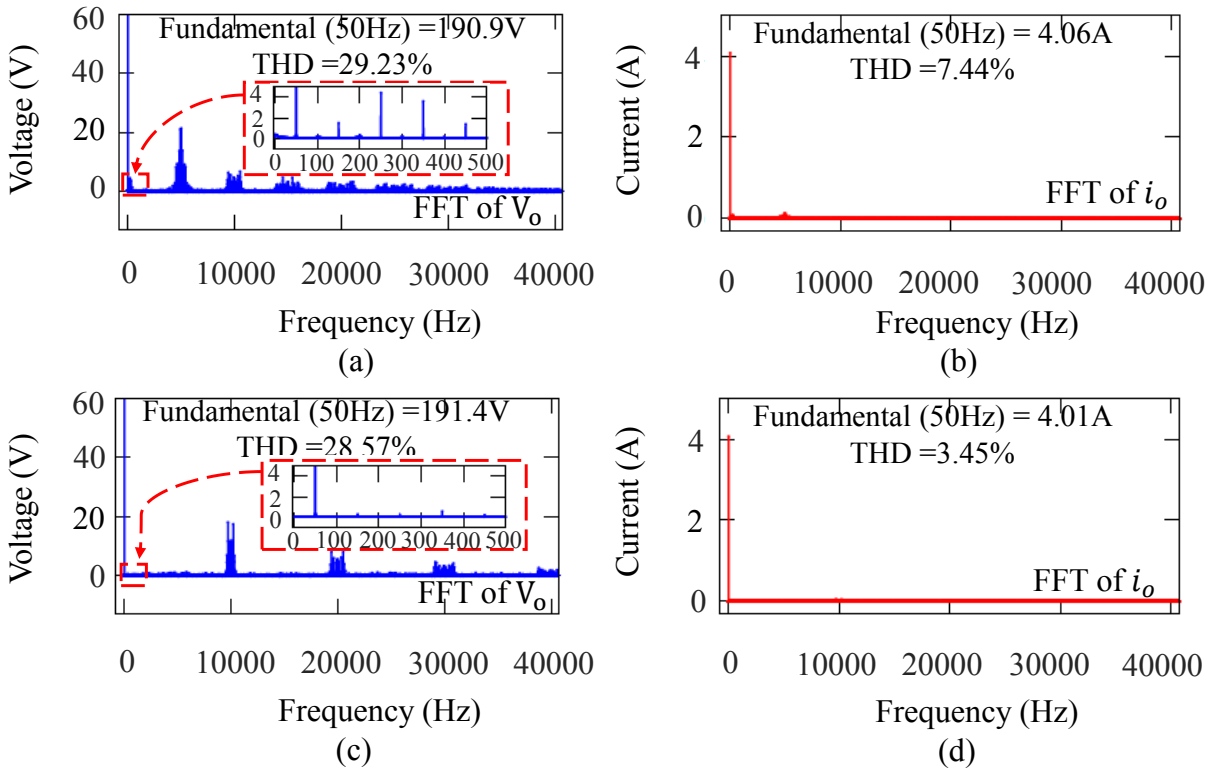


Figure 3.17: FFT analysis of the Simulated output voltages and currents ($C_1 = C_2 = 100$ μF and $f_c = 5$ kHz) obtained by (a) and (b) the conventional method, and (c) and (d) the proposed method.

analysis was performed on the generated output load voltage and current during R–L load-

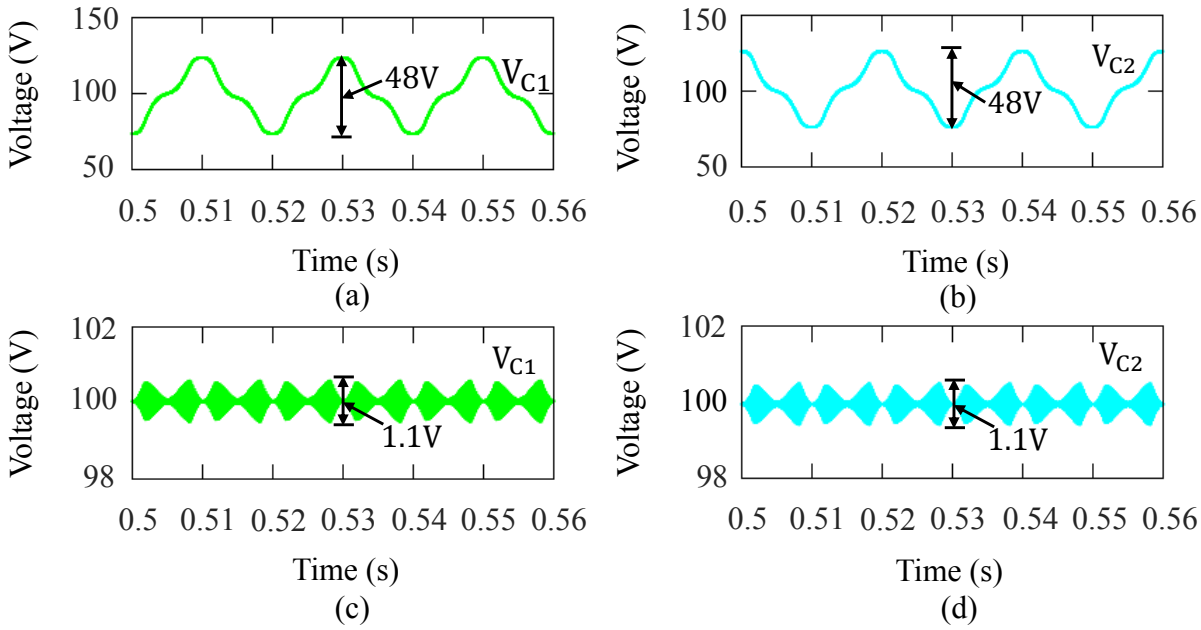


Figure 3.18: Simulated V_{C1} and V_{C2} over three fundamental periods ($C_1 = C_2 = 100$ μF and $f_c = 5$ kHz) obtained by (a) and (b) the conventional method, and (c) and (d) the proposed method.

ing. The results of the conventional and proposed methods are plotted in panels (a)–(b) and (c)–(d) of Fig. 3.17, respectively. Comparing the harmonic spectra of the output voltages in the two methods (Fig. 3.17(a) and (c), respectively), we find that the proposed PS-PWM method considerably reduced the low-order harmonics of the output voltage. The THDs in the generated output voltage and current were 29.23% and 7.44%, respectively under the conventional method, but were reduced to 28.57% and 3.45%, respectively, after employing the proposed PS-PWM. Furthermore, the first switching harmonics of the output voltage in the proposed PS-PWM strategy were at $2f_c$ and other harmonics occurred at integer multiples of the ESF, verifying that odd multiples of f_c were eliminated. Therefore, the proposed PS-PWM maintained the number of carrier crossings as in the classic PS-PWM without invoking the capacitor-voltage balancing scheme.

Fig. 3.18 displays the simulated voltages of the dc-link capacitors under the conventional and proposed methods at $f_c = 5$ kHz. The voltage ripple of the dc-link capacitors was 48 V in the conventional method, but reduced to 1.1 V (0.55% of the total dc voltage) after applying the proposed method. Thus, the proposed PS-PWM method reduced the voltage ripple by 97.7% from that of the conventional method at $f_c = 5$ kHz.

Fig. 3.19 shows the simulated voltages of the dc-link capacitors after increasing the carrier frequency to 10 kHz in both methods. Under the conventional method, the voltage

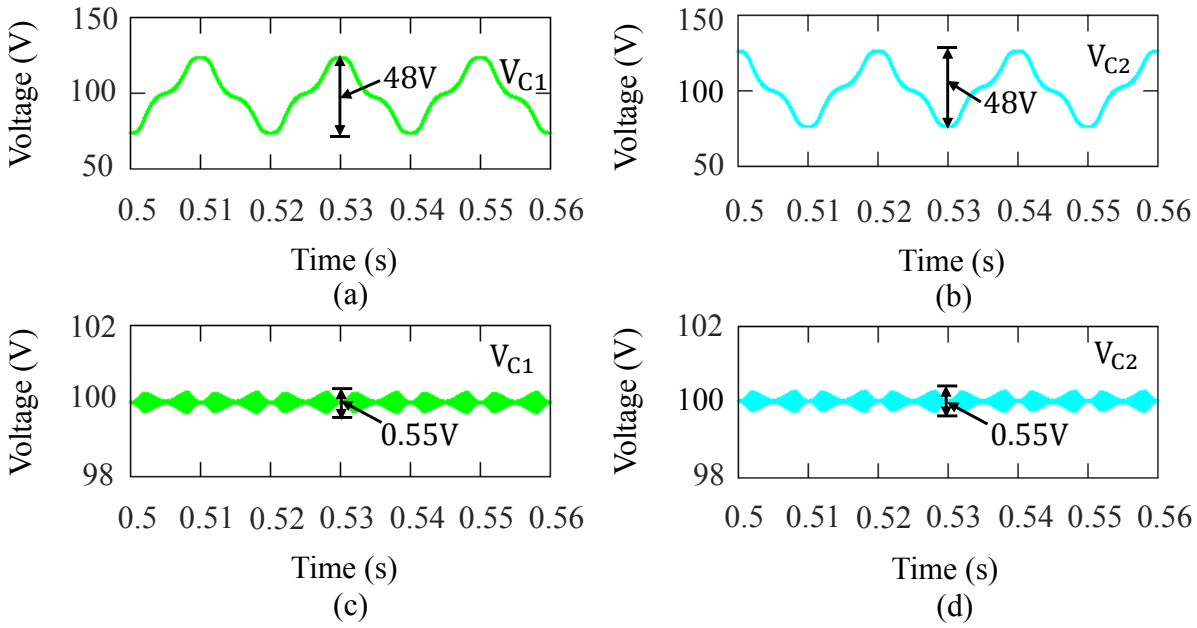


Figure 3.19: Simulated V_{C1} and V_{C2} over three fundamental periods ($C_1 = C_2 = 100$ μF and $f_c = 10$ kHz) obtained by (a) and (b) the conventional method, and (c) and (d) the proposed method.

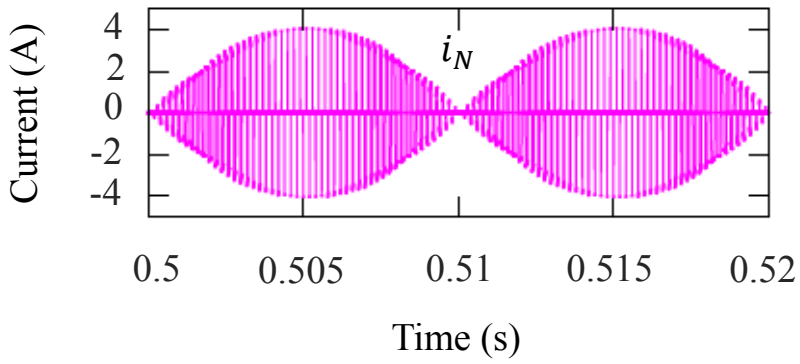


Figure 3.20: Simulated i_N over one fundamental period in the proposed modulation strategy ($f_c = 5$ kHz).

ripple of the dc-link capacitors remained at 48 V, but the proposed method reduced the voltage ripple to 0.55V (only 0.28% of the total dc voltage). This result shows that the proposed PS-PWM method can regulate the dc-link capacitor-voltage ripple by adjusting the carrier frequency.

Fig. 3.20 shows the current of the neutral-potential point during one fundamental period after applying the proposed PS-PWM method at $f_c = 5$ kHz. The current i_N was 4.1 A, the same amplitude as the output current, and both positive and negative polarities

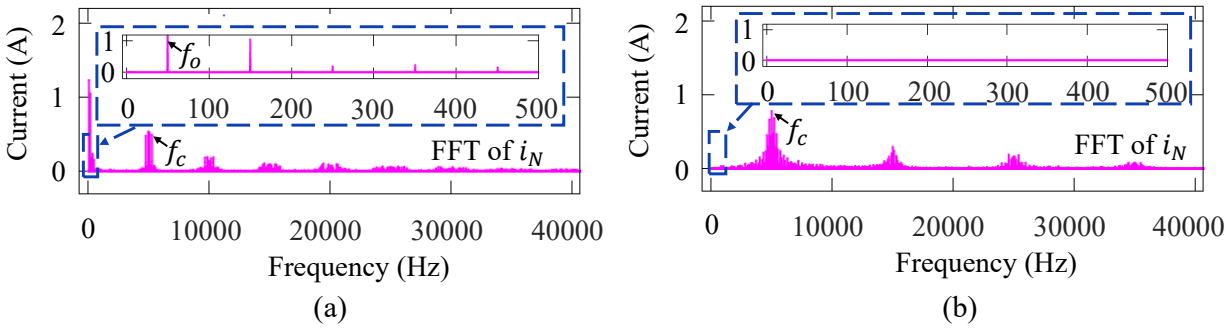


Figure 3.21: FFT analysis of the simulated i_N ($C_1 = C_2 = 100$ μF and $f_c = 5$ kHz) obtained by (a) the conventional method and (b) the proposed method.

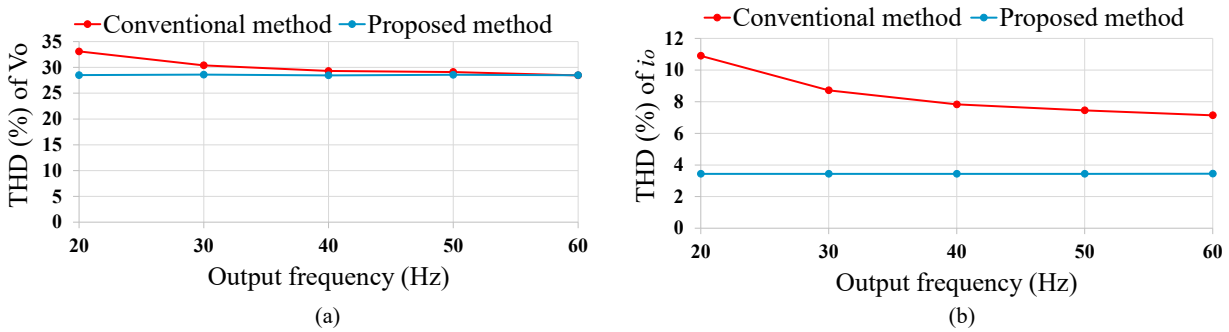
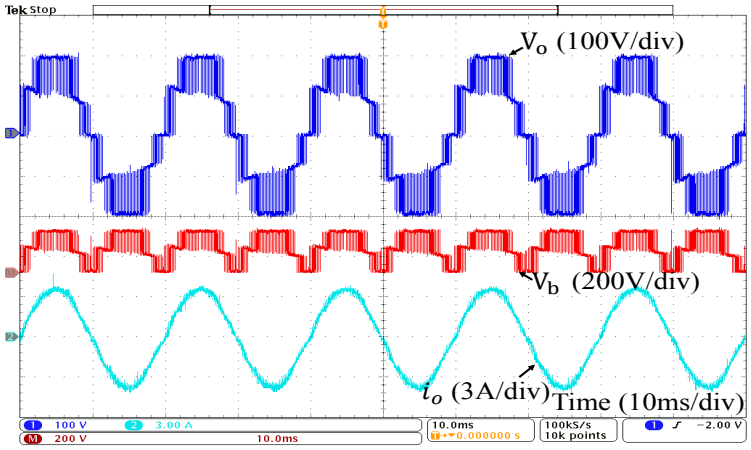


Figure 3.22: Simulated results of the inverter using the conventional and proposed PS-PWM methods showing the THDs of (a) the output voltage and (b) the output current obtained by varying the output frequency ($C_1 = C_2 = 100$ μF and $f_c = 5$ kHz).

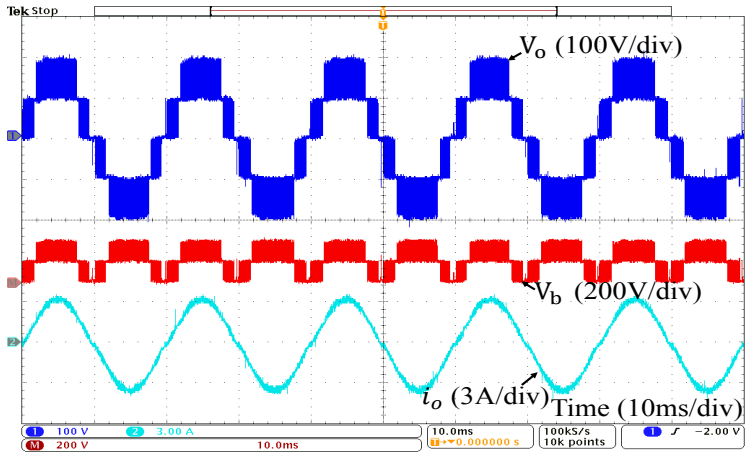
appeared in each half-cycle of the fundamental period. This result verifies the analysis in Table 2.1 and (3.46).

Fig. 3.21 displays the FFT analysis of the simulated current of the neutral-potential point obtained by the conventional and proposed methods at $f_c = 5$ kHz. By comparing the frequency spectra of i_N for the two methods (Figs. 3.21(a) and (b)), it can be seen that the proposed method eliminated the fundamental frequency components of i_N. Thus, in the proposed method, the capacitor-voltage ripple depends only on the switching frequency.

Fig. 3.22 displays the THDs of the simulated output voltage and current obtained by the conventional and proposed methods at $f_c = 5$ kHz when the output frequency varied from 20 to 60 Hz. By comparing the THD response of V_o and i_o for the two methods (Figs. 3.22(a) and (b)), it can be seen that the proposed method maintains the THDs of output voltage and current. In contrast, the THD in the conventional method increases with the decrease in the output frequency. Thus, the proposed method achieves improved power



(a)



(b)

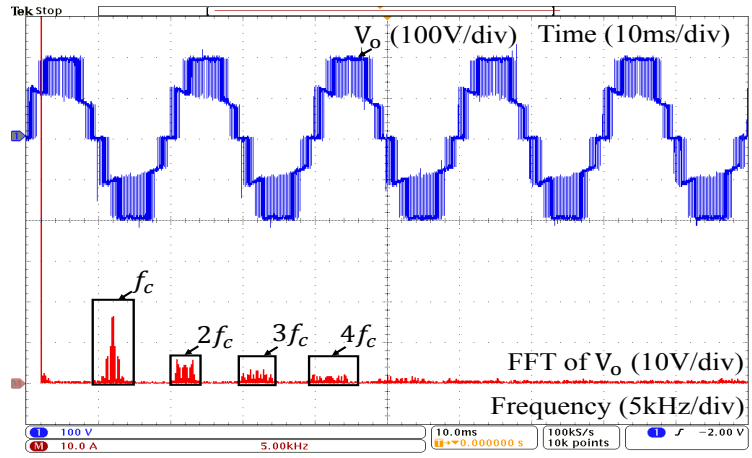
Figure 3.23: Experimental steady-state results of V_o, V_b, and i_o obtained by (a) the conventional method and (b) the proposed method.

quality performance at all output frequencies.

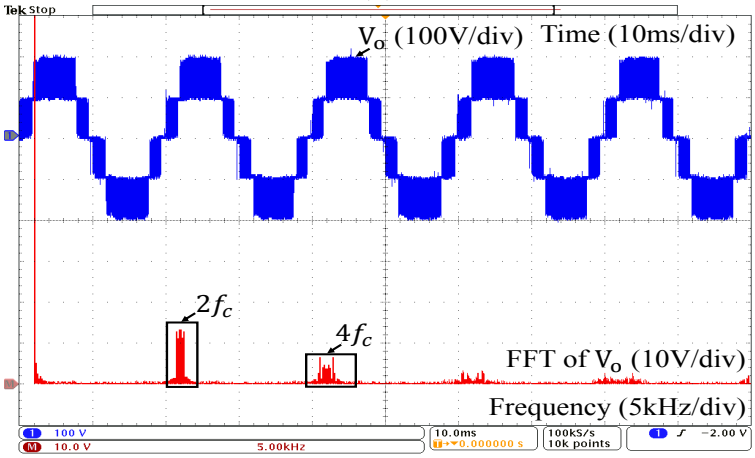
3.8 Experimental Results by the Proposed PS-PWM: A Comparative Investigation

3.8.1 Steady-State Performance

Figs. 3.23–3.26 compare the steady-state results of the proposed PS-PWM and conventional methods implemented on the 5-level hybrid MLDCL inverter with $C = 100$ μF.



(a)

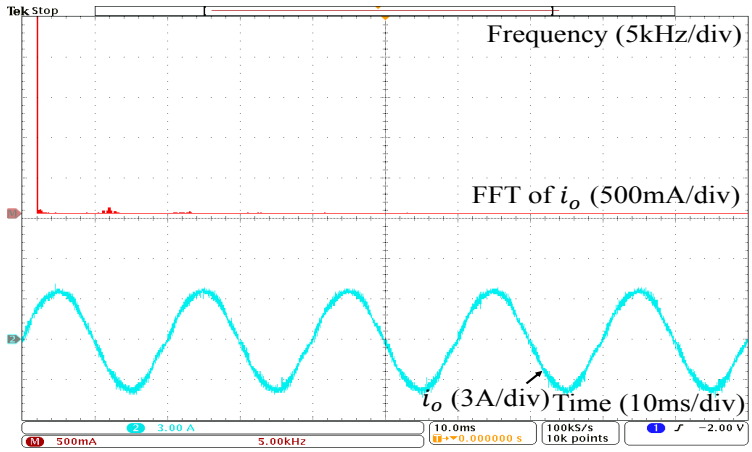


(b)

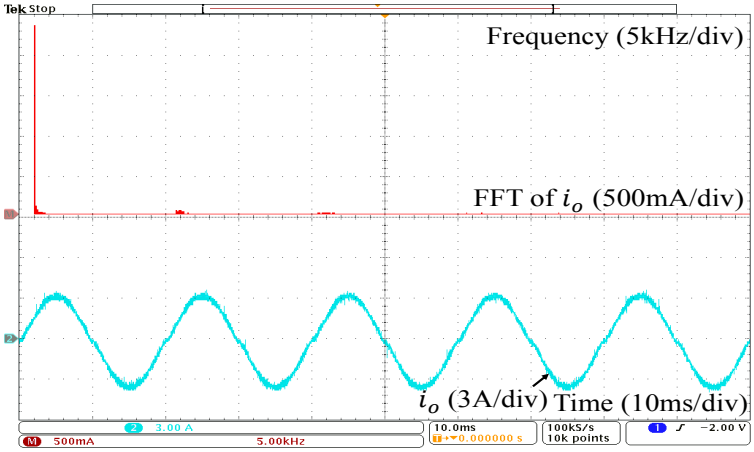
Figure 3.24: Experimental steady-state results of V_o and their FFT-derived harmonic spectra obtained by (a) the conventional method and (b) the proposed method.

Fig. 3.23 shows the generated output voltages, output voltages of the level-generation stage, and output currents when the inverter supplied an R–L load. Notably, both methods obtained a unipolar output voltage in the level-generation stage, as expected from (2.1). However, the generated output voltage and output voltage of the level-generation stage under the conventional method were distorted by high fluctuations of the dc-link capacitor voltage (Fig. 3.23(a)). In contrast, the waveform of the generated output voltage under the proposed method exhibited five levels with a maximum voltage of 200 V, a step voltage of 100 V, and no noticeable distortion (Fig. 3.23(b)).

To confirm the feasibility of the proposed PS-PWM scheme, the generated output voltages and currents in both methods were analyzed using FFT. The corresponding results are shown in Figs. 3.24 and 3.25, respectively. The harmonic spectra of the output voltages



(a)

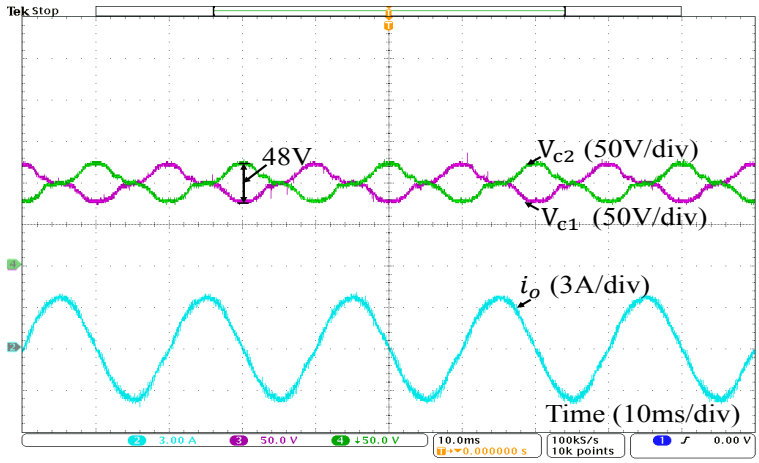


(b)

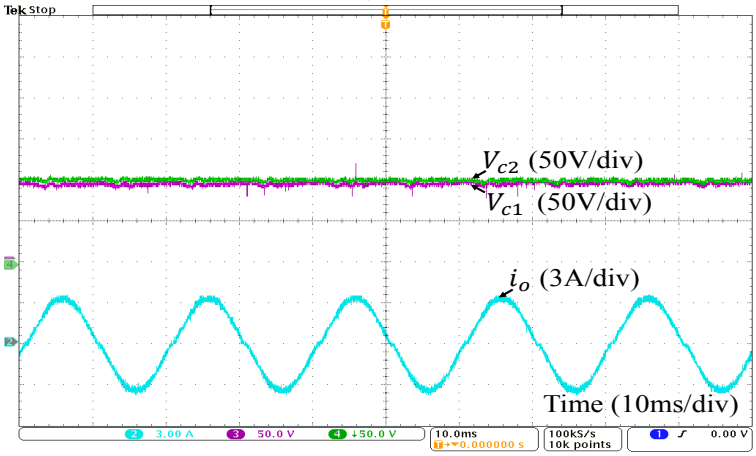
Figure 3.25: Experimental steady-state results of i_o and their FFT-derived harmonic spectra obtained by (a) the conventional method and (b) the proposed method.

and currents were similar to the simulated results of both methods. Moreover, as evidenced in Fig. 3.24(b), the proposed PS-PWM strategy eliminated the harmonics at odd integer multiples of the carrier frequency. Therefore, in the proposed PS-PWM strategy, a THD within the IEEE 519 standard can be achieved with a smaller filter than the conventional method. Examining the first 50 harmonics on the HIOKI power analyzer, the THDs of the generated output voltage and current were 3.72% and 3.49%, respectively, when implementing the conventional method, reducing to 3.51% and 3.45%, respectively, after implementing the proposed PS-PWM strategy. The lower THD in the output voltage of the proposed method was attributed to the reduced number of lower-order harmonics.

Fig. 3.26 shows the dc-link capacitor-voltage balancing in both methods at $f_c = 5$ kHz. The peak–peak voltage ripple of the dc-link capacitor was 48 V after implementing the



(a)



(b)

Figure 3.26: Steady-state experimental results of V_{C1}, V_{C2}, and i_o obtained by (a) the conventional method and (b) the proposed method.

conventional method (Fig. 3.26(a)). The proposed method with the same load and carrier frequency achieved capacitor-voltage (V_{C1} and V_{C2}) balancing at around $\frac{V_{dc}}{2}$, with a small peak–peak voltage ripple of 3.4 V (less than 1.7% of the total dc source voltage; see Fig. 3.26(b)). This result verified that the proposed PS-PWM scheme remarkably reduces the voltage ripple of the dc-link capacitors.

Fig. 3.27 shows the current that flows out of the dc voltage source I_{dc} and the output current after applying the proposed PS-PWM method at $f_c = 5$ kHz. Notably, the current I_{dc} preserved the double-fundamental frequency characteristic (100 Hz, i.e., the period of 10 ms) of the dc source despite the capacitor-voltage balancing in each carrier period. Also, the double-fundamental frequency component does not influence the capacitor voltage ripple (see Appendix).

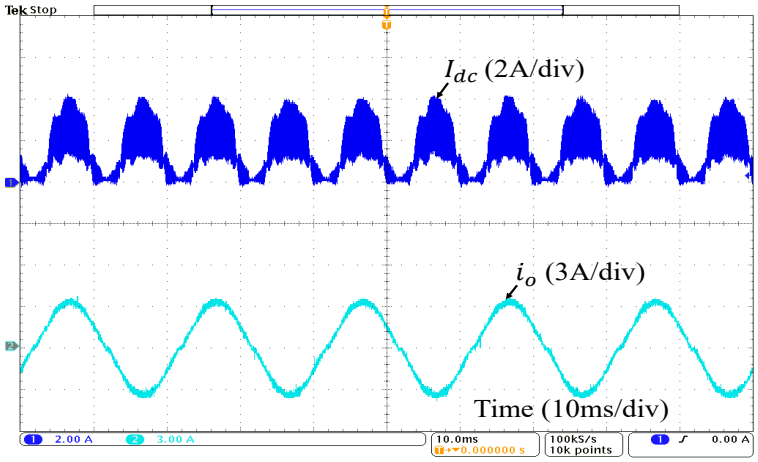


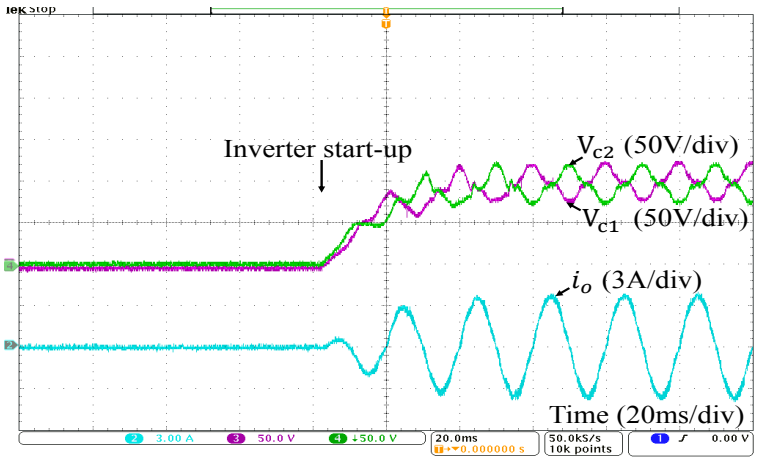
Figure 3.27: Experimental results of the current that flows out of the dc voltage source I_{dc} and i_o obtained by the proposed method.

3.8.2 Transient-State Performance

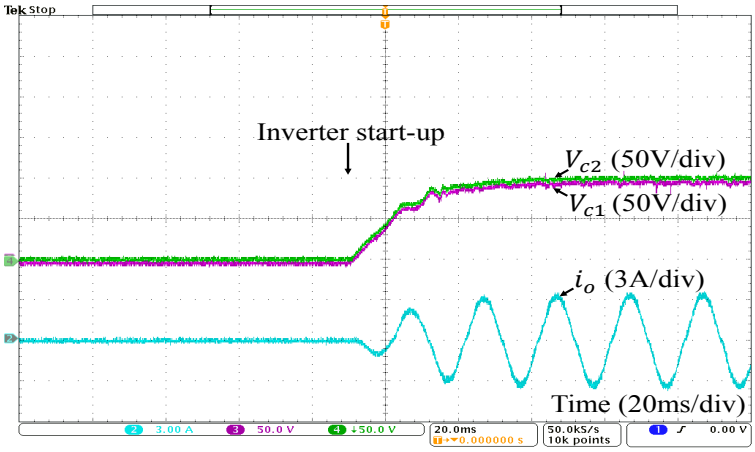
The transient analyses were carried out on the 5-level hybrid MLDCL inverter with $C = 100$ μF and $f_c = 5$ kHz. These analyses examined the dynamic performances of the capacitor-voltage balancing in the two methods.

Fig. 3.28 shows the dc-link capacitor voltages and output currents of the inverter when started on-load. As confirmed in the capacitor-voltage plots of both methods, no precharged capacitor was needed during the start-up of the inverter. After implementing the conventional method, the transient response time of the dc-link capacitors was 60 ms and a high voltage ripple was observed (Fig. 3.28(a)), but the proposed PS-PWM method reduced the transient response time to less than 45 ms and greatly attenuated the voltage ripple (Fig. 3.28(b)). When employing small-size capacitors, the proposed method reduces the danger of breaking the switching devices by diminishing the voltage ripples and shortening the time of charging the capacitors during the inverter start-up. These advantages of the proposed PS-PWM method increase the reliability of the inverter.

Next, a sudden load change from $R = 48$ Ω, $L = 10$ mH to $R = 148$ Ω, $L = 10$ mH was imposed on the 5-level hybrid MLDCL inverter. The results of both methods are shown in Fig. 3.29. When implementing the conventional method, the dc-link capacitors were unbalanced by sudden load change (Fig. 3.29(a)). The peak voltage shifted by 10 V from the balanced state and recovered its balance after around 200 ms. In contrast, the proposed PS-PWM method instantly recovered and maintained a balanced voltage of the dc-link capacitors after the load shock (Fig. 3.29(b)). The negligible voltage shift and the short recovery time exhibited by the proposed PS-PWM are attributable to the improved sensitivity of the dc-link to load changes. As demonstrated in the dynamic



(a)

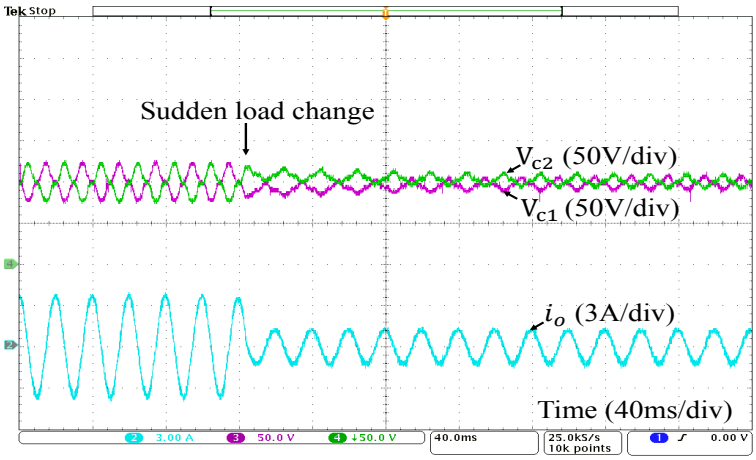


(b)

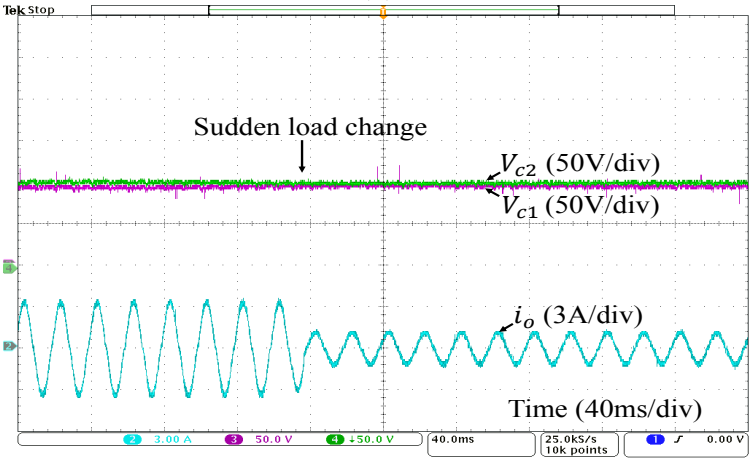
Figure 3.28: Transient-state experimental results of V_{C1}, V_{C2}, and i_o during start-up of the inverter, obtained by (a) the conventional method and (b) the proposed method.

analyses, the proposed capacitor-voltage balancing scheme is feasible and fast even under transient conditions.

Additionally, to verify the effectiveness of the proposed scheme in balancing the capacitor voltages, a resistor $R_C = 100\ \Omega$ was connected in parallel with C_2 through a switch S_C to emulate an unbalanced state of the capacitor voltages. The experimental circuit diagram is presented in Fig. 3.30(a). In this experiment, the capacitor voltages started under unbalanced states, and then the capacitor-voltage balancing scheme was enabled to balance the capacitor voltages. Notably, the proposed scheme balanced the capacitor voltages even under heavily unbalanced conditions (Fig. 3.30(b)).



(a)

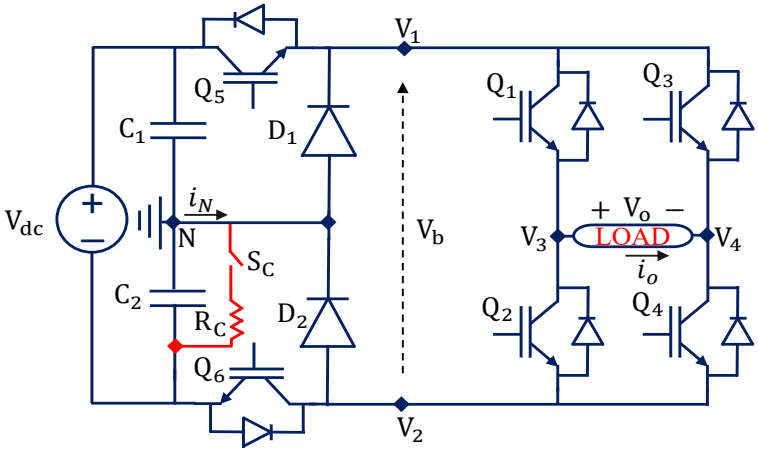


(b)

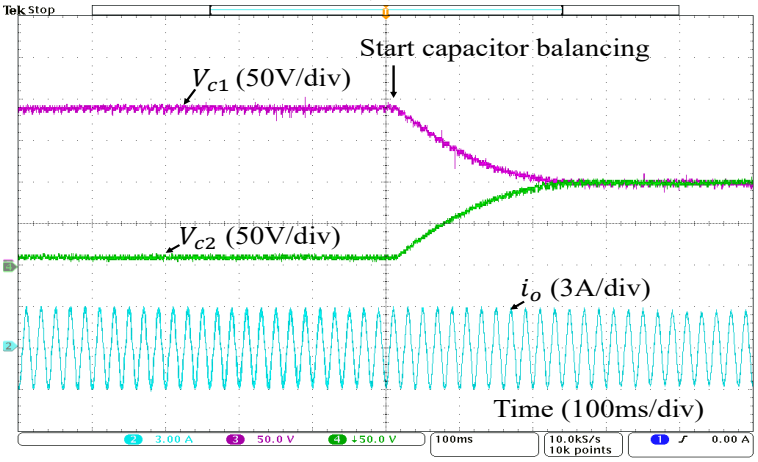
Figure 3.29: Transient-state experimental results of V_{C1}, V_{C2}, and i_o during a sudden load change from $R = 48\ \Omega$, $L = 10$ mH to $R = 148\ \Omega$, $L = 10$ mH, obtained by (a) the conventional method and (b) the proposed method.

3.8.3 Inverter Efficiency Analysis

Finally, the efficiency of the 5-level hybrid MLDCL inverter was experimentally evaluated under the same load ($R = 48\ \Omega$, $L = 10$ mH) for both methods. After implementing the conventional and the proposed PS-PWM methods, the measured total power losses were 9.60 W and 9.68 W; consequently, the experimental efficiencies of the inverter were 97.3% and 97.26%, respectively. The slightly lower efficiency of the proposed PS-PWM method than the conventional method can be explained by the increased switching loss. However, this trade-off did not lessen the contributions of the proposed method: a 90% reduction of the dc-link capacitance and a 97.7% reduction in the capacitor-voltage ripple, as mentioned earlier. It is worth noting that the HIOKI PW6001 during efficiency measurements has



(a)



(b)

Figure 3.30: Experimental transient-state of the proposed voltage-balancing scheme. (a) Circuit diagram when the resistor is connected in parallel with C_2, and (b) results of V_{C1}, V_{C2}, and i_o.

the basic accuracy of ± 0.02% reading (rdg.), ±0.02% full scale (f.s.) [77].

3.9 Proposed Single-Carrier PWM Scheme

Based on Table 2.1, the single-carrier PWM (SC-PWM) scheme was developed to generate the switching patterns for Q_6 and Q_5. In the proposed SC-PWM, S_{Q6} and S_{Q5} were synthesized through logical functions when one triangular carrier v_{cr} of frequency f_c and peak amplitude A_c was compared with two quasi-reference voltages v_{ref1} and v_{ref2}, which demonstrated two unipolar peaks at the fundamental frequency with a peak amplitude of A_r, though phase-shifted by 180° (see Fig. 3.31). As the switching patterns are synthesized

using one carrier, the proposed method can be implemented using a low-cost digital signal processor with a limited number of PWM timers. Additionally, the two quasi-reference voltages can be obtained easily as

$$v_{ref1} = |v_{ref}|, \tag{3.51}$$

$$v_{ref2} = A_c - |v_{ref}| \tag{3.52}$$

where v_{ref} is the bipolar reference voltage with a peak amplitude A_r and fundamental frequency.

The quasi-reference voltages for S_{Q6} and S_{Q5} were selected by considering their limiting conditions: $0 \leq v_{ref1} \leq \frac{1}{2}$ and $\frac{1}{2} \leq v_{ref1} \leq 1$, and $\frac{1}{2} \leq v_{ref2} \leq 1$ and $0 \leq v_{ref2} \leq \frac{1}{2}$ for v_{ref1} and v_{ref2}, respectively. The quasi-reference voltages were synthesized logically to generate the half-wave and quarter-wave symmetry of the voltage V_b. This approach reduces the THD of the generated inverter voltage. Fig. 3.32 shows the selection of quasi-reference voltages, triangular carrier, and the switching patterns synthesized during two carrier periods under the aforementioned limiting conditions. Under the conditions $0 \leq v_{ref1} \leq \frac{1}{2}$ and $\frac{1}{2} \leq v_{ref2} \leq 1$ (see Fig. 3.32(a)), two voltage levels were produced as follows:

$$q_0 = \left[\left(0 \leq v_{ref1} \leq \frac{1}{2}\right) \wedge (v_{ref1} \geq v_{cr})\right] \wedge \left[\left(\frac{1}{2} \leq v_{ref2} \leq 1\right) \wedge (v_{ref2} \leq v_{cr})\right], \tag{3.53}$$

where q_0 is the switching pattern function of Q_6 and Q_5 for synthesizing a zero voltage. The zero voltage level is obtained in the first set of limiting conditions, when the carrier is less or equal to the unipolar quasi-reference voltage signal in the range from 0 to $\frac{1}{2}$, and greater or equal to the quasi-reference voltage signal in the range from $\frac{1}{2}$ to 1, simultaneously, as denoted in (3.53).
To obtain the first $V_b = \frac{V_{dc}}{2}$, the quasi-reference voltages can be decided as

$$q_{\frac{1}{2}-1} = \left[\left(0 \leq v_{ref1} \leq \frac{1}{2}\right) \wedge (v_{ref1} \geq v_{cr})\right] \vee \left[\left(\frac{1}{2} \leq v_{ref2} \leq 1\right) \wedge (v_{ref2} \leq v_{cr})\right], \tag{3.54}$$

where $q_{\frac{1}{2}-1}$ is the switching pattern function of Q_6 and Q_5 generating $V_b = \frac{V_{dc}}{2}$. The half-full dc voltage level is obtained in the first set of limiting conditions, when the carrier is either less or equal to the unipolar quasi-reference voltage signal in the range from 0 to $\frac{1}{2}$, or greater or equal to the quasi-reference voltage signal in the range from $\frac{1}{2}$ to 1, as denoted in (3.54). To ensure capacitor-voltage balancing, (3.54) must be equally allocated to Q_6 and Q_5 as follows:

$$q_{Q5-1} = \left(0 \leq v_{ref1} \leq \frac{1}{2}\right) \wedge (v_{ref1} \geq v_{cr}), \tag{3.55}$$

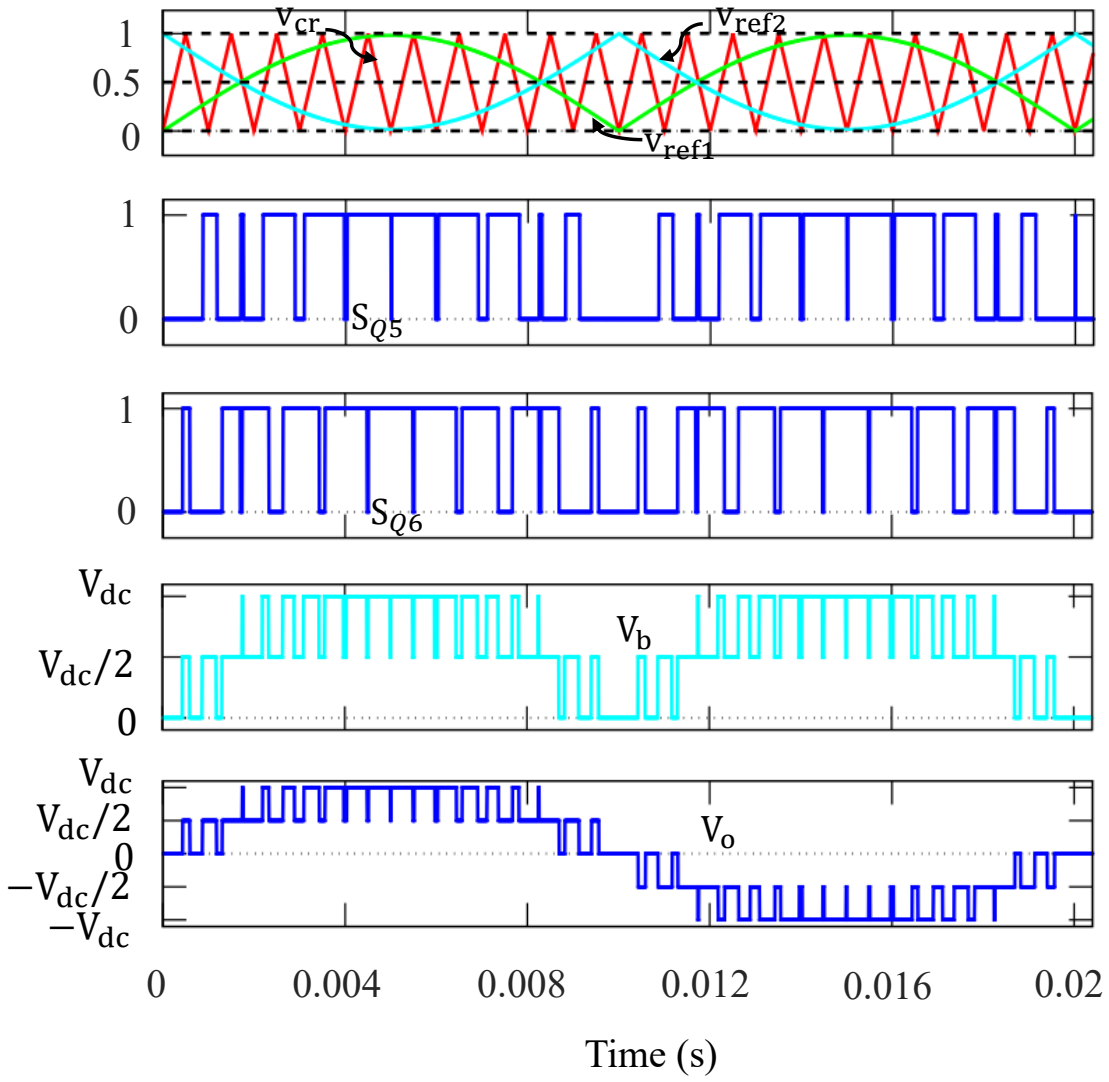


Figure 3.31: Proposed SC-PWM scheme and output voltage of the 5-level hybrid MLDCL inverter at $f_c = 1$ kHz.

$$q_{Q6-1} = \left(\frac{1}{2} \leq v_{ref2} \leq 1\right) \wedge (v_{ref2} \leq v_{cr}) \tag{3.56}$$

where q_{Q5-1} and q_{Q6-1} are the switching pattern functions of Q_5 and Q_6, respectively for generating $V_b = \frac{V_{dc}}{2}$.

Furthermore, under the other set of conditions ($\frac{1}{2} \leq v_{ref1} \leq 1$ and $0 \leq v_{ref2} \leq \frac{1}{2}$ in Fig. 3.32(b)), the choices of the quasi-reference voltages were determined as explained below.

To obtain the second half-full dc voltage under these conditions, the quasi-reference voltages can be selected as

$$q_{\frac{1}{2}-2} = \left[\left(\frac{1}{2} \leq v_{ref1} \leq 1\right) \wedge (v_{ref1} < v_{cr})\right] \vee \left[\left(0 \leq v_{ref2} \leq \frac{1}{2}\right) \wedge (v_{ref2} > v_{cr})\right], \tag{3.57}$$

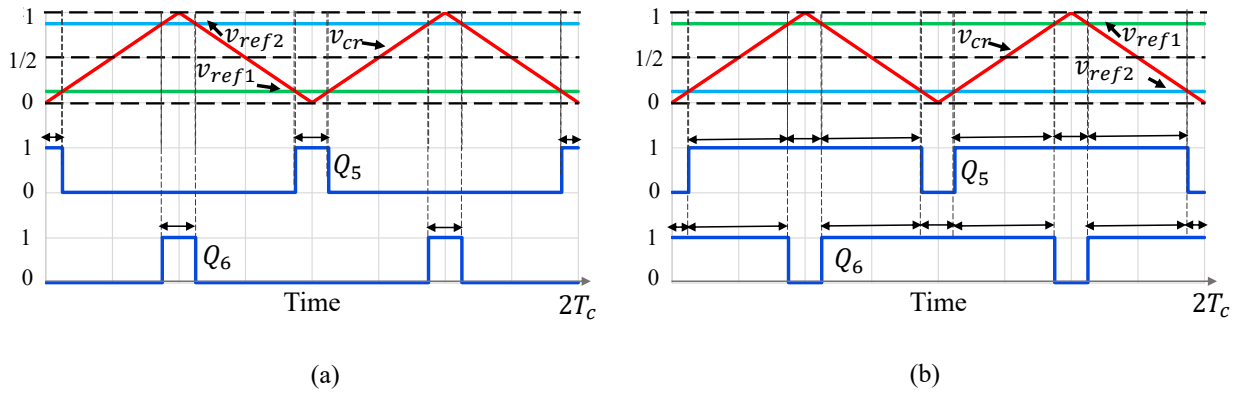


Figure 3.32: Selection of quasi-reference voltages and sequence of switching signals in the proposed single-carrier PWM scheme: (a) $0 \leq v_{ref1} \leq \frac{1}{2}$ and $\frac{1}{2} \leq v_{ref2} \leq 1$, and (b) $\frac{1}{2} \leq v_{ref1} \leq 1$ and $0 \leq v_{ref2} \leq \frac{1}{2}$, where v_{ref1} and v_{ref2} are the unipolar sinusoidal quasi-reference voltages.

where $q_{\frac{1}{2}-2}$ is the switching pattern function of Q_6 and Q_5 generating the second half-full voltage. The half-full dc voltage level is obtained in the second set of limiting conditions, when the carrier is either greater than the unipolar quasi-reference voltage signal in the range from $\frac{1}{2}$ to 1, or less than the quasi-reference voltage signal in the range from 0 to $\frac{1}{2}$, as denoted in (3.57). To ensures the capacitor-voltage balancing, (3.57) must be equally allocated to Q_5 and Q_6 as follows:

$$q_{Q5-2} = \left(\frac{1}{2} \leq v_{ref1} \leq 1\right) \wedge (v_{ref1} < v_{cr}), \tag{3.58}$$

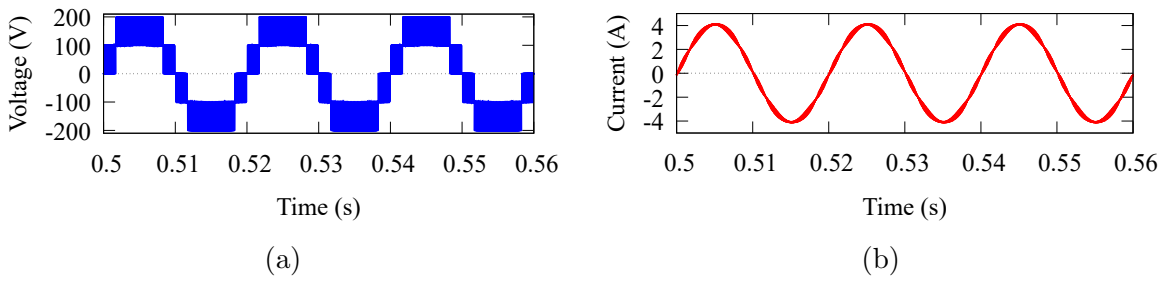
$$q_{Q6-2} = \left(0 \leq v_{ref2} \leq \frac{1}{2}\right) \wedge (v_{ref2} > v_{cr}) \tag{3.59}$$

where q_{Q5-2} and q_{Q6-2} are the switching pattern functions of Q_5 and Q_6, respectively for generating the second half-full voltage. To generate the full dc voltage, the quasi-reference voltages can be decided as

$$q_1 = \left[\left(\frac{1}{2} \leq v_{ref1} \leq 1\right) \wedge (v_{ref1} \geq v_{cr})\right] \wedge \left[\left(0 \leq v_{ref2} \leq \frac{1}{2}\right) \wedge (v_{ref2} \leq v_{cr})\right], \tag{3.60}$$

where q_1 is the switching pattern function of Q_5 and Q_6 for synthesizing the full dc voltage. The full dc voltage level is generated in the second set of limiting conditions, when the carrier is less or equal to the unipolar quasi-reference voltage signal in the range from $\frac{1}{2}$ to 1, and greater or equal to the quasi-reference voltage signal in the range from 0 to $\frac{1}{2}$, simultaneously, as shown in (3.60).

The complete logical switching functions of Q_5 and Q_6 were obtained by merging (using OR gate) their corresponding logical switching functions (deduced above) into a single



(a) (b)

Figure 3.33: Simulated results obtained by the proposed SC-PWM method: (a) the output voltage and (b) output current.

logical switching function for each controlled-switching device. S_{Q5} and S_{Q6} are then described by (3.61) and (3.62), respectively.

$$S_{Q5} = q_0 \vee q_{Q5-1} \vee q_{Q5-2} \vee q_1. \tag{3.61}$$

$$S_{Q6} = q_0 \vee q_{Q6-1} \vee q_{Q6-2} \vee q_1. \tag{3.62}$$

In the proposed SC-PWM strategy, like the proposed PS-PWM, the ESF of the output voltage is $2f_c$. Hence, the first switching harmonic cluster of the output voltage has a frequency of $2f_c$ and other high-frequency harmonic clusters occur at integer multiples of ESF. This modulation scheme is easy to implement using comparators and logic gates.

3.10 Simulation Results by the Proposed SC-PWM: A Comparative Analysis

The 5-level hybrid MLDCL inverter with the proposed SC-PWM scheme presented in Section 3.9 was simulated in the PSIM software environment. The conventional method was also simulated as a benchmark. The circuit parameters are listed in Table 2.2.

Fig. 3.33 displays the simulated output voltage and current of the 5-level hybrid MLDCL inverter after applying the proposed SC-PWM scheme. Notably, the generated output voltage has five output levels as expected from (2.3) (Fig. 3.33a). Moreover, the output current is almost pure sinusoidal with less distortion (Fig. 3.33b). To confirm the performance of the proposed SC-PWM, the FFT analysis was performed on the output voltage and current, and it was observed that the THDs of output voltage and current were 28.07% and 3.39%, respectively.

Fig. 3.34 displays the simulated voltages of the dc-link capacitors under the conventional method and proposed SC-PWM method at $f_c = 5$ kHz. The voltage ripple of the

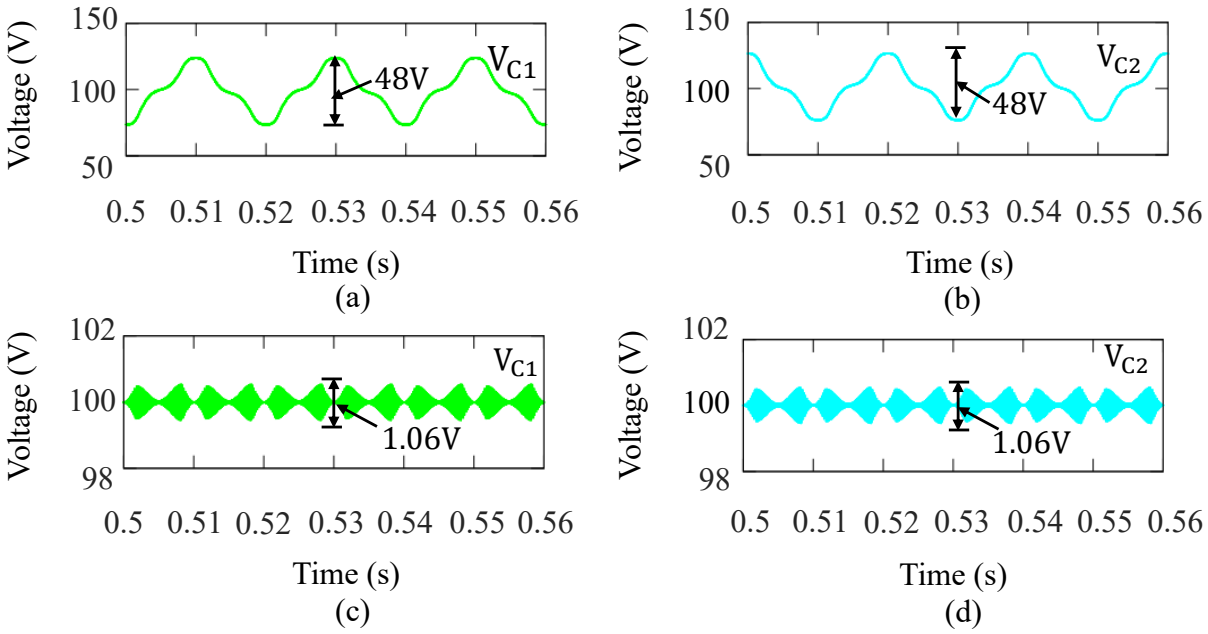


Figure 3.34: Simulated V_{C1} and V_{C2} over three fundamental periods ($C_1 = C_2 = 100$ μF and $f_c = 5$ kHz) obtained by (a) and (b) the conventional method, and (c) and (d) the proposed SC-PWM method.

dc-link capacitors was 48 V in the conventional method, but reduced to 1.06 V (0.53% of the total dc voltage) after applying the proposed SC-PWM method. Thus, the proposed SC-PWM method reduced the voltage ripple by 97.8% from that of the conventional method at $f_c = 5$ kHz.

Fig. 3.35 displays the simulated voltage ripples of the dc-link capacitors under the conventional method and proposed SC-PWM method at $f_c = 5$ kHz. The voltage ripple of the dc-link capacitors increased with decrease in the output frequency in the conventional method, but maintained at 1.06 V after applying the proposed SC-PWM method. Thus, the proposed SC-PWM method achieves constant capacitor-voltage ripple at all output frequencies.

3.11 Summary

In this chapter, the conventional LS-PWM strategy, the operating principle of the hybrid multilevel dc-link (MLDCL) inverter under the conventional strategy, and its impact on the dc-link capacitor voltages ripple were studied. Moreover, detailed modeling, analysis, and verification of the proposed modulation strategies were provided. Notably, the proposed switching and voltage-balancing schemes are easy to implement using only comparators

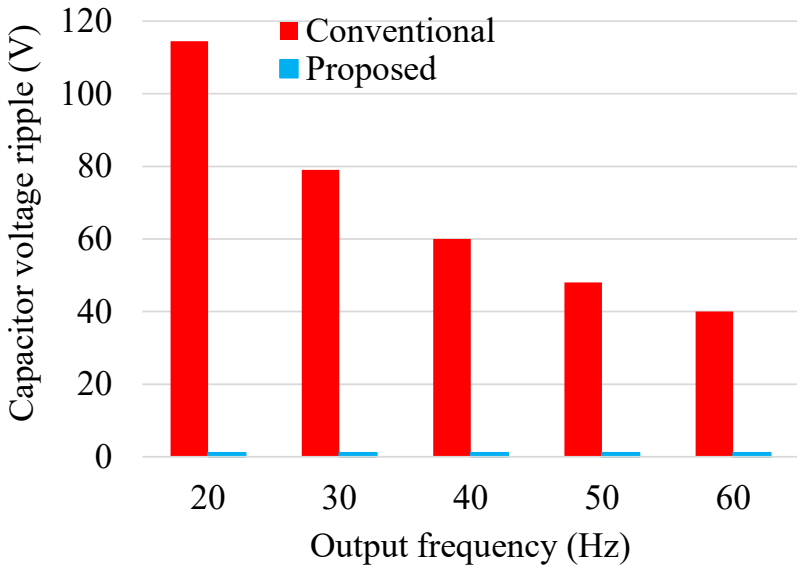


Figure 3.35: Simulated dc-link capacitor voltage ripples obtained by varying output frequency of the inverter using the conventional and proposed SC-PWM methods ($C_1 = C_2 =$ 100 μF and $f_c = 5$ kHz).

and logic gates, thereby reducing the control complexity. The dc-link capacitor voltage was balanced in both steady-state and dynamic operations, demonstrating the feasibility of the proposed voltage-balancing scheme despite having lower control complexity than the conventional method. Finally, the detailed performance experimental validations and comparative investigations of the proposed modulation schemes over the conventional scheme were provided in this chapter. It was depicted that the proposed modulation schemes reduce the capacitor voltage ripple by 97.7% at f_c =5 kHz from that of the conventional schemes while reducing the THDs of output voltage and current. Unlike the conventional strategy, in the proposed schemes, the dc-link capacitor voltage ripple can be adjusted by regulating the carrier frequency.

Chapter 4

Design of DC-Link Capacitors, Filter Circuit, and a Comparative Study

This chapter describes detailed guidelines for designing the dc-link capacitors and LC filter circuit for the single-phase 5-level hybrid MLDCL inverter under the proposed PWM strategies in comparison with the conventional method. Therefore a step-by-step mathematical design formulation is provided for the reader to grasp the entire working principle of the inverter. Moreover, simulation and experimental validations at different working conditions are conducted to confirm the performance of the inverter under the designed new features.

4.1 Determination of Capacitors Using the Proposed Methods

The dc-link capacitor design is determined by its voltage ripple. As discussed earlier, the capacitor charge is balanced in each carrier period, which leads the capacitor-voltage ripple to depend on the carrier frequency. Thus, the maximum capacitor voltage ripple is given by

$$\Delta V_{Cm} = \frac{\Delta Q_{Cm}}{C} = \frac{I_{om}}{C} t_{ch} \tag{4.1}$$

where ΔQ_{Cm} is the maximum differential charge in the capacitor when the capacitor charges/discharges and t_{ch} is the maximum charging/discharging time in the carrier period. The maximum value of t_{ch} is equal to $\frac{T_c}{2} = \frac{1}{2f_c}$. Then, ΔV_{Cm} in (4.1) can be expressed, as

$$\Delta V_{Cm} = \frac{I_{om}}{2Cf_c}. \tag{4.2}$$

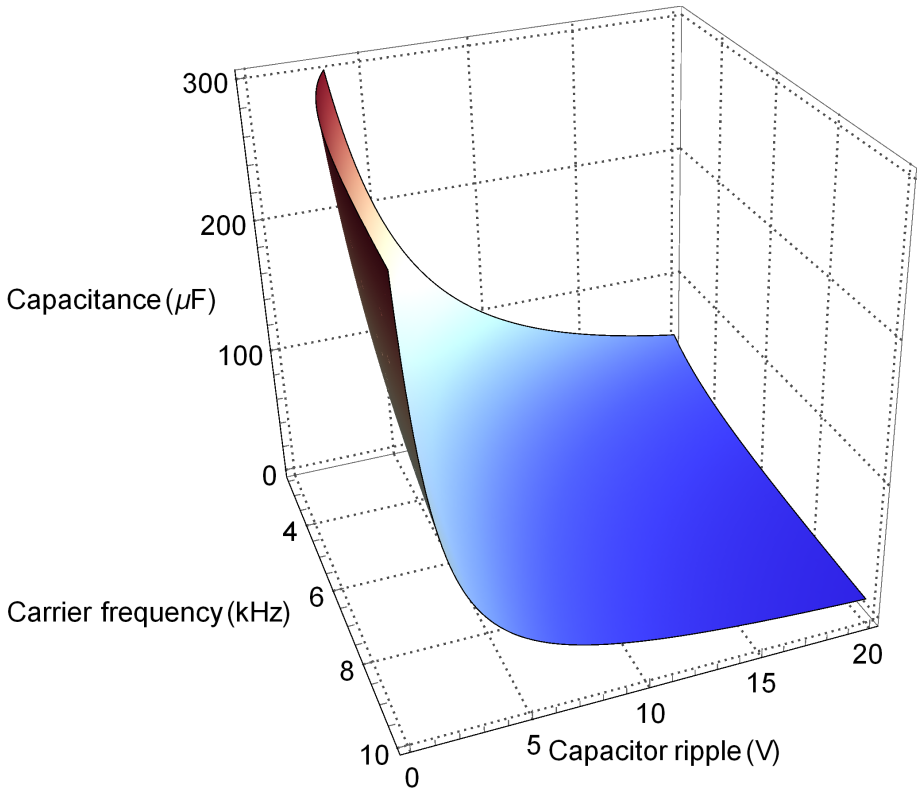


Figure 4.1: 3-D plot relating the dc-link capacitance, maximum capacitor-voltage ripple, and carrier frequency in the proposed method with a maximum load current $I_{om} = 5$ A.

From (4.2), the desired dc-link capacitance C can be selected as

$$C = \frac{I_{om}}{2\Delta V_{Cm} f_c}. \tag{4.3}$$

As indicated in (4.3), the desired dc-link capacitance in the proposed modulation method depends on the maximum allowable voltage ripple, the maximum load current, and the carrier frequency. In the conventional method, the dc-link capacitance depends on the fundamental frequency, the maximum allowable voltage ripple, and maximum load current (see (3.3)). Therefore, the proposed method reduces the capacitance in the conventional method by a factor of the frequency modulation ratio ($m_f = \frac{f_c}{f_o}$).

Fig. 4.1 demonstrates that in the proposed method, the dc-link capacitance and capacitor voltage ripple can be reduced by increasing the carrier frequency. For example, suppose that $I_{om} = 5$ A, $f_c = 5$ kHz, and $\Delta V_{Cm} = 5$ V. The dc-link capacitance in the proposed modulation method is then calculated as

$$C = \frac{I_{om}}{2\Delta V_{Cm} f_c} = 100\mu F. \tag{4.4}$$

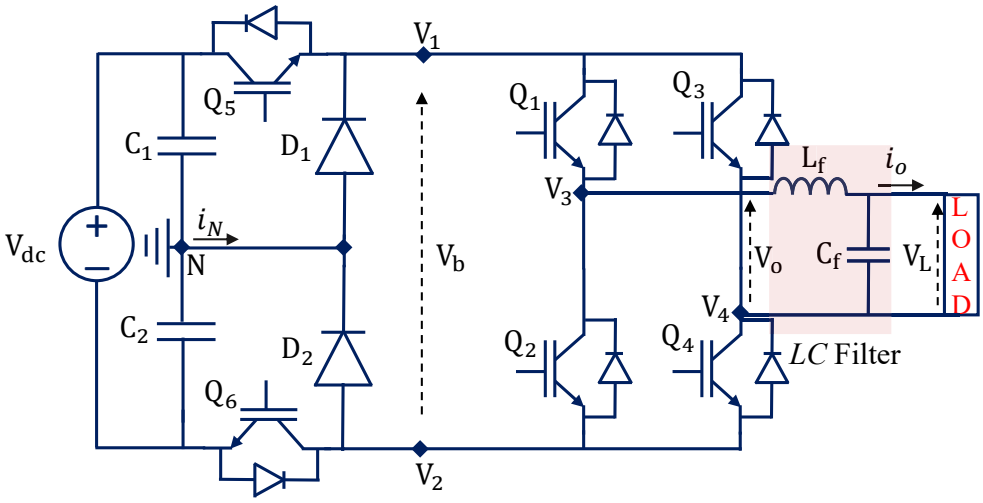


Figure 4.2: Circuit diagram for LC filter design in the 5-level hybrid MLDCL inverter.

Comparing the dc-link capacitances in the conventional and proposed methods, we find that the proposed method reduces the capacitance by a factor of 10.

From (4.2) and the operation of the inverter, we infer that the capacitor-voltage ripples depend on the carrier frequency. Hence, the bulky electrolytic capacitors can be replaced by small-size dc-link capacitors such as ceramic or film capacitors [79, 80], thereby enhancing the power density of the inverter.

4.2 Design of *LC* Filter Using the Proposed Schemes

The filter circuit is required in some applications of the MLIs to reduce the harmonic contents in the output voltage and current. In this study, an LC filter is designed for a 5-level hybrid MLDCL inverter.

The filter inductor is designed based on the ouput current ripple. The output current ripple Δi_o is given as

$$\Delta i_o = \begin{cases} \frac{mV_{dc}(1-2m)}{(n-1)L_f f_{ESF}}, & \text{for } m \leq 0.5, \\ \frac{V_{dc}(m-0.5)(1-2(m-0.5))}{(n-1)L_f f_{ESF}}, & \text{for } m > 0.5, \end{cases} \tag{4.5}$$

where n is the number of voltage levels, m is the modulation index, f_{ESF} is the equivalent switching frequency, and V_{dc} is the dc source voltage. It can be observed that the output current ripple has two similar peaks at m=0.25 and 0.75. Thus, the peak output current ripple is given as

$$\Delta i_{op} = \frac{V_{dc}}{8(n-1)L_f f_{ESF}}. \tag{4.6}$$

Table 4.1:
Simulation Parameters When Using Filter Circuit

Parameter	Symbol	Value
DC-link voltage	V_{dc}	200 V
DC-link capacitance	$C_1 = C_2$	100 μF
Carrier frequency	f_c	5 kHz
Modulation index	m	0.98
Fundamental frequency	f_o	50 Hz
Load resistor	R	48 Ω
Filter inductance	L_f	2 mH
Filter capacitance	C_f	10 μF

For a single-phase 5-level hybrid MLDCL inverter, (4.6) can be improved as

$$\Delta i_{op} = \frac{V_{dc}}{32 L_f f_{ESF}}. \tag{4.7}$$

In applications, it is recommended for the output current ripple to be within 5-10% of the rated output current of the inverter [65], [81], [82]. Thus, the filter inductor can be designed as

$$L_f = \frac{V_{dc}}{32 \Delta i_{op} f_{ESF}}. \tag{4.8}$$

The filter capacitor is designed based on the cut-off frequency of LC filter circuit. The cut-off frequency $f_c - off$ is given as

$$f_{c-off} = \frac{1}{2\pi\sqrt{C_f L_f}}. \tag{4.9}$$

where C_f is filter capacitor. For filter capacitor design, the cut-off frequency is recommended to be 10% of the ESF [65]. Thus, the filter capacitor is given as

$$C_f = \frac{1}{(2\pi \frac{f_{ESF}}{10})^2 L_f}. \tag{4.10}$$

Equation (4.10) can be improved as

$$C_f = \frac{100}{4\pi^2 f_{ESF}^2 L_f}. \tag{4.11}$$

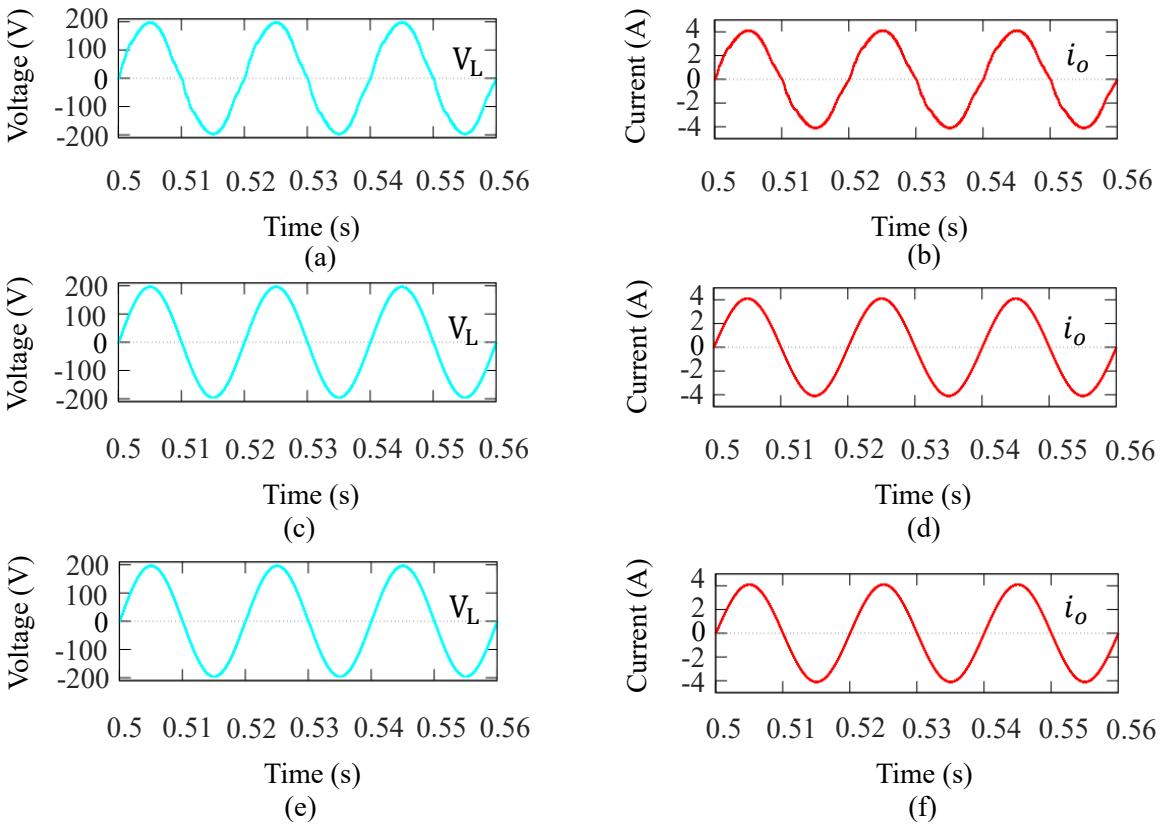


Figure 4.3: Simulated V_L and i_o over three fundamental periods after applying LC filter ($C_1 = C_2 = 100$ μF and $f_c = 5$ kHz) obtained by (a) and (b) the conventional method, (c) and (d) the proposed PS-PWM method. and (e) and (f) the proposed SC-PWM method.

In the conventional method, the required filter inductor is two times, and the capacitor is four times higher than in the proposed method because $f_{ESF} = f_c$ in the conventional method, whereas, in the proposed method $f_{ESF} = 2f_c$. For the rated output current of 2.88 A, $V_{dc} = 200$ V, and ESF of 10 kHz in the proposed methods, a LC filter of 2.17 mH, 11.5 µF was designed. However, the values that are close to the designed parameters (2 mH and 10 µF) which can be found in the industry were selected for the simulation analysis.

4.3 Simulation Results When Using Filter Circuit

The load voltages and output currents of the 5-level hybrid MLDCL inverter were obtained under the conventional method (Fig. 4.3(a)–(b)), the proposed PS-PWM method (Fig. 4.3(c)–(d)), and the proposed SC-PWM (Fig. 4.3(e)–(f)) with $C = 100$ μF, $L_f = 2$ mH, and $C_f = 10$ μF. To confirm the higher performance of the proposed PS-PWM and SC-

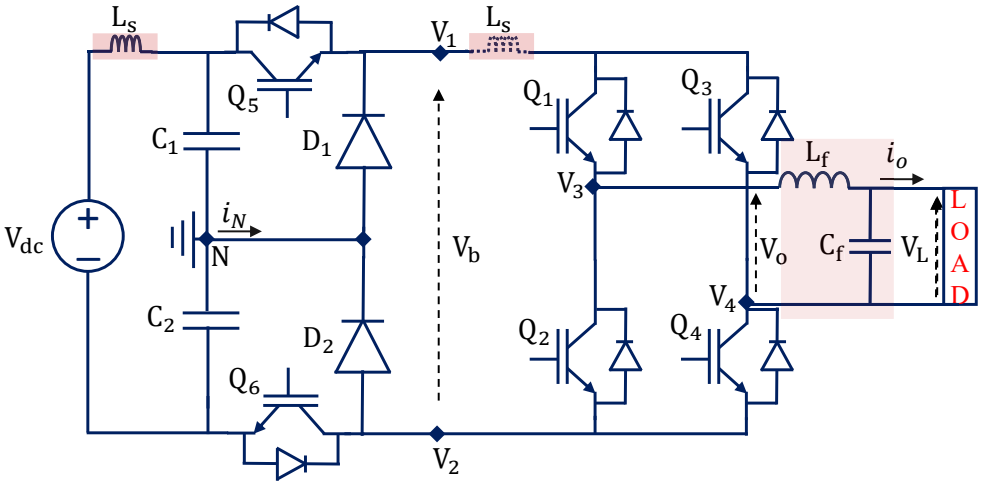


Figure 4.4: Circuit diagram for analyzing the influence of parasitic inductance in the 5-level hybrid MLDCL inverter.

PWM method than the conventional method in the 5-level hybrid MLDCL inverter, an FFT analysis was performed on the load voltage and current. The THDs in both the load voltage and current were 3.76% under the conventional method, but were reduced to 0.47% after employing the proposed PS-PWM. Furthermore, the THDs in both the load voltage and current was reduced to 0.30% after applying the proposed SC-PWM method. Therefore, both proposed methods considerably reduced the THDs of load voltage and current. Although comparing all methods analyzed in this thesis, the proposed SC-PWM has superior power quality performance to the proposed PS-PWM and conventional methods.

On the other hand, some parasitic inductance occurs between the dc voltage source and the dc-link and/or between the level-generation stage and H-bridge module in the NPC-based inverter (see Fig. 4.4). The stray inductance (L_s) causes inductive power loss and may lead to dc-link voltage oscillations [83]. Thus, to verify the effectiveness of the proposed voltage balancing strategy, the influence of parasitic inductance on the dc-link capacitor voltages was studied, and the results are displayed in Figs. 4.5–4.7.

Fig. 4.5 displays the simulated dc-link capacitor voltages under the conventional method (Fig. 4.5 (a)) and proposed PS-PWM method (Fig. 4.5 (b)), when the parasitic inductance $L_s = 100$ nH was introduced between the dc voltage source and the dc-link at $f_c = 5$ kHz. Notably, both methods at the start of commutation experienced the oscillations with similar peak value on the capacitor voltages because of the influence of the parasitic inductance. However, the voltage oscillations under the conventional method were eliminated after one carrier period (200μs). In contrast, the voltage oscillations under the proposed method were eliminated within one-half of the carrier period (100μs) without

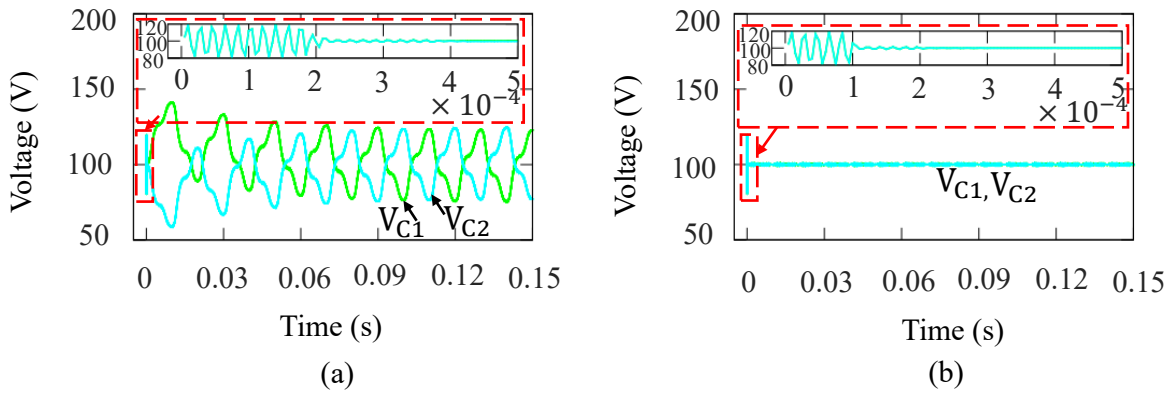


Figure 4.5: Simulated V_{C1} and V_{C2} showing the influence of parasitic inductance between V_{dc} and the dc-link, obtained by the (a) conventional method (b) proposed PS-PWM method ($C_1 = C_2 = 100$ μF, $f_c = 5$ kHz, and $L_s = 100$ nH).

causing noticeable imbalances on the capacitor voltages. It is necessary to mention that this study was conducted using PSIM, in which the switching devices are ideal. Although, in the experimental environment, the IGBT device has an output capacitance that should be considered during the parasitic inductance study.

Fig. 4.6 shows the simulated dc-link capacitor voltages under the conventional method (Fig. 4.6 (a)) and proposed PS-PWM method (Fig. 4.6 (b)), when the parasitic inductance $L_s = 100$ nH was introduced between the dc voltage source and the dc-link, and an output capacitance of 110 pF (extracted from the data sheet of the IGBT (STGW20H60DF)) was connected across the collector and emitter terminals of Q_5 and Q_6 at $f_c = 5$ kHz. Notably, after connecting the output capacitance, the capacitor voltage oscillations were considerably reduced in both methods. However, the time to eliminate the voltage oscillations was maintained to be 200 μs and 100 μs in the conventional me and proposed methods, respectively, because it depends on their ESF. This study implies that the parasitic inductance has less influence on the capacitor-voltage oscillation during the experiment because of the output capacitance of the IGBT.

Fig. 4.7 displays the simulated dc-link capacitor voltages under the conventional method (Fig. 4.7 (a)) and proposed PS-PWM method (Fig. 4.7 (b)), when the parasitic inductance $L_s = 100$ nH was introduced between the level-generation stage and H-bridge module at $f_c = 5$ kHz. Notably, both methods do not experience the voltage oscillations on the capacitor voltages because the parasitic inductance at this point does not influence the capacitor voltage. Also, when the parasitic inductance is introduced between the positive dc-link and Q_5, and between the negative dc-link and Q_6 does not influence the capacitor voltages. In both regards, the low parasitic inductance acts as the filter component in the inverter.

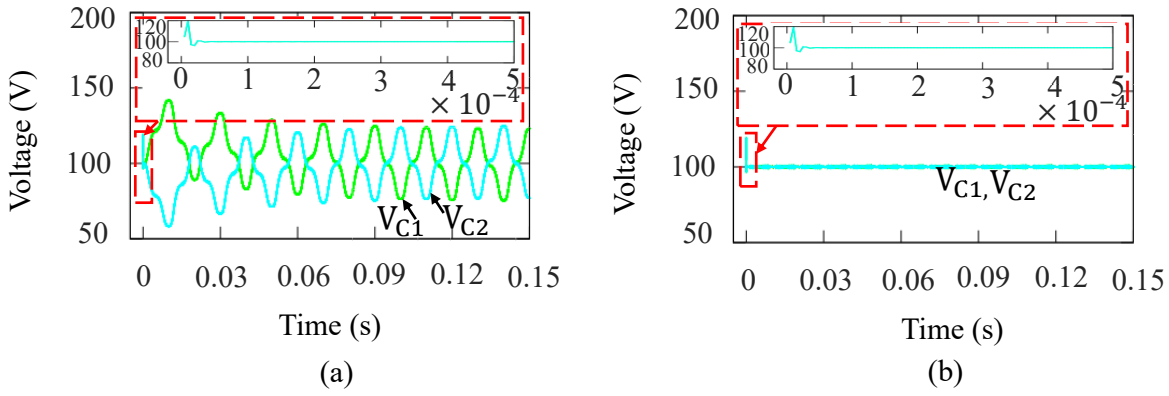


Figure 4.6: Simulated V_{C1} and V_{C2} showing the influence of parasitic inductance between V_{dc} and the dc-link when an output capacitance was connected across the collector-emitter of Q_5 and Q_6, and obtained by the (a) conventional method and (b) proposed PS-PWM method ($C_1 = C_2 = 100$ μF, $f_c = 5$ kHz, and $L_s = 100$ nH).

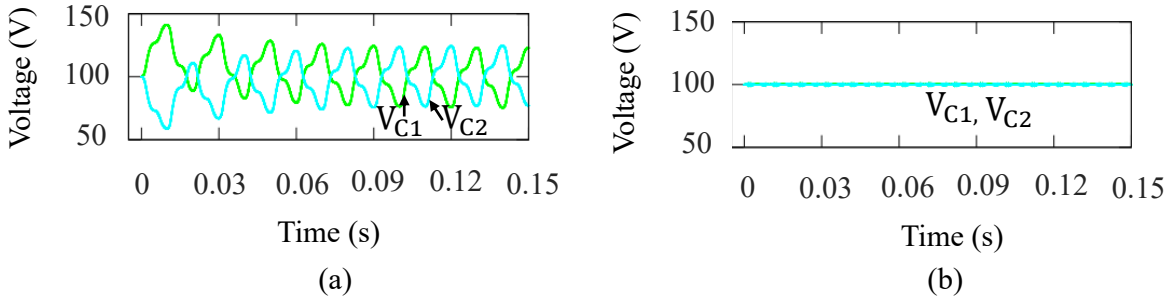


Figure 4.7: Simulated V_{C1} and V_{C2} showing the influence of parasitic inductance between the level-generation stage and H-bridge module, obtained by the (a) conventional method (b) proposed PS-PWM method ($C_1 = C_2 = 100$ μF, $f_c = 5$ kHz, and $L_s = 100$ nH).

4.4 A Comparative Study

A comparative study was conducted to demonstrate the merits and distinctions of the proposed modulation over other modulation schemes in the reference.

4.4.1 Comparison Between the Proposed and Conventional Methods

Table 4.2 compares the analyses and results of the proposed PS-PWM strategy and the conventional modulation strategy. In the proposed PS-PWM scheme, the dc-link capacitance and capacitor-voltage ripple could be regulated by adjusting the carrier frequency. This characteristic was not possible in the conventional method because the dc-link capac-

Table 4.2:
Comparison between the conventional and proposed PS-PWM methods

Parameter	Conventional method		Proposed PS-PWM method	
DC-link capacitance	$\frac{I_{om}}{2\Delta V_{Cm} f_o}$		$\frac{I_{om}}{2\Delta V_{Cm} f_c}$	
Capacitor voltage ripple	$\frac{I_{om}}{2C f_o}$		$\frac{I_{om}}{2C f_c}$	
First switching harmonic cluster frequency	f_c		$2f_c$	
Studied capacitance	1000 μF	100 μF	1000 μF	100 μF
Simulated capacitor voltage ripple	4.8 V	48 V	1.07 V	1.1 V
THD of output current	6.64%	7.44%	3.45%	3.45%
THD of output voltage	28.71%	29.23%	28.57%	28.57%
Inverter efficiency	98.58%	98.58%	98.56%	98.56%

itance and capacitor-voltage ripple depend on the fundamental frequency. The simulated voltage ripple of the dc-link capacitors was 48 V in the conventional method, but reduced to 1.1 V (0.55% of the total dc voltage) after applying the proposed method. In addition, the proposed method generates the first switching harmonic cluster of the output voltage at $2f_c$, whereas in the conventional method, the first harmonic cluster occurs at f_c. Therefore, the output filter size can be reduced in the proposed method.

The proposed method achieved a 10-fold lower dc-link capacitance than the conventional method without compromising the quality of the output voltage. It also reduced the THD of the output current. In the meantime, increasing the capacitor size beyond the designed value does not significantly improve the capacitor voltage ripple and the THD of the output current. However, the efficiency of the 5-level hybrid MLDCL inverter was reduced to 98.56% owing to high switching loss in the proposed PS-PWM method.

4.4.2 Comparison Between the Proposed Scheme and Other Capacitor Voltage Ripple Reduction Schemes

Table 4.3 qualitatively compares and shows the distinction of the proposed strategies against other capacitor-voltage ripple reduction strategies for the single-phase inverters.

Table 4.3:
Qualitative comparison between the capacitor voltage ripple reduction methods and proposed methods

Reference	Topology	Method	Comp.	ESF	P_{sw}	THD	ΔV_{cm}	Freq. of ΔV_{cm}
[39]	5L-MLDCL	LSPWM	medium	f_c	low	high	large	low freq.
[72], [73]	3L-T-type	LBPWM	low	f_c	low	-	medium	low freq.
Proposed	5L-MLDCL	PSPWM	low	$2f_c$	high	low	small	switching freq.

5L/3L = 5/3-level, Comp.= complexity, P_{sw} = switching loss, and freq. = frequency.

In this study, the complexity of the modulation method was defined based on the number of measurements and steps considered to balance the capacitor voltages. For the loss balance PWM (LBPWM) scheme in [72], [73], and the proposed strategies in the present work, the control complexity was considerably reduced because it was achieved using only comparators and logic gates without exerting high computational burden. Moreover, the proposed schemes generate the first switching harmonic cluster of the output voltage at $2f_c$, whereas in the conventional method and LBPWM method, the first harmonic cluster occurs at f_c. Thus, the output filter size was considerably reduced in the proposed strategies, as verified in Section 4.2. However, the proposed scheme is negatively impacted by high switching loss because it has higher commutations than the conventional and LBPWM methods.

On the other hand, the proposed schemes achieve a small capacitor-voltage ripple than the conventional and LBPWM strategies. In the proposed strategies, the capacitor voltage ripples depend on the switching frequency, and can be regulated by adjusting the carrier frequency. This feature was not attainable in the conventional and LBPWM schemes because the capacitor voltage ripple depends on the fundamental frequency. Thus, bulky dc-link capacitors remain necessary when the modulation methods in [39], [72], and [73] are implemented.

4.5 A Case Study of Non-Unity Power Factor Operation of the Inverter

In the next generation of the inverter applications, such as photovoltaic grid-connected systems, demand the capability of the inverter to inject reactive power to the grid in case of voltage sag caused by heavy transient phenomena such as grid fault [84]. This inverter capability is well-known as low voltage ride-through (LVRT), which demands the inverter to support voltage recovery and ensure the continuous connection of the inverter for a short period during grid fault. As mentioned earlier, the H6D2 hybrid MLDCL inverter can not operate at non-unity power factors when generating five voltage levels because it only operates in two quadrants. However, modulation techniques that can operate interchangeably between two PWM methods were proposed in the literature to improve the performance of the grid-connected inverter during LVRT [84]- [86]. The LVRT capability is achieved in the H6D2 inverter when it operates in the 3-level state [84], [86]. Moreover, when the H6D2 inverter topology generates three voltage levels, the dc-link capacitors do not charge/discharge. In this approach, the instantaneous neutral-point current is zero, thus are no ac voltage oscillations on the capacitor voltages. However, during LVRT, the THDs of output voltage and current increase due to the decrease in the output voltage levels. On the other hand, the H8 hybrid MLDCL inverter in Fig. 2.3 is capable of non-unity power factor operations and suitable for LVRT without changing the modulation technique.

In single-phase inverters, the reactive current generation and injection is performed considering the over-current protection of the inverter. Therefore, the LVRT capability of the inverter can be achieved in three common possible strategies; the constant average active power strategy, constant active current strategy, and constant peak current strategy [84]. The former two strategies pose the danger of over-current, and if proper design considerations are not achieved, the inverter shutdown may be experienced during LVRT [84], [86]. In contrast, the latter strategy has no risk of over-current problems. Thus, the study performed in this work adopted the constant peak current technique to demonstrate the effectiveness of the proposed modulation schemes.

First, the reactive power generation was verified in the H6D2 hybrid MLDCL inverter with filter by switching between two modulation methods (the proposed SC-PWM scheme and the 3-level method in [55]). In this study, the carrier frequency in the 3-level modulation method was set at 10 kHz, whereas the proposed SC-PWM method was maintained at 5 kHz. In this case both schemes have an ESF of 10 kHz. Fig. 4.8 displays the transient simulated dc-link capacitor voltages, output voltage and current of the inverter by switch-

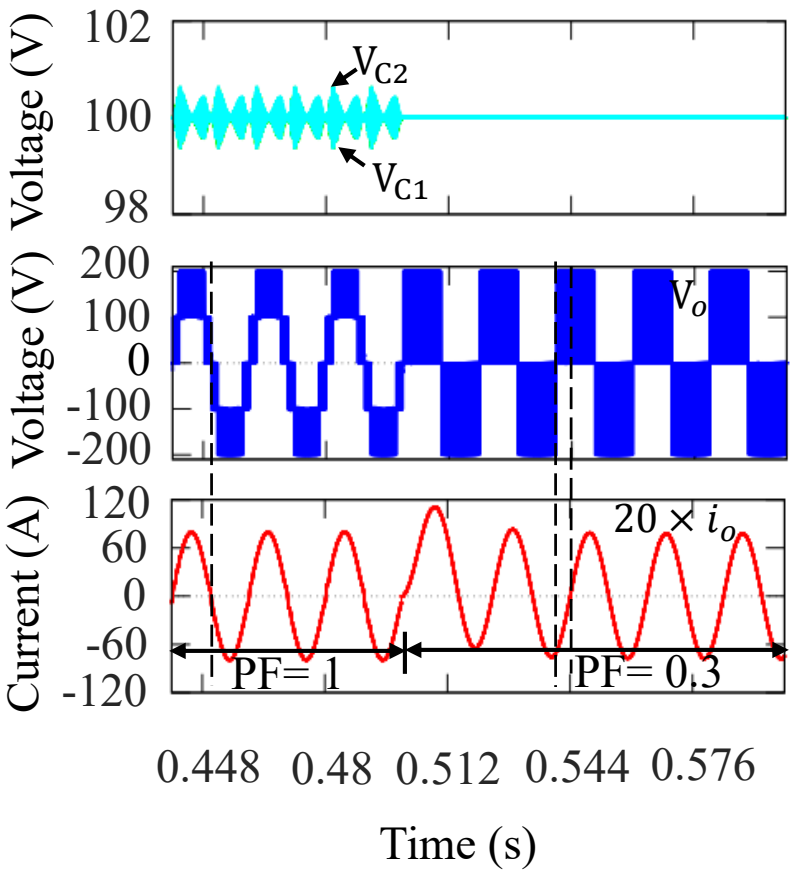


Figure 4.8: Transient simulated V_{C1}, V_{C2}, V_o, and i_o during reactive power generation (PF= 1 to PF= 0.3 lagging) in the H6D2 hybrid MLDCL inverter with filter, when constant peak current strategy was performed by switching from the proposed SC-PWM scheme to the 3-level modulation method in [55] ($C_1 = C_2 = 100$ μF).

ing from the proposed SC-PWM method to the 3-level modulation method in [55] during reactive current generation using constant peak current strategy. In this analysis the peak current was 4 A at steady-state. The reactive current generation was achieved from unity power factor to 0.3 lagging power factor. During transition at 0.5s, the output peak current increased from 4 A to 5.5 A then, the current recovered to 4 A within one fundamental cycle. Notably, during reactive current generation, the dc-link capacitor voltage ripples are considerably smaller than in the proposed SC-PWM scheme at unity power factor. The lower ripple in the capacitor voltage of the 3-level modulation method was attributed to the absence of charging/discharging of the capacitors. Thus, the designed capacitance is suitable in the event of LVRT of the H6D2 inverter by switching between the 5-level and the 3-level modulation methods when the constant peak current strategy is implemented.

Next, the steady-state and transient-state performance analyses were conducted in the

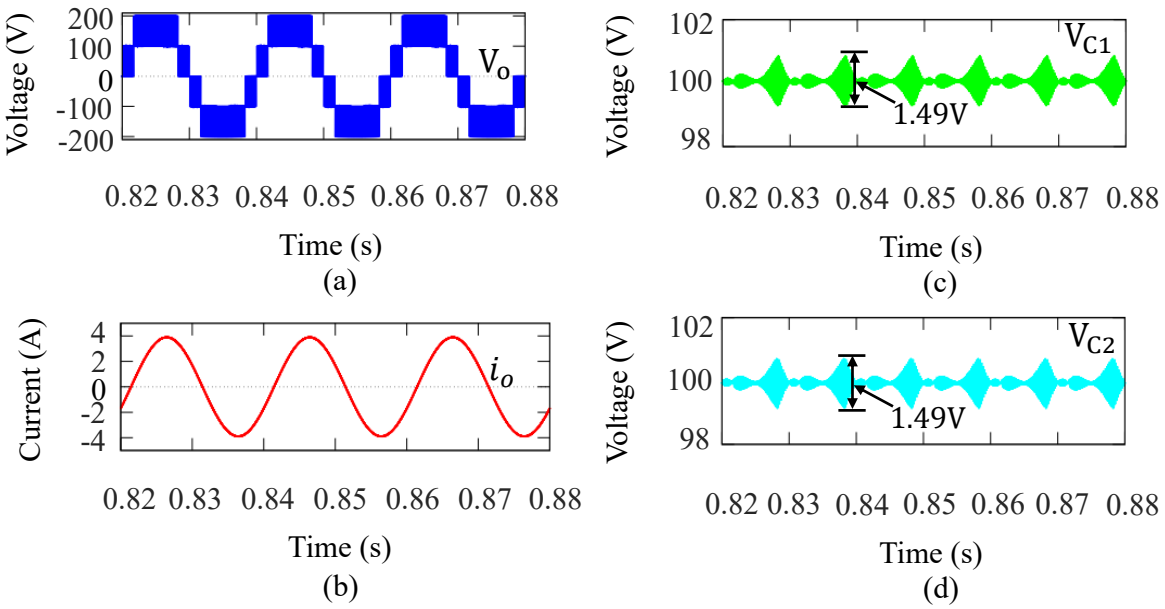


Figure 4.9: Simulated (a) V_o (b) i_o (c) V_{C1}, and (d) V_{C2} obtained the proposed SC-PWM scheme at 0.9 (45.5 Ω, 70 mH) lagging power factor ($C_1 = C_2 = 100$ μF and $f_c = 5$ kHz).

H8 topology to verify the effectiveness of the proposed modulation schemes at different non-unity power factors without changing the modulation method. To be able to operate the H8 topology, the switching signal functions for the H6D2 topology, which were developed in Section 3.5 and 3.9 can be improved as

$$S_{Q7} = \neg S_{Q5}, \tag{4.12}$$

$$S_{Q8} = \neg S_{Q6}, \tag{4.13}$$

where S_{Q7} and S_{Q8} are the switching signal functions for Q_7 and Q_8, respectively.

Figs. 4.9-4.11 display the steady-state simulated results of the proposed modulation schemes implemented on the 5-level hybrid MLDCL inverter (H8 topology) connected to an R-L load without filter and $C = 100$ μF. In this study, large inductive loads were applied to account for similar scenarios in the application.

Fig. 4.9 shows the simulated output voltage, output current, and dc-link capacitor voltages obtained at 0.9 lagging power factor when the proposed SC-PWM was applied. At 0.9 power factor, the dc-link capacitor voltage ripple was slightly increased to 1.49 V when compared to voltage ripple (1.06 V) at unity power factor. But, the proposed modulation scheme maintained the elimination of low-fundamental frequency voltage ripple.

Fig. 4.10 shows the simulated output voltage, output current, and dc-link capacitor voltages obtained at approximately zero lagging power factor when the proposed SC-PWM

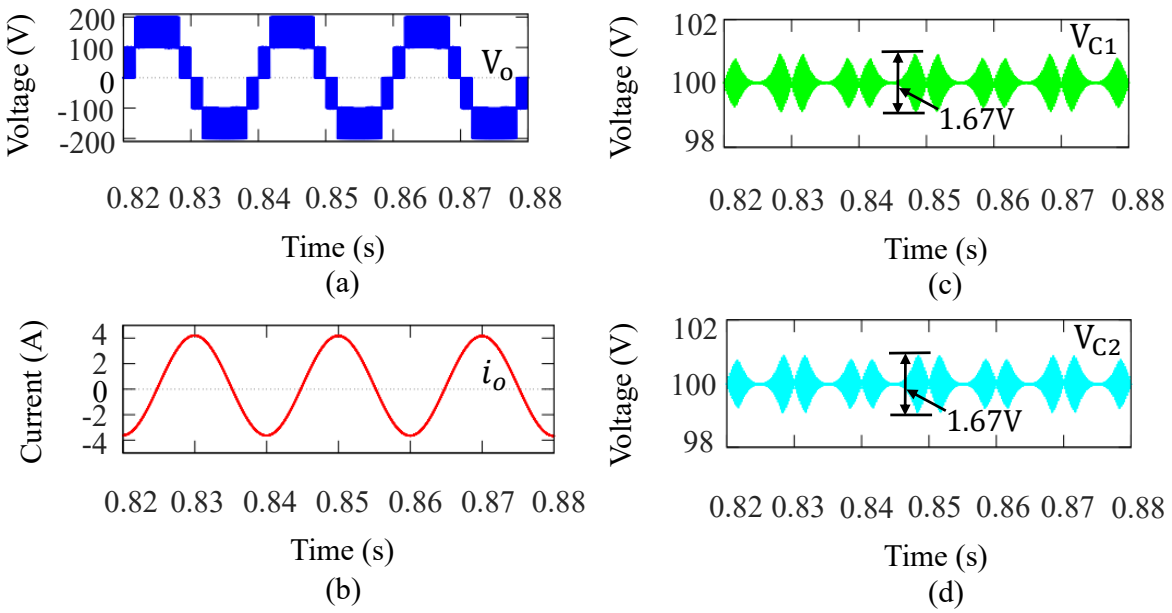


Figure 4.10: Simulated (a) V_o (b) i_o (c) V_{C1}, and (d) V_{C2} obtained the proposed SC-PWM scheme at 0 (0.5 Ω, 160 mH) lagging power factor ($C_1 = C_2 = 100$ μF and $f_c = 5$ kHz).

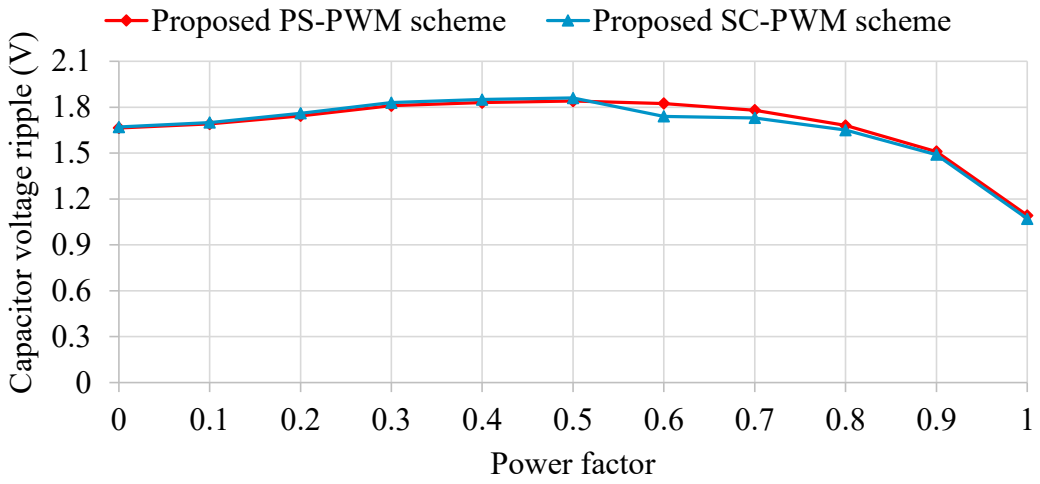


Figure 4.11: Simulated dc-link capacitor voltage ripples obtained at different power factors using the proposed PS-PWM and SC-PWM schemes ($C_1 = C_2 = 100$ μF, $f_c = 5$ kHz) and constant $I_{om} \approx 4$ A).

was applied. At zero power factor, the dc-link capacitor voltage ripple was increased to 1.67 V from 1.06 V at unity power factor. Nevertheless, the proposed modulation scheme maintained its capability to eliminate the low-fundamental frequency voltage ripple. Thus, the proposed SC-PWM schemes can be employed in applications that demands reactive current capability of the inverter without compromising the power quality.

Fig. 4.11 displays the simulated voltage ripples of the dc-link capacitors under the

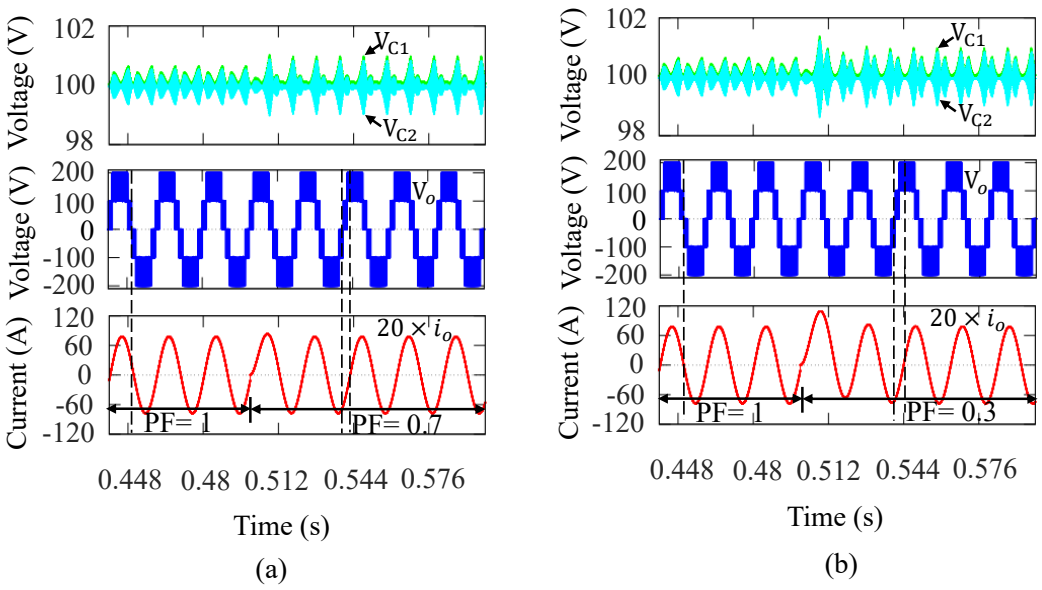


Figure 4.12: Transient simulated V_{C1}, V_{C2}, V_o, and i_o during reactive power generation (a) PF= 1 to PF= 0.7 and (b) PF= 1 to PF= 0.3, when constant peak current strategy was applied using the proposed SC-PWM scheme ($C_1 = C_2 = 100$ μF and $f_c = 5$ kHz).

proposed PS-PWM and SC-PWM methods at $f_c = 5$ kHz by varying the load power factors. The voltage ripple of the dc-link capacitors was maintained below 1.86 V in both proposed modulation schemes, with the lowest voltage ripple observed at the unity power factor and the highest at the power factor of 0.5. The proposed PS-PWM and SC-PWM methods maintain the capacitor voltage ripples, which are dominated by the switching frequency for the full range of lagging power factors.

Fig. 4.12 shows the transient simulated dc-link capacitor voltages, output voltage and current of the inverter under the proposed SC-PWM method during reactive power generation using constant peak current strategy. In this analysis the peak current was 4 A at steady-state. Fig. 4.12 (a) shows reactive power generation from unity power factor to 0.7 lagging power factor. Notably, during transition at 0.5s the peak current increased from 4 A to 4.2 A, and within one fundamental cycle, the current recovered to 4 A with the operating power factor being 0.7 lagging. Moreover, in Fig. 4.12 (b), the reactive power generation was achieved from unity power factor to 0.3 lagging power factor. During transition at 0.5s, the output peak current increased from 4 A to 5.5 A then, the current recovered to 4 A within one fundamental cycle. In both analyses, the dc-link capacitor voltages increased during reactive power generation, the highest voltage ripple observed during the transition from unity power factor to non-unity power factor. However, the capacitor voltage ripples were maintained at a small value enough not to distort the output voltage. Thus, the designed capacitance is suitable even in the event of

LVRT of the inverter when the constant peak current strategy is implemented.

4.6 Summary

In this chapter, the detailed guidelines for designing the dc-link capacitors and LC filter circuit for the single-phase 5-level hybrid MLDCL inverter under the proposed PWM strategies in comparison with the conventional method were provided. Notably, in the proposed modulation schemes, the dc-link capacitance was reduced by 90% from that of the conventional scheme. Moreover, the parameters of the LC filter were considerably reduced in the proposed scheme than in the conventional scheme.

Chapter 5

Thermal Analysis and Power Loss Estimation in a 5-Level Hybrid MLDCL Inverter

In this chapter, an extended performance analysis in terms of power losses distribution is presented. In the first part, the theoretical power loss analysis is modeled, and similar analysis is performed in simulation using PLECS software. Moreover, a comparative discussion between the proposed scheme and conventional scheme in terms of junction temperature of the switching devices and power loss is provided.

5.1 Power Loss in Switching Devices

Mainly there are two losses that occur in electronic devices. Those losses are switching and conduction which sums up to total losses that dissipate from the respective device [35]− [37]. The theoretical analysis and computation of power losses in the 5-level hybrid MLDCL inverter are performed considering the switching devices data sheet parameters, the circuit working conditions and output voltage and current. This analysis considers a modified sine wave output voltage waveform with maximum amplitude of 200 V and sinusoidal output current with peak value 4.01 A and THD of 3.45%.

5.1.1 Conduction Losses

Generally, Conduction losses in multilevel inverter occur during ON-state of the switching power device when conducting current is flowing through it. In multilevel inverter, all

semiconductor switches which are in the current flow-path at the same moment lead to such power loss [35].

The instantaneous conduction losses of the controlled-switching device (IGBT) $P_{c,IGBT}(t)$ and diode $P_{c,diode}(t)$ are given as

$$P_{c,IGBT}(t) = \left[V_{on,IGBT} + R_{on,IGBT} i^{\beta}(t)\right] i(t) \tag{5.1}$$

$$P_{c,diode}(t) = [V_{on,diode} + R_{on,diode} i(t)] i(t) \tag{5.2}$$

where $V_{on,IGBT}$ and $V_{on,diode}$ are the ON-state threshold voltages of IGBT and diode, $R_{on,IGBT}$ and $R_{on,diode}$ are the equivalent resistances of voltage drops during ON-state of IGBT and diode, respectively, β is the constant, and $i(t)$ is the instantaneous conduction current. Then, the average conduction power loss of the switching device is given as

$$P_c = \frac{1}{T} \int_0^T \left[N_{on,IGBT} \cdot P_{c,IGBT}(t) + N_{on,diode} \cdot P_{c,diode}(t)\right] d(t) \tag{5.3}$$

where T is the conduction time period, $N_{on,IGBT}$ and $N_{on,diode}$ are the numbers of IGBTs and diodes in ON-state, respectively.

Conduction Losses in H-bridge Module

During the half cycle of the fundamental period, two free-wheel diodes and two IGBTs in the H-bridge module in the MLDCL inverter conduct simultaneously. From (5.1), conduction loss per IGBT in the H-bridge module is given as

$$P_{Hc,IGBT}(t) = \left[V_{on,IGBT} + R_{on,IGBT} i_H^{\beta}(t)\right] i_H(t) \tag{5.4}$$

where $i_H(t)$ is the current flowing through the IGBT in the H-bridge module. From (5.2), conduction power loss per free-wheel diode in the H-bridge module is given as

$$P_{Hc,diode}(t) = [V_{on,diode} + R_{on,diode} i_{fH}(t)] i_{fH}(t) \tag{5.5}$$

where $i_{fH}(t)$ is the current flowing through the free-wheel diode in the H-bridge module. From (5.4), (5.5), and the operation of the MLDCL inverter, the total conduction loss in H-bridge module is obtained as

$$P_{Hc}(t) = 4(P_{Hc,IGBT}(t) + P_{Hc,diode}(t)) \tag{5.6}$$

Conduction Losses in the Level-Generation Stage

During one fundamental cycle, In mode 4 or 8, two IGBTs conduct simultaneously. While in modes 2, 3, 6, or 7, one power diode and one IGBT conduct simultaneously. From (5.1) and (5.2), the conduction loss per IGBT $P_{LG4c,IGBT}(t)$ and power diode $P_{LG4c,diode}(t)$ of the level-generation (LG) stage during mode 4 or 8 is expressed as

$$P_{LG4c,IGBT}(t) = \left[V_{on,IGBT} + R_{on,IGBT} i_{4LG}^{\beta}(t)\right] i_{4LG}(t) \tag{5.7}$$

where $i_{4LG}(t)$ is the instantaneous current flowing through the IGBT in the LG stage during mode 4 or 8. In the single-phase hybrid MLDCL inverter, no current flows through the free-wheel diodes in the LG stage. Thus, their conduction power loss is zero [75].

During modes 2, 3, 6, or 7; the conduction loss per IGBT $P_{LG2c,IGBT}(t)$ and diode $P_{LG2c,pdiode}(t)$ in the LG stage are given as

$$P_{LG2c,IGBT}(t) = \left[V_{on,IGBT} + R_{on,IGBT} i_{2LG}^{\beta}(t)\right] i_{2LG}(t) \tag{5.8}$$

$$P_{LG2c,pdiode}(t) = [V_{on,pdiode} + R_{on,pdiode} i_{2pLG}(t)] i_{2pLG}(t) \tag{5.9}$$

where $i_{2LG}(t)$ and $i_{2pLG}(t)$ are the instantaneous currents flowing through the IGBT and power diode in the level-generation stage during modes 2, 3, 6, or 7, and $V_{on,pdiode}$ is the ON-state threshold voltage of the power diode.
Then, the total conduction loss in the LG stage is expressed as

$$P_{LGc}(t) = 2\left[P_{LG4c,IGBT}(t) + P_{LG2c,IGBT}(t) + P_{LG2c,pdiode}(t)\right] \tag{5.10}$$

From (5.6) and (5.10), the total conduction power loss in the single-phase 5-level hybrid MLDCL inverter is given as

$$P_c = P_{Hc}(t) + P_{LGc}(t) \tag{5.11}$$

5.1.2 Switching Losses

The switching loss is dissipated during turn-on and turn-off of the controlled-switching devices (IGBTs), whereas the switching loss in the diode is due to the reverse recovery operation of the diode. The turn-off energy loss E_{off}, turn-on energy loss E_{on}, and reverse recovery energy loss E_{rec} can be obtained as

$$E_{off,q} = \int_0^{t_{off}} v(t)i(t)d(t) = \int_0^{t_{off}} \left[\left(\frac{v_{sw,q}}{t_{off}}t\right)\left(\frac{-I}{t_{off}}(t - t_{off})\right)\right] d(t) = \frac{1}{6} v_{sw,q} I t_{off} \tag{5.12}$$

$$E_{on,q} = \int_0^{t_{on}} v(t)i(t)d(t) = \int_0^{t_{on}} \left[\left(\frac{v_{sw,q}}{t_{on}} t \right) \left(\frac{-I'}{t_{on}} (t - t_{on}) \right) \right] d(t) = \frac{1}{6} v_{sw,q} I' t_{on} \tag{5.13}$$

$$E_{rec} = Q_{rr} V_{rr} \tag{5.14}$$

where $E_{off,q}$ and $E_{on,q}$ are the turn-off and turn-on energy losses of switch q, t_{off} and t_{on} are the turn-off and turn-on time of a switching device, I and I' are the currents through a switching device before turn-off and after turn-on, Q_{rr} and V_{rr} are the reverse recovery charge and reverse voltage of the diode, respectively, and $v_{sw,q}$ is the OFF-state voltage of the switching device q.

Then, the total switching power loss is given as

$$P_{sw} = f_c \left[\sum_{q=1}^{N_{switch}} \left(\sum_{i=1}^{N_{on,q}} E_{on,qi} + \sum_{i=1}^{N_{off,q}} E_{off,qi} \right) \right] \tag{5.15}$$

where $N_{on,q}$ and $N_{off,q}$ are the number of times switch q turn on and off, $E_{on,qi}$ and $E_{off,qi}$ are the energy loss of switch q during i^{th} turn-on and turn-off, respectively, and N_{switch} is the total number of switches.

Switching Losses in H-bridge Module

In the proposed modulation strategies, the switching devices in the H-bridge module are operated at fundamental frequency. Therefore, the switching loss in the H-bridge module is negligible and it can be neglected.

Switching Losses in the Level-Generation Stage

During one-half of the fundamental period, in mode 4 or 8, two IGBTs switch off and on once simultaneously. From (5.12) and (5.15), the switching loss during off-state in the IGBTs of the level-generation stage is expressed as

$$P_{LG4swoff} = \frac{1}{3} f_c v_{sw,LGq} I_{4LG} t_{off} \tag{5.16}$$

Also, from (5.13) and (5.15), the switching loss during on-state in the IGBTs of level-generation stage is expressed as

$$P_{LG4swon} = \frac{1}{3} f_c v_{sw,LGq} I'_{4LG} t_{on} \tag{5.17}$$

Moreover, during one-half of the fundamental period, in modes 2, 3, 6, or 7, one IGBT and one power diode switch off and on twice simultaneously. From (5.12), (5.14), and (5.15),

the switching loss during off-state of the IGBT and power diode in the level-generation stage is expressed as

$$P_{LG2swoff} = \frac{1}{3} f_c v_{sw,LGq} I_{2LG} t_{off} + 2 f_c Q_{prr} V_{rrLG} \tag{5.18}$$

From (5.13) and (5.15), the switching loss during on-state of the IGBT in the LG stage is given as

$$P_{LG5swon} = \frac{1}{3} f_c v_{sw,LGq} I'_{2LG} t_{on} \tag{5.19}$$

The total switching loss in the LG stage of the 5-level hybrid MLDCL inverter is expressed as

$$P_{LGsw} = 2[P_{LG4swoff} + P_{LG4swon} + P_{LG2swoff} + P_{LG2swon}] \tag{5.20}$$

It should be well-noted that the E_{rec} of the free-wheel diodes in the LG stage is zero because no negative current flows through them. Therefore, the total switching loss in the single-phase 5-level hybrid MLDCL inverter is expressed as

$$P_{sw} = P_{LGsw} \tag{5.21}$$

The theoretical power loss calculations were performed in [75], and it was verified that the calculated power loss values closely match the simulated power loss values when the parameters of the switching devices are equally applied in thermal analysis.

5.2 Simulation Thermal Analysis and Power Loss Estimation

As the proposed modulation strategy performs more commutations in the level-generation stage than the conventional strategy (see Fig. 3.13), it is expected to increase the power loss and the junction-temperature T_j of the devices. To understand the impacts of increasing the number of commutations, a thermal analysis and power-loss distribution analysis were performed in PLECS software. In this simulation, all IGBTs were STGW20H60DF and the power diodes were STPSC20065Y. When simulating the thermal characteristics for each switching device, the ambient temperature was assumed constant at 40°C.

Fig. 5.1 shows the junction temperatures of the switching devices in the level-generation stage. Comparing the results of the proposed method and conventional method, one notices that after applying the proposed method, the differential increase in the average junction

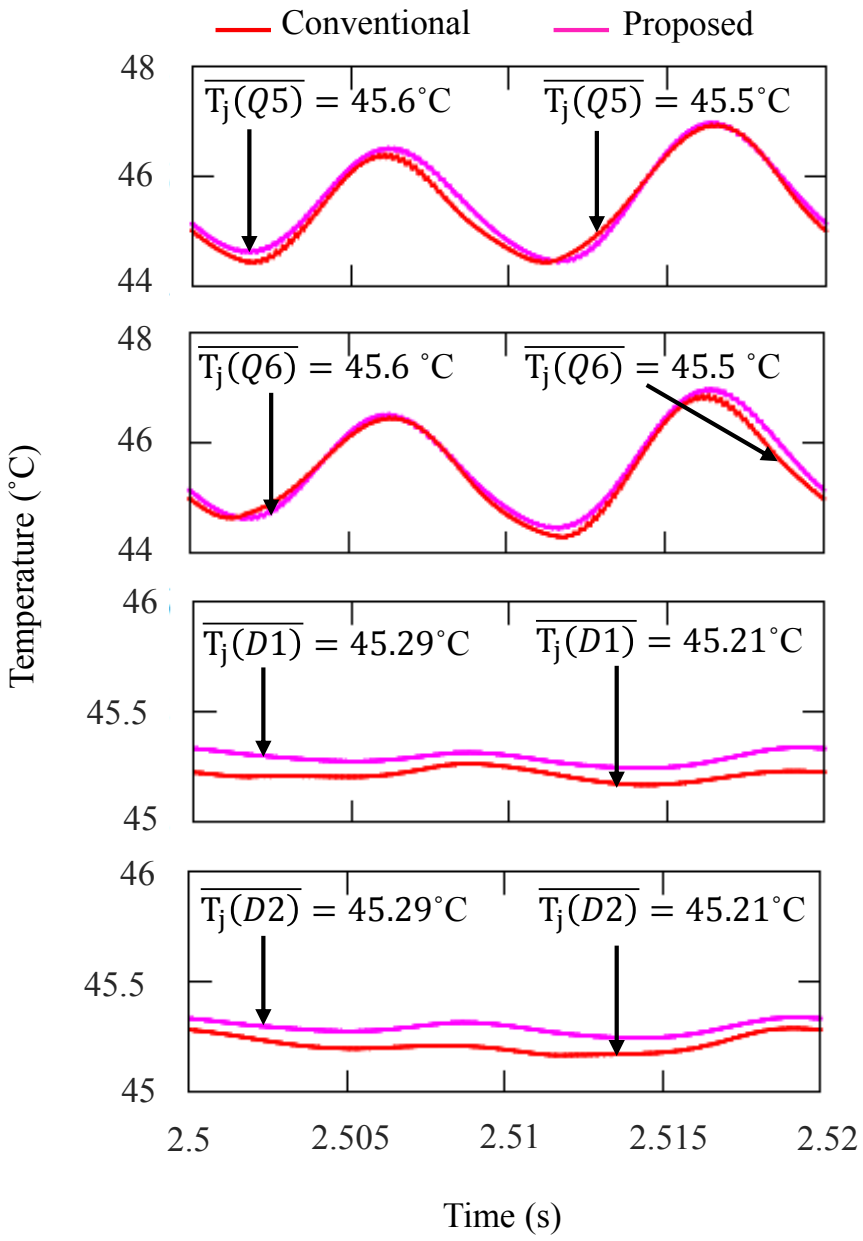


Figure 5.1: Simulated junction temperatures of the switching devices during one fundamental period ($f_c = 5$ kHz).

temperature was less than 0.1°C in each device, sufficiently negligible to preserve the effectiveness of the proposed PS-PWM method.

The main losses in electronic devices are the conduction and switching losses (P_c, and P_{sw}, respectively). These losses are summed to give the total losses P_{loss} dissipated from the inverter device [75, 87]:

$$P_{loss} = P_c + P_{sw}. \tag{5.22}$$

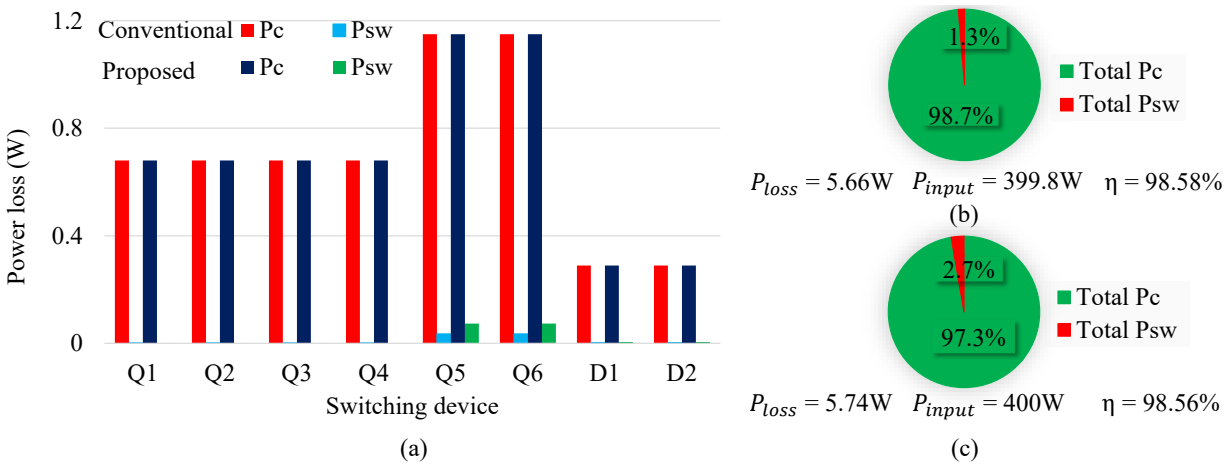


Figure 5.2: Simulated power losses at $f_c = 5$ kHz: (a) power losses of the switching devices using the conventional and proposed methods; power-loss distributions using (b) the conventional method, and (c) the proposed method.

It is important to estimate the efficiency of the single-phase 5-level hybrid MLDCL inverter under the proposed methods in comparison with the conventional method. Thus, the efficiency η of the inverter can be determined as

$$\eta = (1 - \frac{P_{loss}}{P_{input}}) \times 100.$$

Fig. 5.2(a) shows the power losses in the 5-level hybrid MLDCL inverter after implementing the conventional and proposed methods. Here, the input power (P_{input}) was 400 W. Comparing the power losses in the conventional and proposed methods (c.f. Fig. 5.2(b) and (c)), one observes that the proposed method more than doubled the switching losses. However, the contribution of the switching loss to the total power loss was negligible compared to the conduction loss. Accordingly, doubling the switching loss reduced the efficiency by only 0.02%. At an output power of 394.3 W, the conventional and proposed methods achieved an efficiency of 98.58% and 98.56%, respectively.

5.3 Summary

In this chapter, the theoretical power loss analysis in the single-phase 5-level hybrid MLDCL inverter was conducted, and similar analysis was performed in simulation using PLECS software. Moreover, a comparative discussion between the proposed scheme and conventional scheme in terms of junction temperature of the switching devices and

power loss was provided. In this study, it was observed that the proposed method more than doubled the switching losses. However, the contribution of the switching loss to the total power loss was negligible compared to the conduction loss. Accordingly, doubling the switching loss reduced the efficiency by only 0.02%.

Chapter 6

Conclusions and Future Works

6.1 Conclusions

This research dissertation proposed the simple PS-PWM and SC-PWM schemes based on redundant switching states, which controls a 5-level hybrid MLDCL inverter and balance the voltage of the dc-link capacitors during each carrier period. After implementing the proposed PS-PWM and SC-PWM schemes, the dc-link capacitance was reduced by 90% from that of the conventional method. The reduction of the dc-link capacitance not only increases the power density but also reduces the cost and physical size of the inverter. Additionally, the proposed schemes achieve over two-fold reduction in the filter circuit design that further improve the power density of the inverter. Moreover, the dc-link capacitor voltage was balanced in both steady-state and dynamic operations, demonstrating the feasibility of the proposed voltage-balancing scheme despite having lower control complexity than the conventional method. Furthermore, the voltage ripples of the dc-link capacitors were reduced by 97.7% at $f_c = 5$ kHz and can be regulated by adjusting the carrier frequency. Accordingly, the proposed methods reduce the voltage stress on the switching devices and improves the reliability of the inverter. As a further advantage of the proposed methods, the THDs of the output voltage and current of the inverter were considerably reduced from those of the conventional method. Finally, the proposed PS-PWM and SC-PWM schemes improved the dynamic performance of the 5-level hybrid MLDCL inverter, invoking a fast response to both start-up of the inverter and a sudden load change. The results of simulations were verified in experiments on a prototype.

6.2 Future Works

The following topics can be considered as the continuation of this research work.

6.2.1 Verification of the Reliability of the Inverter Using Mission Profile

From the presented analysis of the proposed modulation strategies in Chapter 3, it is shown that the reliability of the inverter was improved by reducing the capacitor voltage ripples. However, a detailed investigation of the reliability of the inverter can be performed using the mission profile, such as, the solar PV or motor operation mission profiles. In this approach, the mean-time-to-failure (MTTF) and life time of the inverter can be obtained.

6.2.2 Common-Mode Voltage (CMV) Reduction

The common-mode voltage (CMV) is an ongoing challenge in solar PV and motor applications. The CMV causes the leakage current due to stray capacitance available between solar PV arrays and in the motor windings and bearing. The leakage current can destroy the motor bearings and causes undesired power loss. The CMV problem was not considered in this thesis, but it can be included in future studies of the 5-level hybrid MLDCL inverter.

6.2.3 Replacement of the Switching Devices in the Level-Generation Stage With Wide Band Gap Devices

The use of wide band Gap switching devices, e.g., SiC, have been studied in some MLI topologies to minimize the switching loss compared to Si-based devices. In this thesis, it has been observed in Chapter 5 that the switching devices in the level-generation stage experienced high switching loss. An investigative study to replace the IGBTs in the level-generation stage with SiC devices is necessary to improve the overall efficiency of the inverter.

6.2.4 Experimental Analysis and Verification Using SC-PWM

The experimental performance verification of the 5-level hybrid MLDCL inverter when the proposed SC-PWM is applied in the H8 topology can be conducted at different power factors.

Appendix A

The Path of Double-Fundamental Frequency Component of the Input Current

The path of the double-fundamental frequency component of I_{dc} is deduced below. Applying Kirchhoff's current law at the positive dc-link of the hybrid MLDCL inverter, the current that flows out of V_{dc} is related to the current that flows through Q_5 as

$$I_{dc} = i_{dc1} - i_{C1} \tag{A1}$$

where I_{dc} is the current that flows out of V_{dc}, and i_{C1} and i_{dc1} are the currents that flow through C_1 and Q_5, respectively. From the operation of the inverter, i_{C1} is equal to $\frac{i_N}{2}$. In the proposed method, the current i_N contains only the switching frequency components, as verified in Fig. 3.21(b). Therefore, the double-fundamental frequency component of I_{dc} is equally contained in i_{dc1}. Note that the currents that flow through Q_5 and Q_6 are equal in magnitude.

Appendix B

An Example of Passive Components Cost Reduction by the Modulation Schemes

The parameters of the dc-link capacitors and LC filter, designed and estimated in Chapter 4 were used to calculate the average cost in this study. The average unit price was computed by considering the prices of components from major manufacturers of passive components, i.e., EPCOS, KEMET, Vishay, and Panasonic. In this example, the considered capacitors were metalized film capacitors, and inductors were common mode choke type. It is worth noting that the unit cost considered was for the minimum order of 10 units. The cost reduces when the minimum order of 100 units or higher is considered.

Table B.1 shows the average cost of the passive components utilized when the conventional and proposed methods were implemented in the 5-level hybrid MLDCL inverter. From Table B.1, the proposed method reduced the cost of dc-link capacitors and the total cost per unit power by more than 79% and 78%, respectively, from that of the conventional method.

Table B.1:
Comparison of the average costs of the utilized passive components between the conventional and proposed PS-PWM methods: An example

Component [Quantity]	Conventional method		Proposed method	
	Value	Unit price ($)	Value	Unit price ($)
C [2]	1000 μF	104.55	100 μF	21.60
L_f [1]	4 mH	5.55	2 mH	2.28
C_f [1]	40 μF	14.56	10 μF	3.94
Total cost ($)	229.21		49.42	
Cost per unit power ($/kW)*	573.03		123.55	

* It was calculated using the base power of 0.4 kW obtained during design.

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Related Publications

Journal Papers

- Almachius Kahwa, Hidemine Obara, and Yasutaka Fujimoto, "Minimization of dc-link capacitance and improved operational performance of a 5-level hybrid multilevel dc-link inverter," *IEEE Open J. Power Electron.*, vol. 3, pp. 182-196, Mar. 2022.

Conference Papers

- Almachius Kahwa, Hidemine Obara, and Yasutaka Fujimoto, "Analysis and implementation of a 5-level hybrid inverter with reduced switching devices using phase-shifted PWM," in *Proc. IEEE Energy Convers. Congres. Expo. (ECCE)*, Vancouver, Canada, Oct. 2021, pp. 2658-2663.

- Almachius Kahwa, Hidemine Obara, and Yasutaka Fujimoto, "Estimation and analysis of power loss in a reduced switches count H-bridge multilevel inverter," in *Proc. IEEE Intl. Conf. on Mechatron. (ICM)*, Ilmenau, Germany, Mar. 2019,pp.25-30.

- Almachius Kahwa, Hidemine Obara, and Yasutaka Fujimoto, "Design of 5-level Reduced Switches Count H-bridge Multilevel Inverter," *IEEE Intl. Workshop Advanced Motion Control (AMC)*, Tokyo, Japan, Mar. 2018.