IEICE TRANSACTIONS

on Electronics

VOL. E105-C NO. 6
JUNE 2022

A PUBLICATION OF THE ELECTRONICS SOCIETY

The Institute of Electronics, Information and Communication Engineers
Kikai-Shinko-Kaikan Bldg., 5-8, Shibakoen 3 chome, Minato-ku, TOKYO, 105-0011 JAPAN

IEICE TRANS. ELECTRON., VOL.E105–C, NO.6 JUNE 2022

PAPER Special Section on Progress & Trend of Superconductor-based Computers

A 16-Bit Parallel Prefix Carry Look-Ahead Kogge-Stone Adder Implemented in Adiabatic Quantum-Flux-Parametron Logic

Tomoyuki TANAKA[†a)], ***Student Member***, **Christopher L. AYALA**[††], ***and*** **Nobuyuki YOSHIKAWA**[††], ***Members***

SUMMARY Extremely energy-efficient logic devices are required for future low-power high-performance computing systems. Superconductor electronic technology has a number of energy-efficient logic families. Among them is the adiabatic quantum-flux-parametron (AQFP) logic family, which adiabatically switches the quantum-flux-parametron (QFP) circuit when it is excited by an AC power-clock. When compared to state-of-the-art CMOS technology, AQFP logic circuits have the advantage of relatively fast clock rates (5 GHz to 10 GHz) and 5 – 6 orders of magnitude reduction in energy before cooling overhead. We have been developing extremely energy-efficient computing processor components using the AQFP. The adder is the most basic computational unit and is important in the development of a processor. In this work, we designed and measured a 16-bit parallel prefix carry look-ahead Kogge-Stone adder (KSA). We fabricated the circuit using the AIST 10 kA/cm^2 High-speed STandard Process (HSTP). Due to a malfunction in the measurement system, we were not able to confirm the complete operation of the circuit at the low frequency of 100 kHz in liquid He, but we confirmed that the outputs that we did observe are correct for two types of tests: (1) critical tests and (2) 110 random input tests in total. The operation margin of the circuit is wide, and we did not observe any calculation errors during measurement.

key words: *superconductor logic circuit, adiabatic quantum-flux-parametron, Kogge-Stone adder, superconductor electronics, digital circuits*

1. Introduction

Most computers that support the information infrastructure in recent years are made from conventional CMOS integrated circuits. The process dimension of CMOS has reached several nanometers but it has been getting more difficult and expensive to scale further [1]. In order to develop the next generation of computing infrastructures to overcome the information processing demand of today, a new integrated circuit technology is required [2]. Based on this, we are focusing on extremely energy-efficient adiabatic quantum-flux-parametron (AQFP) logic [3], [4], and we are conducting various studies on how to systematically develop it for applications related to information technology [5]. The latest development towards this goal is a 4-bit AQFP microprocessor consisting of over 20 000 JJs [6], [7].

To continue to push the complexity of AQFP circuits, we focused on developing a 16-bit parallel prefix carry look-ahead Kogge-Stone adder (KSA) [8] in this work. The adder is one of the very basic components of a microprocessor, and it serves as a useful benchmark for evaluating and refining design strategies for new circuit technologies. In addition, this work is one of the largest superconductor-based parallel adders fabricated and demonstrated so far. This is an important milestone towards large-scale integration of AQFP circuits and towards superconductor-based computation using more practical data word sizes. In this paper, we report the design, fabrication, and demonstration of our 16-bit KSA implemented in AQFP logic.

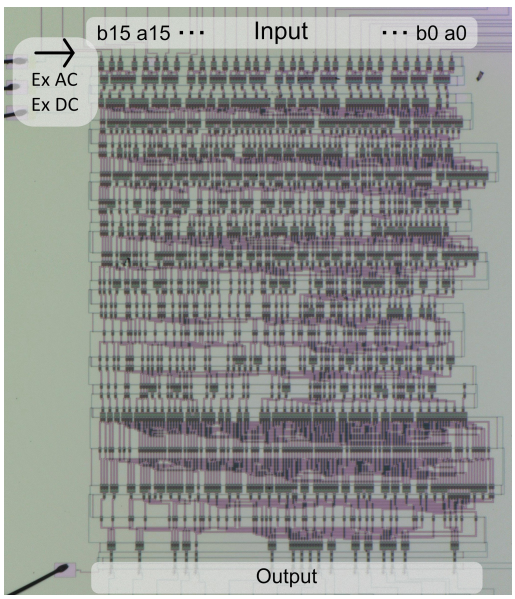


Fig. 1 Microphotograph of AQFP 16-bit KSA chip. The width and height of this circuit are 2.8 mm and 3.6 mm, respectively. Data is applied from the upper side of the circuit and the output is observed from the lower side.

2. Design of the 16-Bit KSA

The logic design of the 16-bit KSA is done by hand using an environment for AQFP semi-custom design [5]. The basic idea of the logic design is the same as the majority-based 8-bit KSA using majority-3 gates described in [9]. The 16-bit KSA block diagram is shown in Fig. 2 with each of the 16-bit inputs labeled at the top of the diagram. The area consisting of the black and gray blocks in the figure is the carry prefix tree which is the main component of the adder

Manuscript received July 30, 2021.
Manuscript revised October 20, 2021.
Manuscript publicized January 19, 2022.

[†]The author is with Department of Electrical and Computer Engineering, Yokohama National University, Yokohama-shi, 240–8501 Japan.
[††]The authors are with Institute of Advancde Sciences, Yokohama National University, Yokohama-shi, 240–8501 Japan.
a) E-mail: tanaka-tomoyuki-wy@ynu.jp

DOI: 10.1587/transele.2021SEP0001

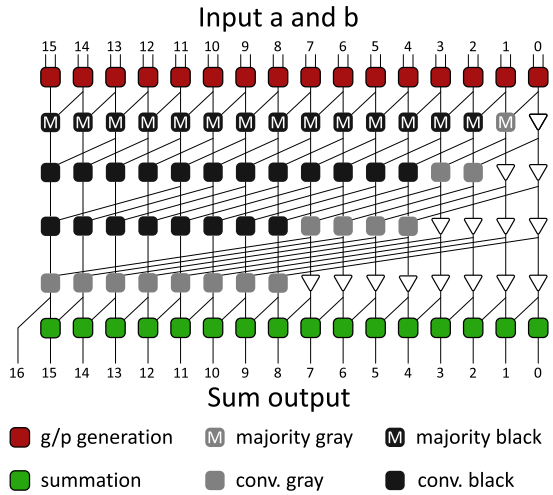


Fig. 2 Block diagram of the 16-bit AQFP Kogge-Stone adder [8], [9].

as described in [8], [9]. The depth of the logic in this region increases logarithmically, so it is faster than the ripple-carry adder.

The difference in the structure of the circuits between the previous study [9] and this study is the fabrication process and the clocking scheme. First, we switched the fabrication process from the STandard Process (STP) [10] to the High-speed STandard Process (HSTP) [11] of AIST. As a result, the critical current density was increased from 2.5 kA/cm^2 to 10 kA/cm^2 and the capacitance of the Josephson junction (JJ) has been reduced. This allowed us to remove the shunt resistor from the JJ. This change reduced the overall area of the cell by two-thirds, and it allowed us to fit more logic in a given footprint. Further by using unshunted JJs, we also reduced the switching energy of the logic cells compared to the shunted version (STP) by about an order of magnitude.

We also changed the structure of the power-clock network to excite the AQFP from 3 phases to 4 phases. The 3-phase power-clock network used three separate AC currents with a relative phase difference of 120° between them. The 4-phase network uses two AC currents (AC1 and AC2) that differ by 90° coupled to a single DC offset which enables 4 different phases to be generated from the two AC currents. Implementation using the 4-phase network becomes a little bit more complex compared to the previous 3-phase approach as we have to pay careful attention to relative directions of the AC and DC currents as they meander throughout the circuit to ensure that the appropriate clock phase is generated correctly [11]. Nonetheless, the 4-phase power-clock network allows data to propagate through 4-stages of logic per cycle instead of 3 in the prior work, and the timing windows also becomes wider thanks to the larger sampling overlap that exists between adjacent clock phases [5]. These benefits are important as we try to scale AQFP circuits to larger complexities.

With the logic netlist prepared, we then performed the automated place and route of the KSA using the genetic algorithm (GA) and channel-based routing [12], [13]. The reason for using GA was to try to solve the constraints of signal propagation in AQFP circuits by finding a quality placement of cells such that the interconnect length between adjacent logic rows do not surpass the driving length constraint. The AQFP signal line propagates the logic state using the current flowing through a superconductor ring of the AQFP. When the inductance of the superconductor ring becomes large, it attenuates the amplitude of the loop current. When the amplitude of the input data signal becomes too small such that it falls within the gray zone of the receiving AQFP, the resulting output is produced stochastically, and would result in bit errors. The exact propagation limit is currently under thorough investigation, but we assume a soft limit of approximately 0.8 mm via preliminary simulation results. In order to propagate signals over even longer distances, it is necessary to insert buffers at appropriate distances to amplify the signals once again. However, the insertion of buffers increases the area, energy and latency of the circuit. The problem is further compounded by the fact that the inserted buffers are also clocked, meaning that even if a single net between two adjacent logic rows is too long and requires a buffer insertion, all other nets between these two logic rows must also be buffered to maintain data synchronization from one phase to the next phase. The insertion of this extra row of buffers is expensive in terms of area, latency, and energy. In manual design, this insertion also introduces complications in the subsequent rows in which the designer may have already assigned clock phases to. If an extra clock phase has to be inserted in the middle of a circuit, the designer may have to redesign the clock network for the subsequent logic rows. Thus, it is important to search for a sufficient cell placement result that does not require the addition of buffers.

Since it is very difficult and time-consuming to do this work by hand, we opted to use our GA-based automatic placement tool which can insert buffers and reconcile the clock network when necessary. The most critical routing section of a conventionally placed KSA is in the final stage of the carry prefix tree where it is necessary for the interconnect to span over half of the bit slices of the adder to perform the calculation. The 16-bit KSA has roughly a horizontal distance of 1.3 mm spanning across 8 bit slices, and the actual wiring will be longer than this when considering the vertical distance. Therefore, when the adder scales to 16-bit or higher, it is necessary to insert buffers for signal amplification. This problem was not an issue in the design of the 8-bit KSA which had a worse-case horizontal interconnect distance of 0.75 mm across 4 bit slices.

To make the circuit more robust and to relax the constraints of the GA placer, we inserted an additional buffer after every logic stage to act as a driver for the next stage. This eliminated the need for the GA to handle gate-dependent driving strengths and ensured all signals from one logic stage to the next are transmitted with good amplification at the cost of doubling the latency of the entire circuit. This design guideline for the GA placer certainly impacts latency.

When compared to a handmade design which carefully considered the gate-dependent driving strengths of each cell, there is 27% reduction in latency which is the tradeoff in using automated place and route tools in this work. The microphotograph of the resulting 16-bit KSA chip is shown in Fig. 1. The circuit area of the adder is 2.8 mm × 3.6 mm, and it consists of nearly 5000 JJs.

3. Measurement Result

Using a low-frequency immersion probe, the KSA circuit was placed in liquid He and measured. Due to poor contact between the measurement system at room temperature and the custom-made terminal box connecting to the test probe, it was difficult to observe the 17 readout signals simultaneously. So a total of nine outputs were checked: bits 0 to 3, bits 12 to 15, and the carry bit. We tried two sets of tests: critical tests and random tests. The critical tests were five test vectors that we explicitly defined to demonstrate passthrough of propagate signals, generation of carry from every bit, and full-propagation along the carry chain from the least significant bit (LSB) to the most significant bit (MSB). If the carry output is correct in the latter case, it is a very a good indication that the prefix signals are properly propagating along the long interconnects between stages, and that the carry prefix tree is working properly. Table 1 lists the critical test vectors we applied and the expected result. We then proceeded to apply a set of random vectors for a total of 110 random additions, as shown in Table 2.

Figure 3 shows the results of the critical tests and 20 random tests, and Fig. 4 shows the results of 90 additional random tests at 100 kHz. The dc-SQUID-based output interface of the KSA produces a unipolar return-to-zero signal. When the output is a logic '1', the output signal rises and then falls back to zero proportional to the applied clock period of the AC clock. When the output is a logic '0', the output signal remains low. We confirmed that both the critical tests and the random tests passed. Even though our experiment was not fully exhaustive, these successful tests provide a strong indication that our design is working correctly.

Some of the outputs were rather noisy with S14 in particular being very unstable. We attribute this to the measurement equipment condition at the time of this writing. Furthermore, we measured the operating margins of the circuit by adjusting how much we can change the amplitudes of AC1 and AC2 before the circuit malfunctions. The operating range is −4.29 dBm to 0.90 dBm for AC1, and −3.41 dBm to 1.02 dBm for AC2. Both ranges are sufficiently wide.

Table 1 List of critical test vectors applied in experiment.

Op. A	Op. B	Result	Description
0xFFFF	0x0001	0x10000	Propagate carry through all bits
0x0001	0xFFFF	0x10000	Propagate carry through all bits
0xFFFF	0x0000	0x0FFFF	Operand A passthrough
0x0000	0xFFFF	0x0FFFF	Operand B passthrough
0xFFFF	0xFFFF	0x1FFFE	Generate carry at all bits

4. Comparison with Different Technologies

We compare several parallel adders under various technologies including superconductor RSFQ/ERSFQ [14], RQL [15], and 90-nm adiabatic CMOS [16]. We decided to

Table 2 Full list of random test vectors applied in experiment.

#	Op. A	Op. B	Result	#	Op. A	Op. B	Result
1	0x00E4A	0x0075B	0x015A5	56	0x06C45	0x068A6	0x0D4EB
2	0x0349A	0x0BDB1	0x0F24B	57	0x0F8A2	0x0F681	0x1EF23
3	0x03291	0x005B0	0x03841	58	0x01514	0x0502C	0x06540
4	0x0AF9C	0x0234D	0x0D2E9	59	0x0FC3D	0x0004D	0x0FC8A
5	0x0D6CC	0x07EB3	0x1557F	60	0x001D2	0x0BBBB	0x0BD8D
6	0x03EDA	0x0120A	0x050E4	61	0x0A57A	0x037FF	0x0DD79
7	0x085FA	0x0F866	0x17E60	62	0x0D00E	0x04853	0x11861
8	0x078A4	0x08059	0x0F8FD	63	0x0D35E	0x019E1	0x0ED3F
9	0x0CA13	0x03397	0x0FDAA	64	0x0D4C9	0x0CA61	0x19F2A
10	0x0E972	0x075A9	0x15F1B	65	0x084AB	0x0D785	0x15C30
11	0x06B60	0x07107	0x0DC67	66	0x0BF4A	0x070B6	0x13000
12	0x04F84	0x0C01C	0x10FA0	67	0x093DC	0x073A3	0x1077F
13	0x0A2E6	0x03A5E	0x0DD44	68	0x0113F	0x0E1FF	0x0F33E
14	0x08C19	0x019D4	0x0A5ED	69	0x02164	0x040F9	0x0625D
15	0x01B0A	0x07944	0x0944E	70	0x0040F	0x0584F	0x05C5E
16	0x0B3FC	0x0CE35	0x18231	71	0x0BDF2	0x0A60D	0x163FF
17	0x060C3	0x02B20	0x08BE3	72	0x0A42F	0x0C89B	0x16CCA
18	0x04FEC	0x04CE9	0x09CD5	73	0x07B1D	0x08CA0	0x107BD
19	0x06661	0x013C2	0x07A23	74	0x0C6D8	0x025C5	0x0EC9D
20	0x0B11F	0x0FF4A	0x1B069	75	0x020D9	0x0876A	0x0A843
21	0x0B380	0x06BFB	0x11F7B	76	0x00BCD	0x0F39F	0x0FF6C
22	0x07C9D	0x03E3B	0x0BAD8	77	0x0BADB	0x0E50B	0x19FE6
23	0x0C93A	0x0836B	0x14CA5	78	0x03CC6	0x0EE08	0x12ACE
24	0x02204	0x0A274	0x0C478	79	0x06D36	0x0312F	0x09E65
25	0x02DEC	0x03876	0x06662	80	0x02DC6	0x0C74D	0x0F513
26	0x06D5B	0x0B819	0x12574	81	0x0335F	0x00204	0x03563
27	0x0F5DB	0x025BA	0x11B95	82	0x012A9	0x076DB	0x08984
28	0x09FE5	0x0F771	0x19756	83	0x069B4	0x01A8C	0x08440
29	0x0E74F	0x0C095	0x1A7E4	84	0x08984	0x0EFEB	0x1796F
30	0x0F4A2	0x09B2B	0x18FCD	85	0x0A5DF	0x0F479	0x19A58
31	0x06230	0x0579F	0x0B9CF	86	0x04F7B	0x0795E	0x0C8D9
32	0x00974	0x00209	0x00B7D	87	0x00210	0x02F62	0x03172
33	0x0C993	0x05F24	0x128B7	88	0x03748	0x0676E	0x09EB6
34	0x0EAB9	0x0B0ED	0x19BA6	89	0x0BDD1	0x013DD	0x0D1AE
35	0x0E074	0x02F86	0x10FFA	90	0x0315A	0x07E86	0x0AFE0
36	0x082E9	0x08309	0x105F2	91	0x0114D	0x00A20	0x01B6D
37	0x063A3	0x004B5	0x06858	92	0x06D6A	0x06551	0x0D2BB
38	0x01895	0x0F683	0x10F18	93	0x02259	0x0BE0A	0x0E063
39	0x03590	0x0C2BE	0x0F84E	94	0x02862	0x02DF4	0x05656
40	0x069C9	0x06D0D	0x0D6D6	95	0x08B3E	0x0FF92	0x18AD0
41	0x0267C	0x0B06B	0x0D6E7	96	0x032AF	0x0CD67	0x10016
42	0x0C602	0x05098	0x1169A	97	0x05C8B	0x042A1	0x09F2C
43	0x0D320	0x06D40	0x14060	98	0x03A3A	0x03AD2	0x0750C
44	0x095FB	0x06603	0x0FBFE	99	0x0CE5D	0x0742A	0x14287
45	0x0513A	0x06B27	0x0BC61	100	0x06619	0x0AFEB	0x11604
46	0x0DD7A	0x0FBD7	0x1D951	101	0x0987D	0x06624	0x0FEA1
47	0x03FDC	0x0F748	0x13724	102	0x0D2C9	0x052C0	0x12589
48	0x0F5B9	0x01601	0x10BBA	103	0x0D7BB	0x00CC1	0x0E47C
49	0x03DF8	0x03EA8	0x07CA0	104	0x00D6F	0x08F55	0x09CC4
50	0x04741	0x0CA1D	0x1115E	105	0x0F4F7	0x00D7D	0x10274
51	0x06063	0x06A60	0x0CAC3	106	0x07391	0x05937	0x0CCC8
52	0x00242	0x02884	0x02AC6	107	0x00B7B	0x059C2	0x0653D
53	0x02BD4	0x0CC85	0x0F859	108	0x032EA	0x04471	0x0775B
54	0x0A4C7	0x0EB0C	0x18FD3	109	0x02DB1	0x0A351	0x0D102
55	0x04E1B	0x0C9B8	0x117D3	110	0x0F361	0x091C1	0x18522

The first 20 vectors in this list correspond to the random tests in Fig. 3, and the last 90 vectors correspond to Fig. 4.

Fig. 3 Measurement waveform of the 16-bit KSA for 5 critical test vectors shown in Table 1 and the first 20 random test vectors shown in Table 2. The signals from top to bottom are the excitation current, output bits 0 (LSB) to 3, bits 12 to 15, and the output of the carry (MSB). Critical tests include test cases in which the carry moves from the LSB to the MSB. All tests cases have been validated.

Fig. 4 Measurement waveform of the 16-bit KSA showing 90 random test vectors listed as 21 through 110 in Table 2. The signals from top to bottom are the excitation current, output bits 0 (LSB) to 3, bits 12 to 15, and the output of the carry (MSB). All observable outputs have been validated. The waveform traces have been averaged to show a clearer picture.

compare RSFQ/ERSFQ as it is the most widespread logic family in superconductor electronics. We include RQL as well even though the reported design is only 8-bit because it is an AC-biased logic just like AQFP, and it is also considered a very energy-efficient technology. Finally, we included the 90-nm adiabatic CMOS work reported in [16] because even though the designs have not been experimentally demonstrated, it is one of the more recent works using a 90-nm fabrication process to manufacture devices that operate adiabatically like AQFP. The area, number of Josephson

junctions (JJs) when applicable, bias magnitude, target operating frequency, and energy/op are compared in Table 3.

Firstly, the footprint area of the adder in this study is larger than that of the RSFQ implementation. Compared to RQL, the area of the AQFP circuit is also larger. The primary cause for this is the large output transformers of each AQFP. Section 5 briefly discusses how this can be improved. The adiabatic CMOS adder occupies even less area despite using a relatively old 90-nm CMOS technology. We expect this difference to grow when considering 7-nm FinFET technology [17].

In terms of the number of JJs, this study is almost half the number of junctions used in the RSFQ implementation. This may be due to the fact that RSFQ circuits are designed for very high-speed operation, so many JJs are inserted to adjust the delay of data propagation. Furthermore, the clock and reset paths of the wave-pipelined RSFQ adder also require active JJs, whereas the AQFP power-clock acts as both the synchronizing clock and reset. This power-clock is distributed through a meandering microstripline and thus requires no active JJs. RQL, like AQFP, distributes power through AC power-clocks along microstriplines, so it also has a low number of JJs. In our work, 3000 JJs are used for the amplification of signal currents, so there is potential to reduce the number of JJs to around the levels of RQL through more intelligent cell placement and interconnect routing.

The target operating frequency of RSFQ is higher than our AQFP implementation as we need to operate our circuit at relatively low clock rates to remain in the adiabatic regime. Despite this, the AQFP adder is still faster than adiabatic CMOS. When the operating frequency of the adiabatic CMOS adder is increased, the dynamic switching energy becomes more dominant compared to the static power consumption, making it difficult for semiconductor technology to make significant improvements in operating frequency while still operating adiabatically.

An important point to emphasize is the energy/op metric. The power consumption in this study was estimated by the product of the power consumption per JJ [18] at the target clock frequency of 5 GHz by the number of JJs in our circuit. For all superconductor circuits in Table 3, we also took into account the cooling overhead using a 1000 $W/W_{4.2K}$ coefficient [19]. Since the static power consumption of RSFQ is too high, we assumed that the bias network of the design can adopt the ERSFQ approach where bias resistors are replaced by current-feeding JJs for this metric. The power consumption P of ERSFQ is obtained from $P = I \times \Phi_0 \times F$, where I, Φ_0, and F are the bias current of the circuit, the quantum flux, and the operating frequency, respectively [20]. For adiabatic CMOS, a 16-bit KSA design was reported in [16], but its power consumption was not mentioned. Based on the dissipated energy for a 3-bit shift register reported in that work, we assumed a linear extrapolation of the energy/op of the CMOS-based adiabatic KSA in Table 3. Our AQFP adder requires five hundred times less power than the ERSFQ implementation, at least fifteen times less power than the RQL implementation, and thirty times less power than the adiabatic CMOS implementation. In the case of semiconductor technology, even 28-nm CMOS does not show substantial improvement over 90-nm technology for adiabatic circuits because the static leakage power becomes more prevalent in the adiabatic operation region as reported in [16]. Considering that our design is more energy-efficient and still operates at a practical clock rate for high-performance computing, this makes AQFP logic a good candidate for building the next generation of low-power supercomputers and data centers.

Table 3 Comparison with other 16-bit parallel adders in literature.

Metric	AQFP (this work)	RSFQ [14]	RQL[c] [15]	Adiabatic CMOS [16]
Area	10.1 mm^2	8.5 mm^2	2.8 mm^2	0.0048 mm^2
Complexity	4976 JJs	9941 JJs	815 JJs	972 Trs
Bias	AC 3.0 mA	DC 1.61 A	AC 0.9 mA	DC 1 V
Target Freq.	5 GHz	30 GHz	10 GHz	0.5 GHz
Energy/op	6.97 fJ[a]	3.13 pJ[ab]	90.2 fJ[a]	182 fJ[d]

[a] Includes 1000 $W/W_{4.2K}$ cooling efficiency.
[b] Design was originally in RSFQ but we assumed ERSFQ biasing.
[c] Note that this is an 8-bit RQL adder, not 16-bit.
[d] Extrapolated from energy per transistor of shift register in [16].

5. Scaling of the AQFP KSA

We estimate how the adder scales in terms of area and latency when we increase the data word size as shown in Fig. 5. Based on these estimates, we discuss where AQFP can use improvement and how such improvements can be carried out. For the estimation, we assumed a simple structure where the bit slices of KSAs are connected directly below each other, and we also considered the insertion of buffers for long-distance wiring. For example, in the final stage of a 128-bit KSA, the data travels a distance of 64-bit slices. In this case, at least 13 levels buffer insertions will be

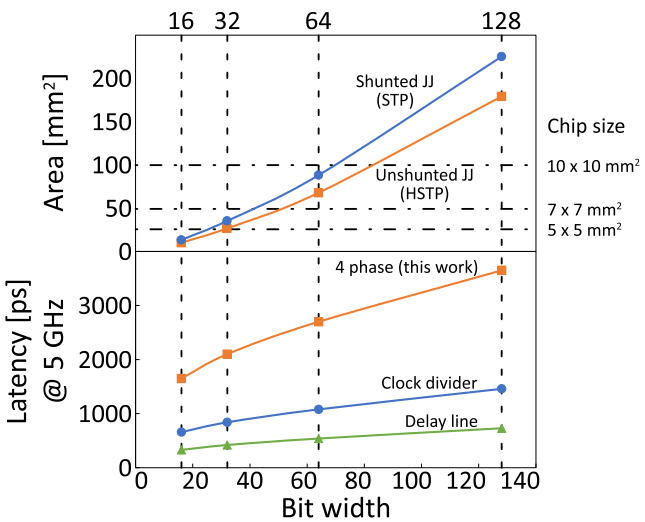


Fig. 5 Word size scaling of the AQFP KSA for area and latency.

required. To estimate the area, we calculated the ratio of the area used by the gate to the area used by the internal wiring and excitation lines for the 16-bit KSA we designed in this work, and estimated the area based on that. The number of buffer insertions increases in proportion to the square of the number of bits in the adder. Therefore, the slope of the curve with respect to area becomes a little larger. Compared to the previous study, the scalability is slightly improved because the gate area is smaller. From these estimates, it was found that, for example, a 64-bit KSA circuit can be implemented on a 1 cm × 1 cm chip. Compared to the CMOS circuits that are widely used today, this area is very large, and efforts are needed to reduce the area. One approach is using a directly coupled quantum-flux-parametron (DQFP) [21], [22] where the large output transformer is completely removed, and logic gates connect directly to each other. This can reduce the cell size in half but unlike conventional AQFP cells, the DQFP buffer and inverter have different core structures, introducing complexities in cell library development. Another approach is to use a more advanced process with more layers [23]–[25]. With more layers, the transformer and the SQUID can be stacked vertically, roughly halving the footprint of the logic cell. Interconnections of the AQFP can also be stacked, potentially reducing the area further. The DQFP approach can also benefit from more advanced processes since the directly coupled inductor structures can be implemented using dedicated kinetic inductance layers such as those in the MIT Lincoln Laboratory SFQ5ee process [26], which opens more opportunities for further scaling.

The increase in latency for KSA should be logarithmic, but according to our estimates, it is increasing a little bit faster than expected. This is due to our conservative design approach of adding buffers after each logic stage in addition to buffer insertions for long interconnects. In any case, the absolute latency is quite high. We can improve the latency by reducing the phase difference of the excitation current or, in other words, adding more clock phases within the same target clock period. This can be achieved through power clock dividers or delay line clocking [27]–[29]. The latency improvement between these techniques is shown in the lower sub-plot of Fig. 5. In the present 4-phase design, the phase difference is 90°, but by using the aforementioned methods, the phase difference can be reduced up to 1/5 of the present design. This means more clock phases become available per cycle and thus data can propagate through more stages of logic in a cycle. Furthermore, we still use the same clock frequency in these methods so the switching energy is unchanged. Lastly, the current design uses only 3-input majority gates, but by using 5-input majority gates, the latency of the prefix carry tree can be reduced by half [9], [30], [31].

6. Conclusion

We have designed and fabricated the first 16-bit AQFP adder chip. Due to a malfunction in the measurement system, we were not able to confirm the complete operation of the circuit, but it worked properly for a total of 115 validated test vectors at the low frequency of 100 kHz in liquid He. The operation range of the AC1 and AC2 excitation currents are −4.29 dBm to 0.90 dBm and −3.41 dBm to 1.02 dBm, respectively, and the circuit consists of just under 5000 JJs. We briefly discussed a few ways in which the latency and area of the circuit can be improved as we scale to larger adders. With this demonstration, we are moving closer towards functionally meaningful AQFP circuits operating on more practical data word sizes.

Acknowledgments

The present study was supported by JSPS KAKENHI (Grants No. 19H05614). CAD and EDA support was provided by the VLSI Design and Education Center (VDEC) of the University of Tokyo in collaboration with Cadence Design Systems, Inc.

The circuits were fabricated in the Clean Room for Analog-digital superconductiVITY (CRAVITY) of the National Institute of Advanced Industrial Science and Technology (AIST) using the high-speed standard process (HSTP).

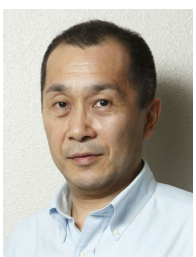
References

[1] J.C. Hurska, "As chip design costs skyrocket, 3nm process node is in jeopardy," Feb. 2019.
[2] N. Collns, "As moore's law nears its physical limits, a new generation of brain-like computers comes of age in a stanford lab," March 2017.
[3] N. Takeuchi, K. Ehara, K. Inoue, Y. Yamanashi, and N. Yoshikawa, "Margin and energy dissipation of adiabatic quantum-flux-parametron logic at finite temperature," IEEE Trans. Appl. Supercond., vol.23, no.3, pp.1700304–1700304, June 2013.
[4] K. Inoue, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Simulation and implementation of an 8-bit carry look-ahead adder using adiabatic quantum-flux-parametron," 2013 IEEE 14th International Superconductive Electronics Conference (ISEC), pp.1–3, July 2013.
[5] C.L. Ayala, R. Saito, T. Tanaka, O. Chen, N. Takeuchi, Y. He, and N. Yoshikawa, "A semi-custom design methodology and environment for implementing superconductor adiabatic quantum-flux-parametron microprocessors," Supercond. Sci. Technol., vol.33, no.5, p.054006, March 2020.
[6] C.L. Ayala, T. Tanaka, R. Saito, M. Nozoe, N. Takeuchi, and N. Yoshikawa, "Mana: A monolithic adiabatic integration architecture microprocessor using 1.4-zj/op unshunted superconductor josephson junction devices," IEEE J. Solid-State Circuits, vol.56, no.4, pp.1152–1165, April 2021.
[7] C.L. Ayala, T. Tanaka, R. Saito, M. Nozoe, N. Takeuchi, and N. Yoshikawa, "Mana: A monolithic adiabatic integration architecture microprocessor using 1.4zj/op superconductor josephson junction devices," 2020 IEEE Symposium on VLSI Circuits, pp.1–2, 2020.
[8] P.M. Kogge and H.S. Stone, "A parallel algorithm for the efficient solution of a general class of recurrence equations," IEEE Trans. Comput., vol.C-22, no.8, pp.786–793, Aug. 1973.
[9] C.L. Ayala, N. Takeuchi, Y. Yamanashi, T. Ortlepp, and N. Yoshikawa, "Majority-logic-optimized parallel prefix carry look-ahead adder families using adiabatic quantum-flux-parametron logic," IEEE Trans. Appl. Supercond., vol.27, no.4, pp.1–7, June 2017.
[10] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Adiabatic quantum-flux-parametron cell library adopting minimalist design," J. Applied Physics, vol.117, no.17, p.173912, May 2015.

[11] N. Takeuchi, S. Nagasawa, F. China, T. Ando, M. Hidaka, Y. Yamanashi, and N. Yoshikawa, "Adiabatic quantum-flux-parametron cell library designed using a 10 ka cm-2 niobium fabrication process," Supercond. Sci. Technol., vol.30, no.3, p.035002, March 2017.
[12] T. Tanaka, C.L. Ayala, Q. Xu, R. Saito, and N. Yoshikawa, "Fabrication of adiabatic quantum-flux-parametron integrated circuits using an automatic placement tool based on genetic algorithms," IEEE Trans. Appl. Supercond., vol.29, no.5, pp.1–6, Aug. 2019.
[13] Y. Murai, C.L. Ayala, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Development and demonstration of routing and placement EDA tools for large-scale adiabatic quantum-flux-parametron circuits," IEEE Trans. Appl. Supercond., vol.27, no.6, pp.1–9, Sept. 2017.
[14] M. Dorojevets, C.L. Ayala, N. Yoshikawa, and A. Fujimaki, "16-bit wave-pipelined sparse-tree RSFQ adder," IEEE Trans. Appl. Supercond., vol.23, no.3, pp.1700605–1700605, June 2013.
[15] A.Y. Herr, Q.P. Herr, O.T. Oberg, O. Naaman, J.X. Przybysz, P. Borodulin, and S.B. Shauck, "An 8-bit carry look-ahead adder with 150 ps latency and sub-microwatt power dissipation at 10 GHz," J. Appl. Phys., vol.113, no.3, p.033911, Jan. 2013.
[16] R. Celis-Cordova, A.O. Orlov, T. Lu, J.M. Kulick, and G.L. Snider, "Design of a 16-bit adiabatic microprocessor," 2019 IEEE Int. Conf. Rebooting Computing (ICRC), pp.1–4, Nov. 2019.
[17] A. Stillmaker and B. Baas, "Scaling equations for the accurate prediction of cmos device performance from 180nm to 7nm," Integration, vol.58, pp.74–81, June 2017.
[18] N. Takeuchi, T. Yamae, C.L. Ayala, H. Suzuki, and N. Yoshikawa, "An adiabatic superconductor 8-bit adder with 24kBT energy dissipation per junction," Appl. Phys. Lett., vol.114, no.4, p.042602, Jan. 2019.
[19] D.S. Holmes, A.L. Ripple, and M.A. Manheimer, "Energy-efficient superconducting computing—Power budgets and requirements," IEEE Trans. Appl. Supercond., vol.23, no.3, pp.1701610–1701610, June 2013.
[20] D.E. Kirichenko, S. Sarwana, and A.F. Kirichenko, "Zero static power dissipation biasing of RSFQ circuits," IEEE Trans. Appl. Supercond., vol.21, no.3, pp.776–779, June 2011.
[21] N. Takeuchi, K. Arai, and N. Yoshikawa, "Directly coupled adiabatic superconductor logic," Supercond. Sci. Technol., vol.33, no.6, p.065002, May 2020.
[22] R. Ishida, N. Takeuchi, T. Yamae, and N. Yoshikawa, "Design and demonstration of directly coupled quantum-flux-parametron circuits with optimized parameters," IEEE Trans. Appl. Supercond., vol.31, no.5, pp.1–5, Aug. 2021.
[23] Y. He, C.L. Ayala, N. Takeuchi, T. Yamae, Y. Hironaka, A. Sahu, V. Gupta, A. Talalaevskii, D. Gupta, and N. Yoshikawa, "A compact AQFP logic cell design using an 8-metal layer superconductor process," Supercond. Sci. Technol., vol.33, no.3, p.035010, Feb. 2020.
[24] L. Schindler, R. van Staden, C.J. Fourie, C.L. Ayala, J.A. Coetzee, T. Tanaka, R. Saito, and N. Yoshikawa, "Standard cell layout synthesis for row-based placement and routing of rsfq and aqfp logic families," 2019 IEEE International Superconductive Electronics Conference (ISEC), pp.1–5, 2019.
[25] C.J. Fourie, C.L. Ayala, L. Schindler, T. Tanaka, and N. Yoshikawa, "Design and characterization of track routing architecture for rsfq and aqfp circuits in a multilayer process," IEEE Trans. Appl. Supercond., vol.30, no.6, pp.1–9, Sept. 2020.
[26] S.K. Tolpygo, V. Bolkhovsky, T.J. Weir, A. Wynn, D.E. Oates, L.M. Johnson, and M.A. Gouker, "Advanced fabrication processes for superconducting very Large-Scale integrated circuits," IEEE Trans. Appl. Supercond., vol.26, no.3, pp.1–10, April 2016.
[27] Y. He, N. Takeuchi, and N. Yoshikawa, "Low-latency power-dividing clocking scheme for adiabatic quantum-flux-parametron logic," Appl. Phys. Lett., vol.116, no.18, p.182602, May 2020.
[28] N. Takeuchi, M. Nozoe, Y. He, and N. Yoshikawa, "Low-latency adiabatic superconductor logic using delay-line clocking," Appl. Phys. Lett., vol.115, no.7, p.072601, Aug. 2019.
[29] R. Saito, C.L. Ayala, and N. Yoshikawa, "Buffer reduction via n-phase clocking in adiabatic quantum-flux-parametron benchmark circuits," IEEE Trans. Appl. Supercond., vol.31, no.6, pp.1–8, Sept. 2021.
[30] V. Pudi and K. Sridharan, "New decomposition theorems on majority logic for low-delay adder designs in quantum dot cellular automata," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol.59, no.10, pp.678–682, Oct. 2012.
[31] V. Pudi and K. Sridharan, "Low complexity design of ripple carry and Brent-Kung adders in QCA," IEEE Trans. Nanotechnology, vol.11, no.1, pp.105–119, Jan. 2012.

Tomoyuki Tanaka received the B.E. degrees in 2018 and the M.E. degrees in 2020 from Yokohama National University. His research interests include superconductor computing devices and computer architecture. Mr. Tanaka is a student member of the Institute of Electronics, Information and Communication Engineers of Japan, Cryogenics and Superconductivity Society of Japan.

Christopher L. Ayala received the combined B.E./M.S. degree in 2009 and the Ph.D. degree in 2012 from Stony Brook University, Stony Brook, New York, USA, all in electrical and computer engineering. From 2013 to 2015, he was a Post-Doctoral Fellow with IBM Research, Zurich, Switzerland. Since 2015, he has been with the Institute of Advanced Sciences, Yokohama National University, Yokohama, Japan, where he is currently an Associate Professor. His research interests include emerging circuit technologies, superconductor logic, NEMS-MEMS, novel computer architectures, and electronic design automation (EDA). Dr. Ayala is a member of the Institute of Electrical and Electronics Engineers, the Japan Society of Applied Physics, the Institute of Electronics, Information and Communication Engineers of Japan, Eta Kappa Nu Honor Society, and the Tau Beta Pi Engineering Honor Society.



Nobuyuki Yoshikawa received the B.E., M.E., and Ph.D. degrees in electrical and computer engineering from Yokohama National University, Japan, in 1984, 1986, and 1989, respectively. Since 1989, he has been with the Department of Electrical and Computer Engineering, Yokohama National University, where he is currently a Professor. His research interests include superconductive devices and their application in digital and analog circuits. He is also interested in single-flux-quantum circuits, quantum computing devices and cryo-CMOS devices. Prof. Yoshikawa is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Japan Society of Applied Physics, the Institute of Electrical Engineering of Japan, Cryogenics and Superconductivity Society of Japan, and Institute of Electrical and Electronics Engineers.