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Systematization of a Multilevel-Topology-Based Linear Amplifier Family for Noiseless DC–AC Power Conversion

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ABSTRACT Electrical power converters use semiconductor switching devices for a larger loss reduction compared with non-switching power linear amplifiers, such as class-B amplifiers. However, it is well known that the switching operation produces harmonics and electromagnetic interference noise; consequently, passive components are usually required for the suppression of these harmful subproducts. The use of recent fast power devices such as silicon carbide and gallium nitride devices produces larger dv/dt and di/dt than Si power devices, and, as a result, the above-mentioned problem becomes more tangible. In this study, we propose the concept of a family of multilevel linear amplifiers (MLLA) in which no switching power conversion is possible. MLLAs consist of series-connected switching devices, and only one of them operates as a linear amplifier, and the loss is much less than that of the class-B amplifier. The concept of the family is very useful when a proper MLLA topology is selected for application. In this study, three types of MLLA—diode-clamped, flying-capacitor, and novel modular-cascaded linear amplifiers—with four devices connected in series were investigated, and an efficiency of $>82\%$ was demonstrated in the experiments.

INDEX TERMS dc–ac power conversion, high efficiency, linear amplifier, multilevel power converter, power electronics.

I. INTRODUCTION

A. BACKGROUND

In power conversion circuits using power semiconductor devices, it is possible to achieve highly efficient power conversion with switching operations. Output waveforms with pulse width modulation (PWM) are sometimes filtered by passive LC components, and such power conversion circuits are called class-D amplifiers. However, the switching operation inherently produces harmonics and electromagnetic interference (EMI) noise [1]–[3]. For example, these harmful sub-products sometimes cause failure of winding insulation and leak current in motor drive applications [4]–[6]. The noise issue has a significant effect on system performance, and a filter design is still important to eliminate such noise and harmonics even in the case of using multilevel converters [7], [8]. The advent of wide-bandgap (WBG) devices with fast switching characteristics has highlighted this issue. However, the disadvantage of the linear amplifier without switching operation is that the efficiency cannot be higher than that of the class-D amplifier. This disadvantage has recently been reexamined, and the efficiency has been improved by using a series connection of power devices with low on-state resistance. As a result, the feasibility of switching-less power conversion for future power electronics has improved.

B. AIM AND CONTRIBUTION OF THIS STUDY

Under this scenario, a diode-clamped linear amplifier (DCLA) was first proposed in [9], and one solution was demonstrated in terms of low EMI noise and high efficiency [9]–[11]. A flying-capacitor linear amplifier (FCLA) was proposed in [12], and a modular cascaded linear amplifier (MCLA) was proposed in [13]. This study is positioned as an expanded version of the authors' paper by adding detailed contents of the operation principles, experimental results, and discussions including future directions [13]. Our goal is to

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propose the concept of a multilevel linear amplifier (MLLA) family with DCLA, FCLA, and MCLA as one of the new power conversion technologies and to summarize the advantages and disadvantages of each circuit based on the common efficiency improvement mechanism.

The common feature of the above three technologies is that the loss is mainly caused by the linear active device and the switching operation does not occur. The conversion efficiency increases when using multiple series-connected metal–oxide–semiconductor field-effect transistors (MOSFETs) and capacitors to maintain multilevel voltages compared with conventional linear amplifiers. Because the MLLA circuits do not employ high-speed switching operations, the dielectric breakdown of windings and deterioration of the device oxide film are unlikely to occur. From this point of view, MLLAs are expected to become more reliable than switching mode multilevel converters.

There can be many kinds of MLLAs, and their use is highly dependent on the application. For proper topology selection, clarification of the differences among members of the MLLA family is important in terms of operating principles, advantages, and disadvantages. In this study, the concept of the MLLA family is proposed, and the common features and differences among the members are discussed in detail.

The typical members of this family are DCLA, FCLA, and MCLA, and this combination is similar to diode-clamped, flying-capacitor, and cascaded-bridge multilevel converters [14]–[17]. One of the fascinating features is that the loss can be theoretically reduced by increasing the series number of the power devices, with only one being linearly operated. For this achievement, the assumption is that the conduction loss of the devices can be ultimately reduced to almost zero, as discussed in Section V. It is very attractive that the series connection of power devices with low on-state resistance can provide relatively efficient dc–ac power conversion without a switching operation and generate almost no harmonics and no EMI.

In Section II, the basic operations of the three types of MLLA topologies are described, and their advantages and disadvantages are compared. Sections III and IV present the simulation results and experimental data, and the efficiency of the three topologies is measured. In Section V, the design and theoretical efficiency, and voltage balance of the capacitors in MLLAs are discussed. Section VI concludes the paper.

II. FUNDAMENTALS AND COMPARISON OF BASIC TOPOLOGIES OF THE MULTILEVEL-TOPOLOGY-BASED LINEAR AMPLIFIER FAMILY

The operation principles of the basic topologies of the MLLA family to reduce the loss generated in the linear operation of power devices are similar. As described above, the DCLA and FCLA were first reported in [9] in 2008 and in [12] in 2017 by the authors, respectively. The MCLA was first proposed in [13] also by the authors, and these three basic topologies are summarized as the MLLA family in this study.

The topologies shown in Fig. 1 are the 4-series circuit configurations ($n = 4$) of each topology. Table 1 lists the comparison of the component count, complexity, advantages, and drawbacks for each topology. The cost factor can also be evaluated based on these features, including the number and losses of the power devices and capacitors listed in Table 1 [18]. Here, the number of series-connected MOSFETs per arm, n, is defined in the MLLA as a similar extendibility to the number of output levels in the multilevel power converters.

In this study, the concept of a series of linear amplifiers based on the circuit topologies of multilevel converters is proposed as a novel type of power conversion circuit. Furthermore, other topologies of the MLLA family with a similar operation principle can be proposed by extending

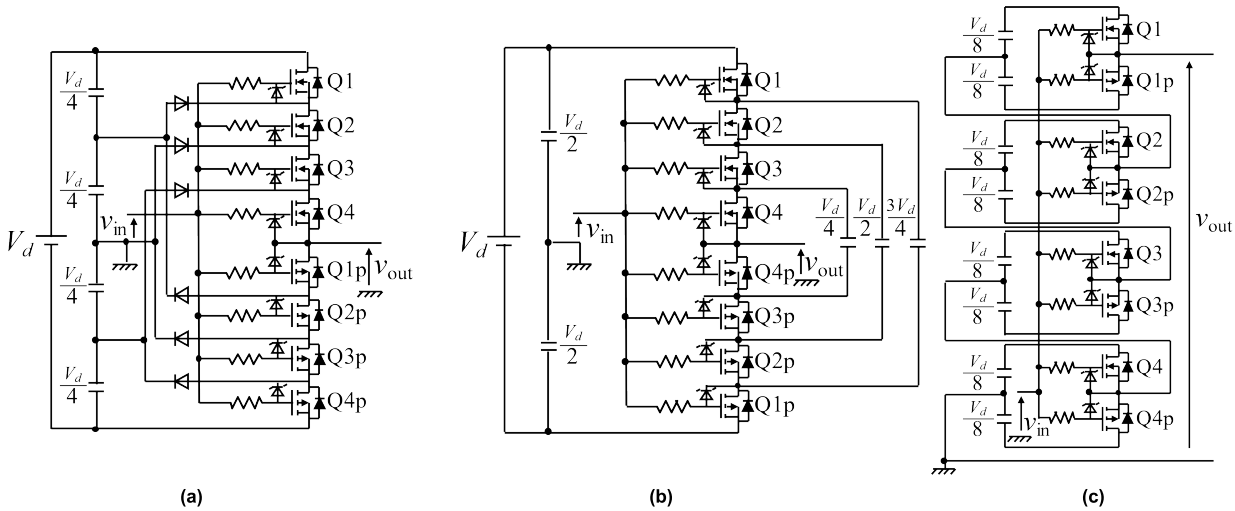

FIGURE 1. Three basic MLLA topologies (for the case of $n = 4$). (a) Diode-clamped linear amplifier (DCLA). (b) Flying-capacitor linear amplifier (FCLA). (c) Modular-cascaded linear amplifier (MCLA).

TABLE 1. Comparison of the three basic topologies of MLLA.

Topology	Diode-Clamped Linear Amplifier (DCLA) proposed in [9]	Flying-Capacitor Linear Amplifier (FCLA) proposed in [12]	Modular-Cascaded Linear Amplifier (MCLA) proposed in [13]
Number of n-channel MOSFETs	n	n	n
Number of p-channel MOSFETs	n	n	n
Number of clamp diodes	$2(n-1)$	0	0
Number of capacitors for multilevel voltages	n (shared with dc-link capacitors)	$(n-1)+2$	$2n$
Advantage	• Lower voltage rating of each dc capacitor	• Smaller capacitance of flying-capacitors • Modularized topology	• Easy to extend the series connection • Modularized topology
Drawback	• Capacitor voltage unbalance • Diode loss	• Higher voltage rating of flying-capacitors close to dc side • Capacitor loss	Large number of isolated dc power supplies for each bridge
For capacitor voltage balance	Additional circuits are required [10].	Self-voltage balancing control can be realized by individual linear gate circuit through load current.	Voltage balancing control for each cell is expected to realize by individual linear gate circuits through a circulating current.

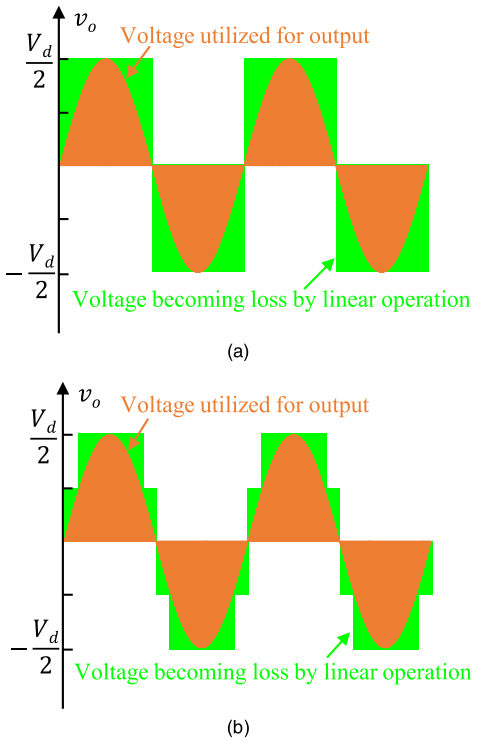

FIGURE 2. Intuitive representations of loss reduction principle in the MLLA family for (a) general class-B amplifiers and (b) 4-series MLLA.

the concept, because many types of multilevel converter topologies have been reported to date [18]–[23]. This means that the other conventional multilevel converter topologies can also be extended as linear amplifiers by modifying the gate circuit configuration. The three basic topologies with essential features can be the origin of all the other MLLA topologies.

A. DIODE-CLAMPED LINEAR AMPLIFIER (DCLA)

The circuit configuration of a 4-series DCLA in each phase is shown in Fig. 1 (a). The DCLA consists of n n-channel MOSFETs, n p-channel MOSFETs, and $2(n-1)$ diodes. In addition, n dc voltage-dividing capacitors including $(n-1)$ floating capacitors are required to maintain multilevel voltages inside the circuit, because the voltage stress of each MOSFET becomes lower by utilizing a combination of the capacitor voltages during the active state operation, as shown in Fig. 2. This operation requires multiple dc voltages in the circuit, such as provided by multilevel power converters [15].

TABLE 2. Operation states in 4-series DCLA with common gate input.

v_{out}	Q_1	Q_2	Q_3	Q_4	Q_{1p}	Q_{2p}	Q_{3p}	Q_{4p}
$E/4 < v_{out} < E/2$	act.	on	on	on	off	off	off	off
$0 < v_{out} < E/4$	off	act.	on	on	fwd	off	off	off
$-E/4 < v_{out} < 0$	off	off	off	fwd	on	on	act.	off
$-E/2 < v_{out} < -E/4$	off	off	off	off	on	on	on	act.

Note: act. = active state; fwd = on state of FWD

TABLE 3. Operation states in 4-series FCLA with common gate input.

v_{out}	Q_1	Q_2	Q_3	Q_4	Q_{1p}	Q_{2p}	Q_{3p}	Q_{4p}
$E/4 < v_{out} < E/2$	act.	on	on	on	off	off	off	off
$0 < v_{out} < E/4$	off	act.	on	on	fwd	off	off	off
$-E/4 < v_{out} < 0$	fwd	off	off	off	off	act.	on	on
$-E/2 < v_{out} < -E/4$	off	off	off	off	act.	on	on	on

Note: act. = active state; fwd = on state of FWD

TABLE 4. Operation states in 4-series MCLA with common gate input.

v_{out}	Q_1	Q_2	Q_3	Q_4	Q_{1p}	Q_{2p}	Q_{3p}	Q_{4p}
$3E/8 < v_{out} < E/2$	act.	on	on	on	off	off	off	off
$E/4 < v_{out} < 3E/8$	on	act.	on	on	off	off	off	off
$E/8 < v_{out} < E/4$	on	on	act.	on	off	off	off	off
$0 < v_{out} < E/8$	on	on	on	act.	off	off	off	off
$-E/8 < v_{out} < 0$	off	off	off	off	on	on	on	act.
$-E/4 < v_{out} < -E/8$	off	off	off	off	on	on	act.	on
$-3E/8 < v_{out} < -E/4$	off	off	off	off	on	act.	on	on
$-E/2 < v_{out} < -3E/8$	off	off	off	off	act.	on	on	on

Note: act. = active state; fwd = on state of FWD

All the operation states in the 4-series DCLA with a pure resistive load are listed in Table 2. It is confirmed that only one MOSFET always operates in the active state at the same time. The voltage rating of the dc capacitors can be lowered as the number of series connections increases, which is a major advantage of this topology. However, a comparatively large capacitance is required because they suppress the low-frequency ripple current. Furthermore, the voltages of the voltage-dividing capacitors should be maintained at each prescribed value during the circuit operation. In the case of the diode-clamped multilevel converter, auxiliary circuits are required to maintain the voltage balance of the dc capacitors [24]–[26]. Similarly, the DCLA also requires a voltage-balancing circuit. This is the main drawback of the DCLA, as described in Table 1.

B. FLYING-CAPACITOR LINEAR AMPLIFIER (FCLA)

The circuit configuration of the 4-series FCLA in each phase is shown in Fig. 1 (b). FCLA consists of $(n-1)$ flying capacitors to realize multiple voltages in the circuit instead of the diodes and voltage-dividing capacitors in the circuit of the DCLA. Unlike the DCLA, circuit of the FCLA has modularized and ladder connections without a cross-line in the entire circuit, including n n-channel and n p-channel MOSFETs. In general, the stray inductance does not need to be considered in the design of the linear amplifier because there is no pulsed waveform of voltage or current. Although the stray inductance tends to be larger in such modularized and ladder configurations, the linear amplifier is usually not affected by EMI from such stray inductance because of the no-switching operation, unlike the PWM power conversion circuits. All operation states in the 4-series FCLA with a pure resistive load are listed in Table 3.

Although the balance of capacitor voltages cannot be achieved in the circuit configuration with the common gate circuits shown in Fig. 1 (b), individual gate circuits for each MOSFET instead of the common gate circuit enable the realization of voltage balancing control [27], [28]. This indicates that the voltage balance can be achieved using the same method as in the flying-capacitor multilevel PWM converters [29], [30]. However, the volume of the capacitors tends to become larger than that in the flying-capacitor PWM converters, because the frequency of the charge and discharge in the capacitors is expected to be lower than the PWM switching frequency, as described in Table 1.

C. MODULAR-CASCADED LINEAR AMPLIFIER (MCLA)

The circuit configuration of the 4-series MCLA in each phase is shown in Fig. 1 (c). This circuit configuration is based on a modular multilevel cascaded converter (MMC) or cascaded H-bridge converter [31]–[33] and was first proposed in [13]. This circuit is configured using multiple cascaded connections of conventional class-B amplifiers. Hence, the design procedure and implementation of the MCLA are advantageous compared with those of the other topologies. This facilitates the extension of the number of series connections and offers lower cost, particularly in high-voltage applications such as those using MMCs. Furthermore, some advanced circuit configurations, such as H-bridge, multiphase, and bidirectional converters, can be assumed for various specifications [23], [33]. However, numerous isolated dc power supplies are required in a common gate circuit configuration. All the operation states in the 4-series MCLA with a pure resistive load are listed in Table 4. The MCLA has subdivided operation modes compared with the other two topologies, and this contributes to the uniformity of the loss generated in each MOSFET.

Voltage-balancing control for each cell is expected to be realized in a similar way to the MMC utilizing the circulating current by using the individual gate circuits for each MOSFET, as listed in Table 1 [34], [35]. In either case, the dc capacitors need a large capacitance to suppress the low-frequency ripple, similar to the MMC.

D. OTHER TOPOLOGIES

The other multilevel converter topologies, such as active neutral point clamped (ANPC), T-type, stacked multi-cell (SMC) converters and the other combined topologies [18], [21]–[23] can also be extended to linear amplifiers by modifying the gate circuit configuration, such as with the above three basic topologies. This is because the basic principles of all multilevel converters are common. They have multiple capacitors to maintain multilevel voltages in the circuit and power devices to change the operation states. When the power devices operate in the non-switching but linear region, the output voltage can be controlled in a linear waveform without a pulsed waveform. The characteristics of each amplifier based on multilevel converters are linked to those of each topology of the multilevel converters.

III. SIMULATION AND THEORETICAL INVESTIGATION

A. OPERATING WAVEFORMS OF THE THREE TOPOLOGIES

The simulation waveforms of the three topologies are shown in Figs. 3–6. In this simulation, the circuit simulator PSIM was used. Here, the total input dc source voltage V_d was 200 V, and the pure resistive load was 47 Ω. As shown in these waveforms, all three MLLA topologies operate as a current amplifier. This indicates that the output voltage follows the input voltage if there is no nonideal condition, and the output current is amplified. The voltage v_{QX} indicates the drain–source voltage of switch Q_X of each 4-series topology in Figs. 4–6. It is observed that each drain–source voltage becomes <50 V, which is one-fourth of the input dc voltage V_d. This indicates that the applied voltage of each MOSFET during the linear operation decreases as the number of series MOSFETs, n, increases.

It is observed that the waveforms of the three topologies are slightly different from each other. Even in a MOSFET at the same instant in the output voltage waveform, the operating states of the active, on, and off states are different in each

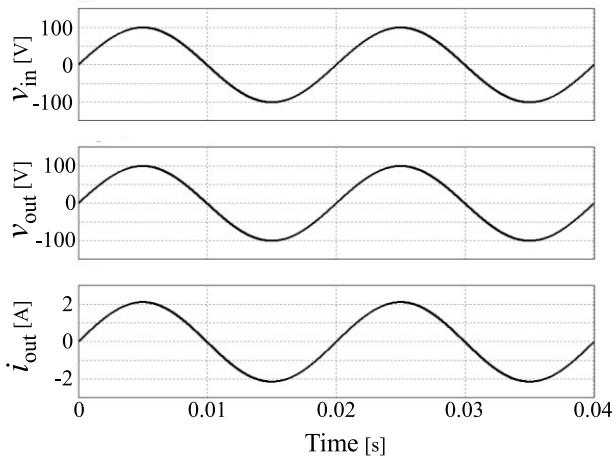

FIGURE 3. Input and output voltages, and output current in the three basic topologies of DCLA, FCLA, and MCLA.

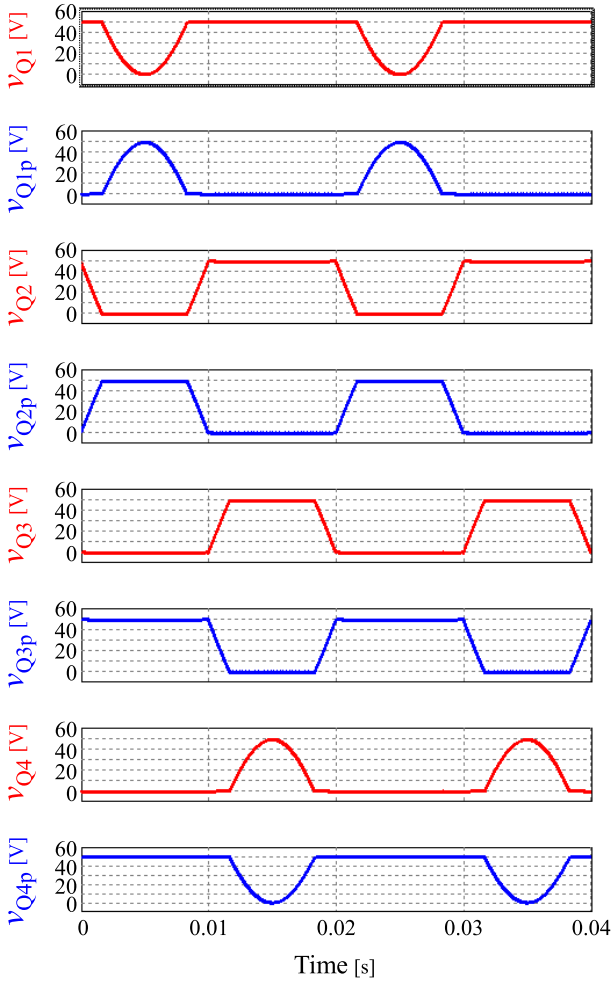

FIGURE 4. Drain–source voltages of MOSFETs Q1–Q4p in the DCLA.

topology. Each operating principle depends on the circuit connection of multiple voltage sources, including capacitors, MOSFETs, diodes, and gate circuit configuration. The basis of the loss reduction in the linear operation shown in Fig. 2

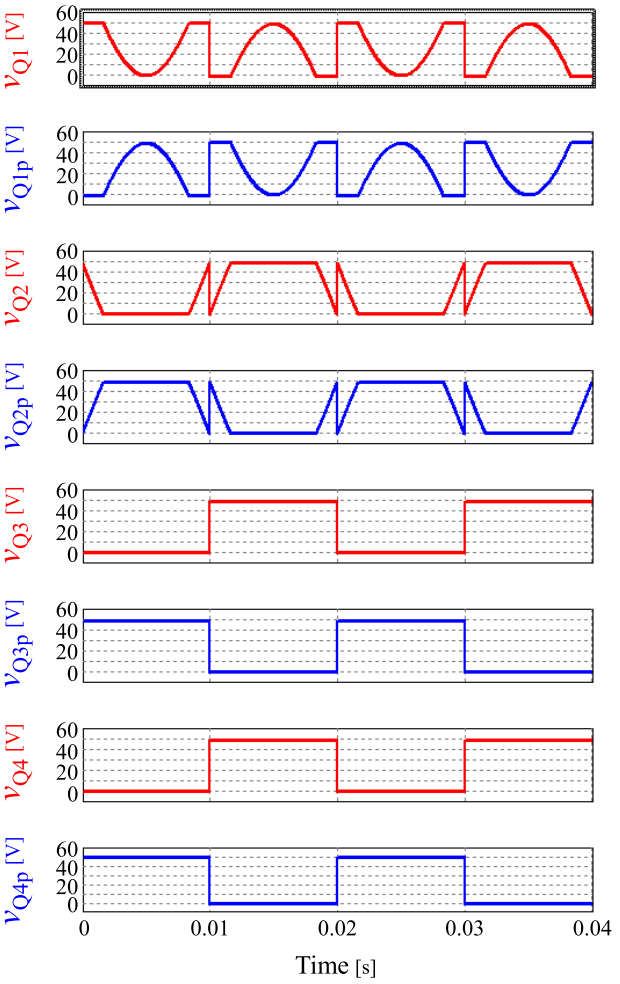

FIGURE 5. Drain–source voltages of MOSFETs Q1–Q4p in the FCLA.

is the same for the three topologies. All three topologies can reduce the applied voltage of the MOSFETs and loss during active state operation.

B. THEORETICAL CONVERSION EFFICIENCY

When the output voltage v_{out} and current i_{out} are given by

$$v_{out} = \frac{V_d}{2} \sin\theta \tag{1}$$

$$i_{out} = I_{rate} \sin\theta \tag{2}$$

respectively, the theoretical formula for the ideal efficiency in the three basic topologies can be derived using the same equation, because the principle of loss reduction of the active state MOSFET is the same as discussed above [9], [12], [27]. Note that the loss generated in each MOSFET is not uniform in the configuration of the common gate circuit. The ideal efficiency of the MLLA family considering only the loss generated in the active state of the MOSFETs can be derived as

$$\eta = \frac{n^2\pi}{16\sum_{k=1}^{n/2}\sqrt{nk-k^2}} \tag{3}$$

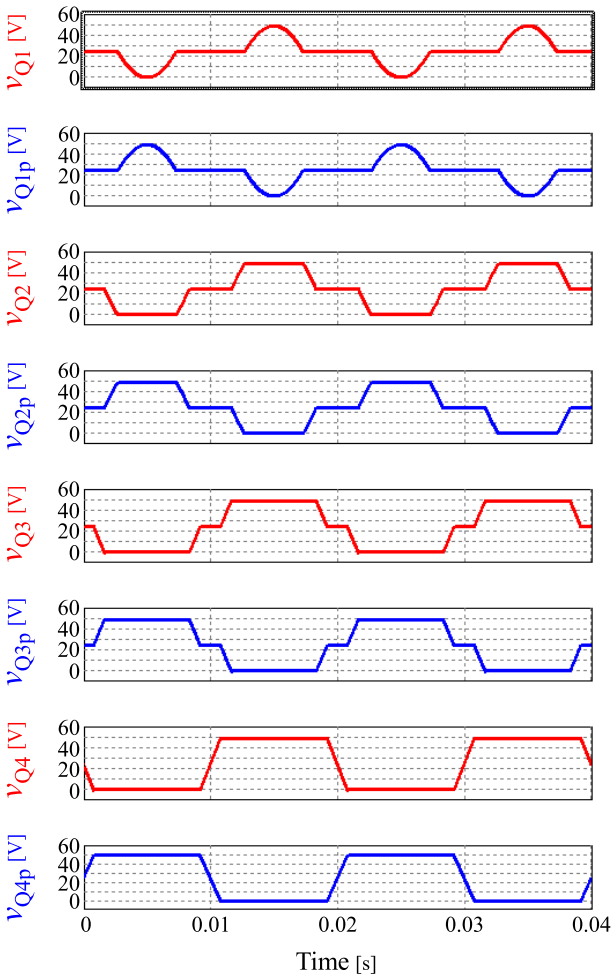

FIGURE 6. Drain–source voltages of MOSFETs Q1–Q4p in the MCLA.

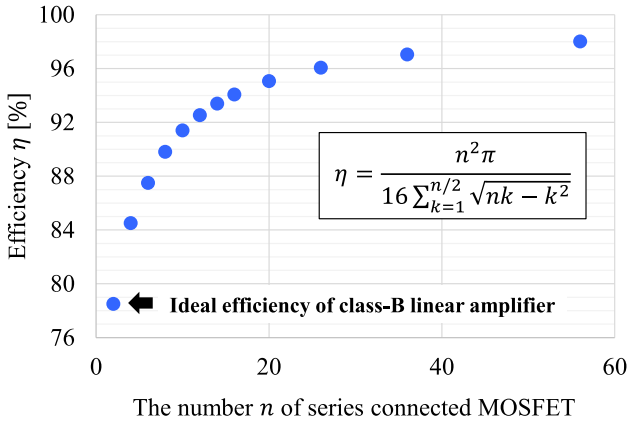

FIGURE 7. Ideal efficiency of the three basic MLLA topologies.

The loss caused by the linear operation does not depend on the load current. Therefore, the theoretical efficiency of the MLLA does not depend on the output power. The ideal efficiency expressed in (3) can be plotted for n, as shown in Fig. 7. It is observed that the efficiency of the MLLA can be improved by increasing the number of series MOSFETs. However, the increase in efficiency gradually saturates as the number n of the series devices increases. When the number of power devices increases to 36, an efficiency of >97% is achievable even in the linear amplifier without noise and harmonics. Therefore, the MLLA is expected to achieve the same level of efficiency as general PWM dc-ac power converters, despite the linear amplifier not having a switching operation. In other words, the linear amplifier of the MLLA family can be used as a noiseless power conversion circuit. In a practical design, other losses such as conduction loss, diode loss, and capacitor loss should also be considered, although these influences are relatively smaller than the linear operation loss, as discussed in Section V.

IV. EXPERIMENT

A. PROTOTYPE CIRCUITS AND CONDITIONS

The overviews of the developed prototype circuits of the 4-series DCLA, FCLA, and MCLA are shown in Figs. 8 (a), (b), and (c), respectively. The FCLA circuit can be realized by replacing the diodes in the DCLA with flying-capacitors, as shown in the circuit configurations in Figs. 1 (a) and (b). In these prototypes, the printed circuit boards of the DCLA and FCLA were the same as there is similarity between these circuit configurations. For the MCLA, unit modules of the class-B amplifier were developed, and the number of series MOSFETs, n, can be flexibly changed by combining multiple unit modules. In Fig. 8 (c), four-unit modules are connected in series to realize the 4-series MCLA, as shown in Fig. 1 (c).

Table 5 lists the electrical characteristics of the MOSFETs and the specification of the components in the gate circuit on the prototype circuits. The experimental condition was the same as that of the simulations mentioned in Section III and shown in Figs. 3–6. The total input dc voltage V_d was 200 V, and the input voltage signal was a sinusoidal waveform with an amplitude of 100 V and a frequency of 50 Hz. The load conditions were pure resistive (47 Ω) and inductive–resistive (37.5 Ω and 80 mH). In these feasibility experiments, isolated dc power supplies for the multiple voltages in each circuit were used, because none of the topologies with a common gate circuit can achieve voltage balance.

B. EXPERIMENTAL WAVEFORMS

The experimental waveforms of the input voltage v_{in}, output voltage v_{out}, output current i_{out}, and drain–source voltage waveforms of the MOSFETs in the DCLA, FCLA, and MCLA prototypes when the load condition was purely resistive are shown in Figs. 9, 10, and 11, respectively. It can be observed that the output voltage follows the input voltage signal adequately in Figs. 9 (a), 10 (a), and 11 (a). These figures confirm that the three MLLA circuits operate as a current amplifier with the same input and output voltages, as discussed above. Although a slight distortion is observed in the output voltage when the polarity of the

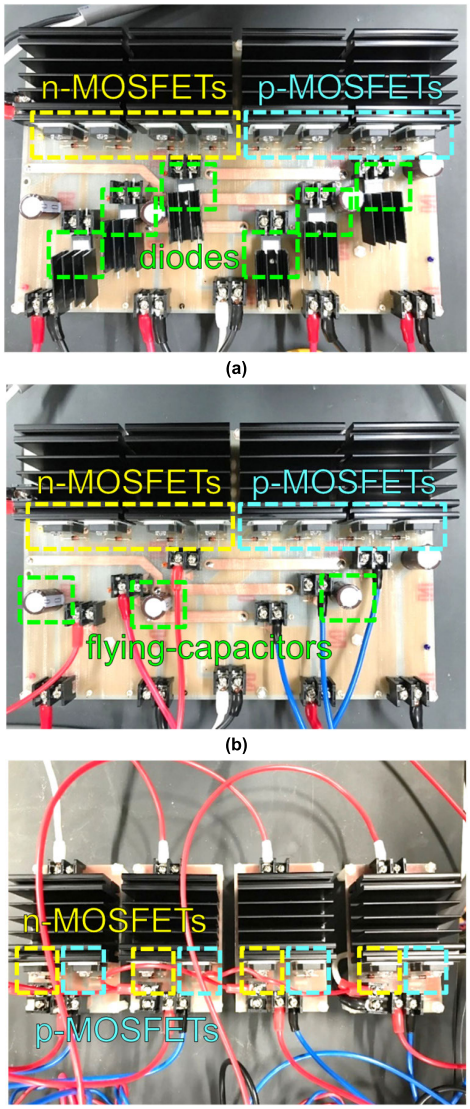

FIGURE 8. Overview of prototype circuits. (a) 4-series DCLA. (b) 4-series FCLA. (c) 4-series MCLA.

TABLE 5. Characteristics of MOSFETs and gate circuit.

Parameter	Symbol	FQA28N15 (n-channel)	FQA36P15 (p-channel)
Drain to source maximum voltage	V_{DS}	150 V	−150 V
Rated current of MOSFETs	I_D	33 A	−36 A
On-state resistance	R_{on}	0.067 Ω	0.076 Ω
Gate to source threshold voltage	V_{th}	2.0–4.0 V	−2.0–−4.0 V
Input capacitance	C_{in}	1250 pF	2550 pF
Gate resistance	R_{gate}	25 kΩ	11.8 kΩ
Zener voltage of zener diode	V_{zener}	15 V	15 V

output current was changed, this phenomenon is the same as the well-known cross-over distortion caused by the threshold

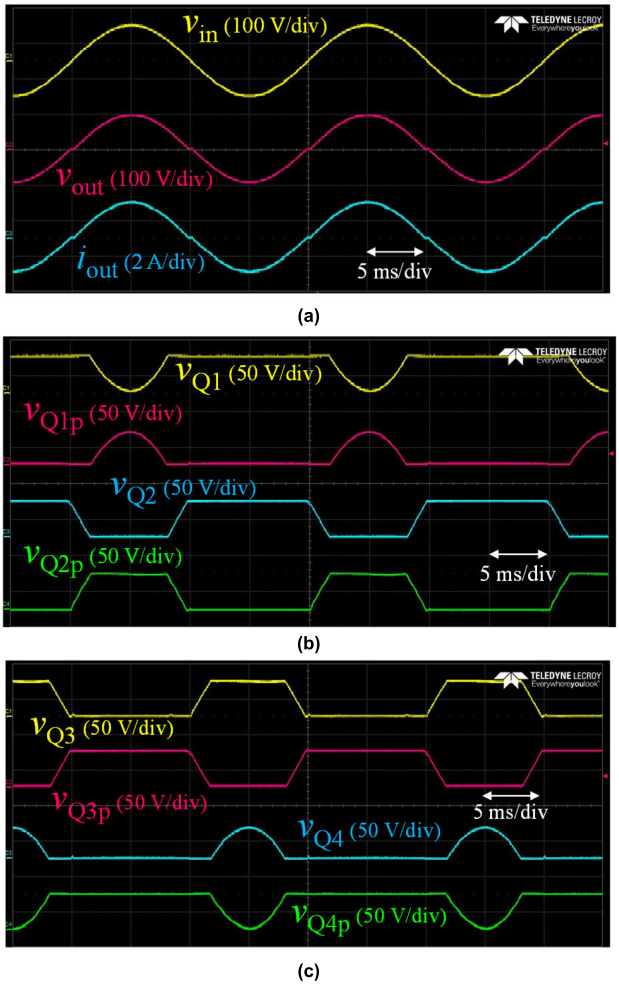

FIGURE 9. Experimental waveforms of 4-series DCLA under a pure resistive load (47 Ω). (a) Input and output voltages, and output current. (b) Drain–source voltage of MOSFETs Q1–Q2p. (c) Drain–source voltage of MOSFETs Q3–Q4p.

voltage of MOSFETs in a conventional class-B amplifier. It is known that such distortion can be compensated by adding a dc offset to the input voltage or by applying feedback control [12], [27]. The total harmonic distortion (THD) of the output voltage was measured as 3.89% among the three topologies in this experiment. The THD of the current is almost the same as that of the voltage because of the pure resistive load.

The drain–source voltage waveforms in Figs. 9 (b), (c), 10 (b), (c), and 11 (b), (c) show that each MOSFET separately operates as the active state for the reduction of the loss generated even in linear operations. The waveforms are in good agreement with the simulation results shown in Figs. 4–6. Moreover, it is verified that each drain–source voltage of the MOSFETs always becomes <50 V, which is one-fourth the dc input voltage of 200 V.

In the DCLA shown in Fig. 9, a MOSFET with a linear operation is changed in accordance with the output voltage range regularly. The upper MOSFETs (Q_1 and Q_2) perform

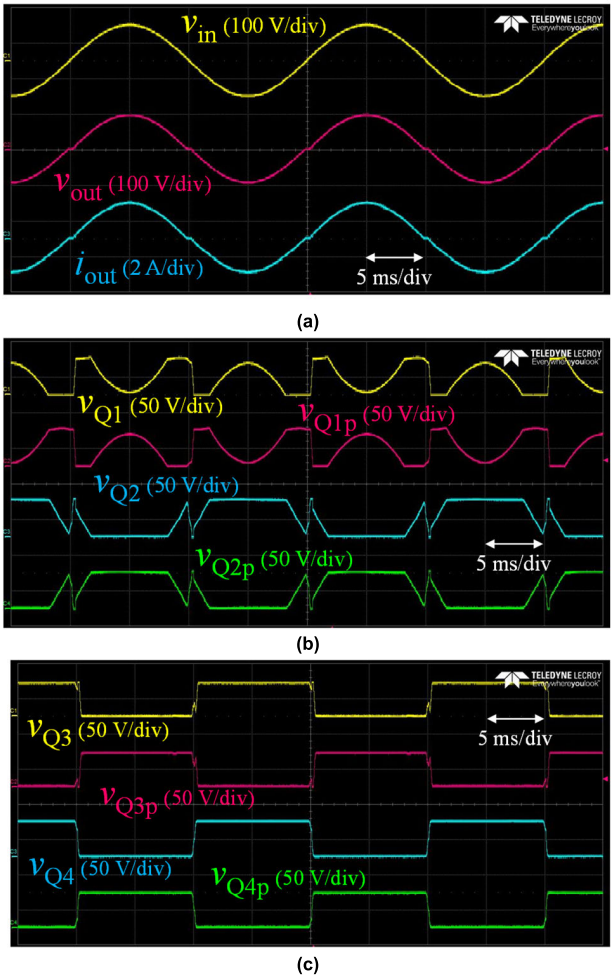

FIGURE 10. Experimental waveforms of 4-series FCLA under a pure resistive load (47 Ω). (a) Input and output voltages, and output current. (b) Drain–source voltage of MOSFETs Q1–Q2p. (c) Drain–source voltage of MOSFETs Q3–Q4p.

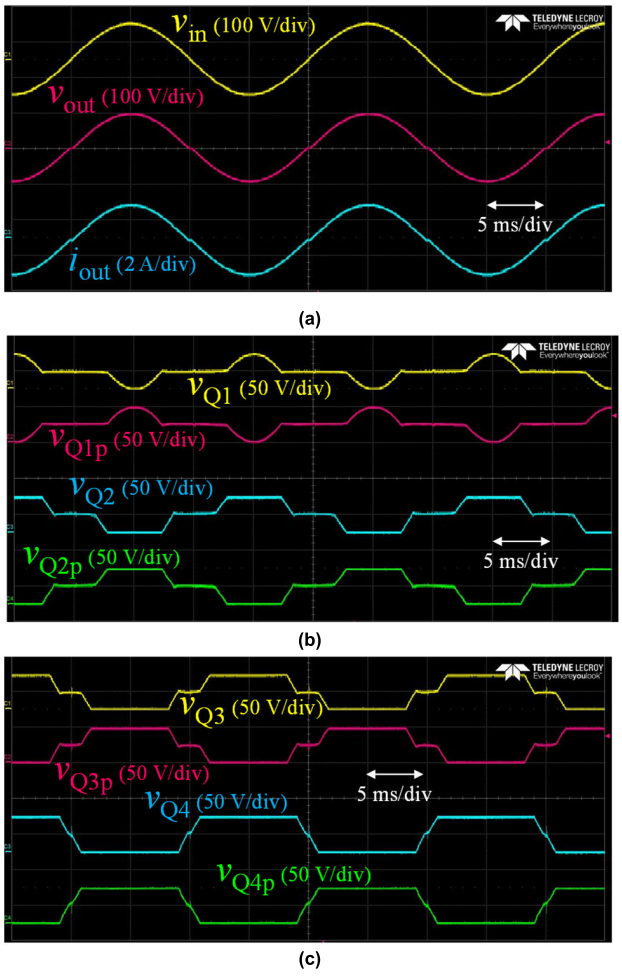

FIGURE 11. Experimental waveforms of 4-series MCLA under pure resistive load (47 Ω). (a) Input and output voltages, and output current. (b) Drain–source voltage of MOSFETs Q1–Q2p. (c) Drain–source voltage of MOSFETs Q3–Q4p.

the linear operation when the output voltage is high, and lower MOSFETs perform the linear operation when the output voltage is low.

In the case of the FCLA shown in Fig. 10, the MOSFETs (Q_3 and Q4) close to the output terminal in the circuit have a short period of linear operation, and the MOSFETs (Q_1 and Q_2) close to the input dc voltage terminals are characterized by a long linear operation period. Therefore, the heat generated by the device closer to the input dc voltage terminal increases, and the variations in the heat generation of the MOSFETs are larger than those of the DCLA.

In the MCLA shown in Fig. 11, it is notable that there are comparatively long sections of linear constant voltage in the drain–source terminals in each MOSFET. In this operation, each cell-module voltage is shared equivalently between the n-MOSFET and p-MOSFET.

The experimental results when the load condition is inductive−resistive are shown in Figs. 12–14. Fig. 12 shows the experimental waveforms in the DCLA under the condition of an inductive−resistive load. Here, a resistance of 37.5 Ω and an inductance of 80 mH were used as the load, and the power factor was calculated to be 0.83. It can be seen that the overall waveforms are adequately obtained, as in the case of the pure resistive load shown in Fig. 9. However, the phase of the small distortion in the output voltage v_{out} is shifted compared with the case of the pure resistive load. This occurs when the current direction is changed by the gate threshold voltage of the MOSFET via a mechanism similar to that of the well-known cross-over distortion. When the load power factor decreases, the distortion point shifts according to the zero-crossing point of the current. This distortion can also be suppressed in the same way as the general cross-over distortion by using a dc offset on the input voltage signal and feedback control.

Fig. 13 shows the experimental results for the FCLA under the resistive−inductive load condition. It is observed that the output voltage has a higher cross-over distortion compared

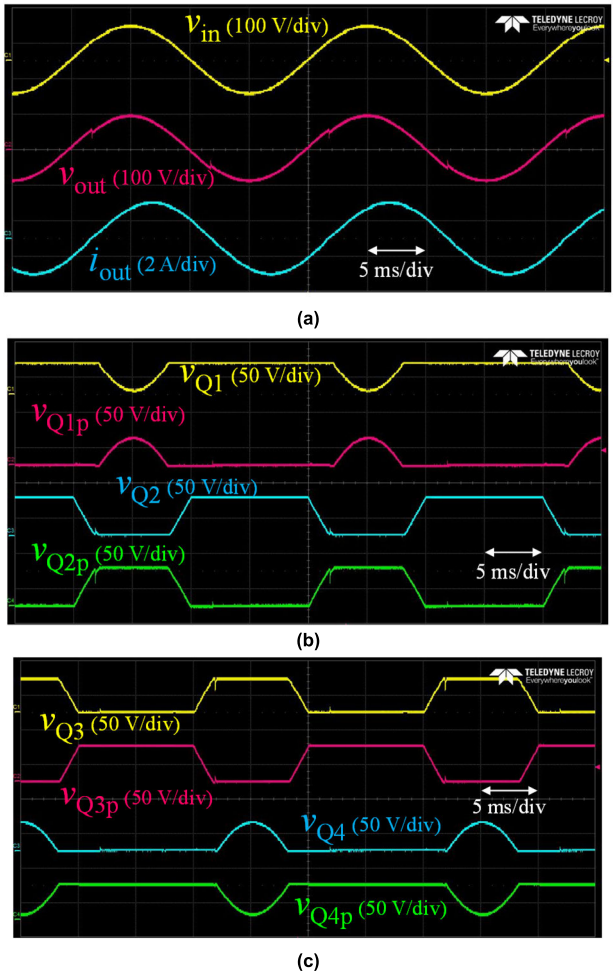

FIGURE 12. Experimental waveforms of 4-series DCLA under an inductive–resistive load (37.5 Ω and 80 mH). (a) Input and output voltages, and output current. (b) Drain–source voltage of MOSFETs Q1–Q2p. (c) Drain–source voltage of MOSFETs Q3–Q4p.

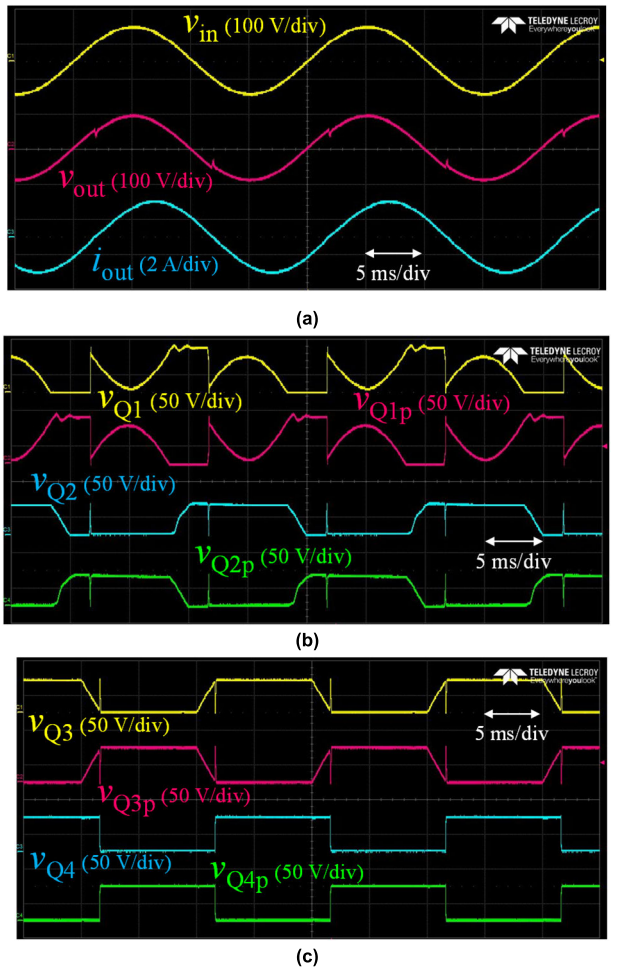

FIGURE 13. Experimental waveforms of 4-series FCLA under an inductive–resistive load (37.5 Ω and 80 mH). (a) Input and output voltages, and output current. (b) Drain–source voltage of MOSFETs Q1–Q2p. (c) Drain–source voltage of MOSFETs Q3–Q4p.

with the case of the pure resistive load in Fig. 10. Furthermore, spike voltages occur in the drain–source voltages of Q_2, Q_{2p}, Q_3, and Q_{3p}. These spike voltages occur when the current direction changes, and they are also a type of cross-over distortion. These drain−source voltages are always <50 V, which is one-fourth the dc input voltage of 200 V, and do not have a significant effect on EMI and loss.

Similarly, Fig. 14 shows the experimental waveforms in the case of MCLA when the load condition is inductive−resistive. It can be seen that proper waveforms with little surge are obtained in the same manner as in the DCLA and FCLA cases.

These results verify that the prototype circuits of the DCLA, FCLA, and MCLA operate adequately according to the principle under both resistive and inductive load conditions.

C. EFFICIENCY MEASUREMENT

The efficiency of the prototype circuits was measured using a power analyzer (Hioki PW6001) with a current probe (CT6841-05). The ideal and measured efficiencies for each topology obtained through theoretical and experimental investigations are summarized in Table 6. The prototype 4-series DCLA, FCLA, and MCLA achieved a higher efficiency of approximately 82% at an output power of 106 W. This is approximately the same as the ideal efficiency of 84.5% and 3 percentage points higher than the ideal efficiency of the conventional class-B linear amplifier. The difference between the measured and ideal efficiencies is considered mainly to be caused by the cross-over distortion and conduction losses of the MOSFETs and diodes. In the MCLA, the measured efficiency was slightly lower than those of the other two topologies, because it has the operation states that the current flows through multiple MOSFETs, as indicated in Table 4. Conduction loss is considered to negatively affect efficiency. However, there are few efficiency differences among the three topologies. In addition, it is expected that, as the number of series MOSFETs increases, the efficiency increases according to the principle, as shown in Fig. 7 [7], [12].

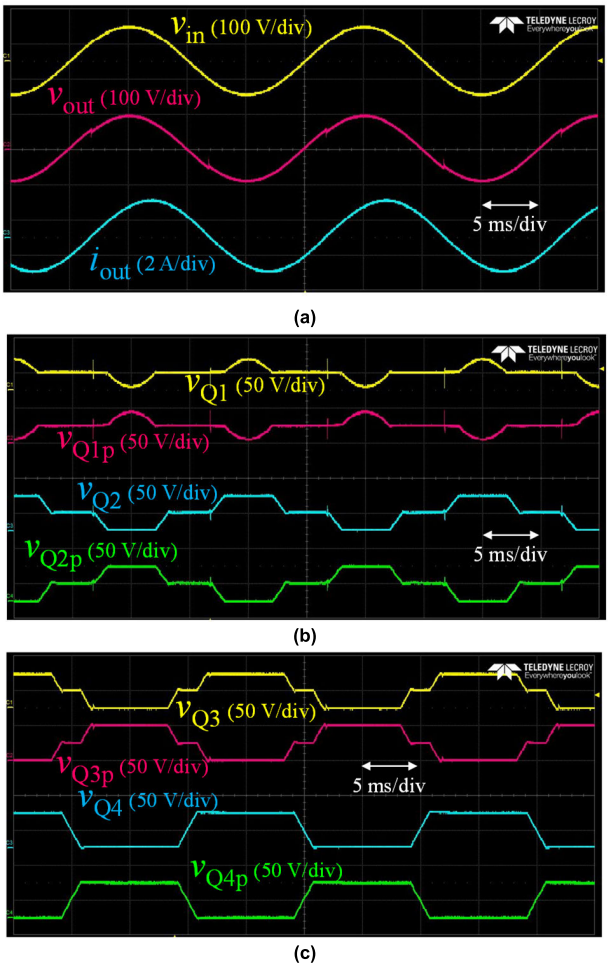

FIGURE 14. Experimental waveforms of 4-series MCLA under an inductive–resistive load (37.5 Ω and 80 mH). (a) Input and output voltages, and output current. (b) Drain–source voltage of MOSFETs Q1–Q2p. (c) Drain–source voltage of MOSFETs Q3–Q4p.

TABLE 6. Comparison of ideal and measured efficiencies in the three 4-Series MLLA topologies at an output power of 106 W.

Topology	Conventional class-B LA	4-series DCLA	4-series FCLA	4-series MCLA
Ideal efficiency	78.5%	84.5%		
Measured efficiency	—	82.0%	82.2%	81.3%

V. DISCUSSION OF EFFICIENCY AND CAPACITOR VOLTAGE BALANCE OF THE MLLA FAMILY

A. EFFICIENCY CONSIDERING CONDUCTION LOSS

The loss of the linear operation device in the MLLA can be reduced when the series device number n increases. In contrast, the conduction loss is proportional to the product of the device series number n and the on-state resistance. The theoretical efficiency equation (4) can be derived by adding the conduction loss to (3), which includes only the linear operation loss.

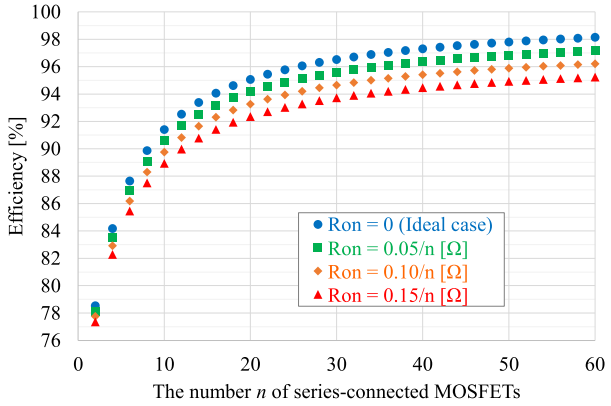

FIGURE 15. Relationship among the efficiency, number of MOSFETs, and on-state resistance of MOSFETs in the MLLA family.

$$\eta = \frac{n^2\pi}{16\sum_{k=1}^{\frac{n}{2}}\sqrt{nk-k^2}}\left\{1-\frac{2R_{on}I_{rate}}{V_d}(n-1)\right\} \quad (4)$$

where the R_{on} [Ω] is the on-state resistance of the power devices in total, I_{rate} [A] is the peak value of the output ac current, and V_d [V] is the source dc voltage. The first term in the curly braces corresponds to the loss of the linear operation, and the second term corresponds to the conduction loss. Although the loss caused by the linear operation does not depend on the load current, the conduction loss depends on the load current.

Here, we will discuss the future trends of efficiency based on future WBG device technology. In the MLLA family, the device voltage rating (where, in this discussion, a MOSFET is assumed) can be reduced in proportion to $1/n$. When the voltage rating of each MOSFET is reduced, the on-state resistance also decreases in general. Let us assume that the on-state resistance R_{on} is proportional to $1/n$ [36]:

$$R_{on} = \frac{R_0}{n} \quad (5)$$

where R_0 is assumed to be constant, which is the product of the on-state resistance of each device and an adjusting coefficient. Substituting (5) into (4) and drawing a graph yields Fig. 15, in which the horizontal axis is n and the vertical axis is the efficiency. The concrete values of $V_d = 200$ V and $I_{rate} = 20$ A were assumed for the numerical calculation. The parameter R_0 was changed from 0 to 0.15 in four different values. When $R_0 = 0$, this curve becomes identical to that in Fig. 7, in which the conduction loss is not included. As n increases, the efficiency also increases and reaches 100% for a significantly large number.

Equations (4) and (5) will be useful when the rough design of the MLLA is attempted as a comparison of several realizations under the given specification. As a future trend of WBG devices, the physical property constant dielectric breakdown strength is a factor of 10timesgreater than that of Si; consequently, the on-state resistance of a WBG MOSFET can

become much lower than that of a Si device because the drift layer of the MOSFET might be thinner in WBG devices [37]. Therefore, in Fig. 15, an efficiency of 95% might be realistic with $n = 20$, depending on the future development of WBG devices.

B. VOLTAGE BALANCE OF CAPACITORS

As shown in Fig. 15, the series device number n should be large to achieve a relatively high efficiency of >90%. Each capacitor voltage should always be maintained around the commanded value because the imbalance of the capacitor voltage increases the voltage stress and loss of an active-state MOSFET. With the common gate driver circuit shown in Fig. 1, the main function is to control the output voltage, if all the capacitor voltages are assumed stay in each commanded value. As a result, control of the capacitor voltage balance was not implemented in this concentrated gate control. There are two approaches for maintaining the capacitor voltages in pre-designed values:

Approach 1. External voltage-balancing circuit:

A new external circuit is required, but the control is relatively simple.

Approach 2. Individual gate circuit for maintaining capacitor voltage by charge and discharge control:

Each gate driver needs to be modified so that it independently controls the power device in the active, on, and off states. Each capacitor voltage should be controlled by charging and discharging using a proper combination of circuit operating modes.

Approach 2 becomes more complicated than approach 1 in general; however, an external circuit is not required. Which approach is better depends on the circuit topology. In [10], an external circuit configured by switched capacitor converters was added, and voltage-balancing control was implemented. In [27], a capacitor voltage-balancing control utilizing redundant circuit operation modes was reported, because there is enough degree of freedom of circuit operation states realized by individual gate circuits as in approach 2. There is very little literature on DCLAs and FCLA, but progress in this field is expected. On the subject of capacitor voltage balancing for the MCLA, there are many studies on multilevel converters using modular cascaded circuits [34], [35], [38], which are useful for the implementation of capacitor voltage control. In [35], capacitor voltage is controlled by the external circuit as in approach 1; in [34], [38], the capacitor voltage is maintained by controlling the circulating current in the circuit, as in approach 2. For other expected future topologies of the MLLA family, the realization of voltage-balancing control is also achievable by extending the existing techniques for various multilevel converters.

C. PRACTICALITY AND FUTURE DIRECTIONS

In the experimental investigation in Section IV, laboratory-scale prototypes were demonstrated. When the number of series devices is small, there is a limit to increasing the handled voltage owing to problems with heat dissipation and withstand voltage; however, it becomes possible to handle a practical voltage by increasing the number of series devices, as reported in [10].

In addition to the above issues, one of the bottlenecks for practical use is the comparative worse characteristics of p-channel MOSFETs in the lower arms in each MLLA topology. To solve this issue, a topology that removes the p-channel MOSFET has been proposed [39]. Furthermore, when the individual linear gate drivers are applied for each MOSFET, p-channel MOSFETs can be removed by realizing the equivalent operation of the p-channel MOSFET using only an n-channel MOSFET [39].

An implementation method for many devices is another issue to realize high efficiency practically. For example, in comparatively small power converters, integrated circuit technology is expected to be used for implementing many devices in a one-chip semiconductor in the future. For large-scale converters, the implementation cost of many devices is not a significant issue. In several applications, such as motor drive systems, grid-connected inverters, and power supplies for medical equipment, the benefit of the lower noise and harmonics in the MLLA is expected to have a greater impact than those of the above issues. MLLA topologies have the potential to be used in some practical applications that require strict performance for generating noise and harmonics. Even if the number of series devices is significantly increased, the MLLA cannot achieve a higher efficiency than that of switching mode converters. Therefore, the cost of losses and heatsinks become higher in the MLLA. However, noise and harmonics are not generated in principle, so the cost of passive components such as filters can be reduced in the MLLA. The choice between switching mode converters and MLLA should depend on the specifications and application.

Moreover, linear amplifiers do not require an output filter, and it is well known that linear amplifiers can eliminate the delay time in the filter and achieve excellent transient response. The transient response of the MLLA is the same as that of conventional linear amplifiers, such as class-B amplifiers. The performance of the output response is mostly determined by the product of the input resistance and capacitance of each MOSFET. Moreover, in the case of the MLLA, MOSFETs with lower rated voltage and small capacitance can be used. Consequently, there is a possibility that the output response can be improved compared to that of class-B amplifiers.

VI. CONCLUSION

In this study, a family of EMI noise-free MLLAs was proposed, and three typical types of members—DCLA, FCLA, and MCLA—were described. The circuit topology, operation principle, and efficiency were summarized, and their advantages and disadvantages were clarified. By using 4-series

circuits, the experimental results were shown for the three topologies. An efficiency of >82% was measured at 106 W output, which is 3 percentage points higher than that of the class-B linear amplifier. Through a discussion on the possible highest efficiency, by assuming that future new power devices may further decrease the on-state resistance, it was theoretically clarified that the efficiency of the MLLA will become as high as that of switching power converters. The feasibility of voltage-balancing control of the capacitors was discussed, which is also valuable for the topology selection and design of MLLA, including expected future new topologies. This study will prove useful when the selection of EMI-free power conversion is needed. The MLLA is one of the excellent candidates for applications without switching operations.

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