Demonstration of an efficient single flux quantum logic circuit by introducing a local magnetic flux biasing

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Abstract: We investigated local magnetic flux biasing (LFB) that induces a phase shift in superconductor circuits by locally applying a magnetic field through the superconductor loop with Josephson junctions. The arbitrary phase shift can be achieved using LFB without modifying the circuit fabrication process. To quantitatively evaluate the effects of introducing LFB for practical superconductor circuit applications, we designed a single flux quantum (SFQ) based non-destructive read-out flip-flop with complementary outputs (NDROC) and a delay flip-flop with complementary outputs (DFFC). The circuit area and static power consumption of the NDROC based on LFB architecture (LFB-NDROC) are approximately 67% and 36% of a conventional NDROC, respectively. The measured bias margin of the LFB-NDROC was in the range of 69%–129%. Using LFB, we were able to reduce the circuit area and power consumption for the DFFC by 67% and 83%, respectively. The measured bias margin of the DFFC with LFB was between 115%–128%. LFB enabled us to implement a 5-to-32 SFQ decoder which comprises NDROC trees with a reduced circuit area of approximately 60% of a conventional decoder. The results

obtained in this study can be applied to not just SFQ circuits but other superconductor circuits also, as they improve the area and power efficiency of such circuits.

Keywords: SFQ circuit, flip-flop, phase shift, circuit design methodology

1 Introduction

Currently, complementary metal-oxide-semiconductor (CMOS) integrated circuits are used for computing in information technology. Although the CMOS integrated circuit technology in recent years has significantly advanced, it is approaching the end forecasted by Moore's law [1, 2]. The power consumption of the CMOS circuit becomes a critical problem as the integration level increases [3]. Superconductor circuits, such as rapid single flux quantum (RSFQ) circuits [4], LR-biased RSFQ circuits [5], energy-efficient RSFQ circuits [6], reciprocal quantum logic circuits [7], and adiabatic quantum flux parametron circuits [8], are capable of low-power and high-speed operations. Therefore, they have a potential for Beyond CMOS [9].

One of the challenges of the currently available superconductor circuit technology is its low-integration level due to immature fabrication technology when compared with the CMOS circuit technology [10, 11]. In addition to improving its fabrication process, an implementation method for area-efficient superconductor circuits should also be explored. Improving the energy efficiency of the superconductor circuits is also important. This is because the superconductor circuits with conventional architecture still requires a considerable power for cooling, although it is significantly lower than that for semiconductor circuits. Reduction in the power consumption of superconductor circuits enables us to increase the circuit scale implemented in a refrigerator with limited cooling capacity. One method for improving the performance of the superconductor circuits is by adopting various superconductor phase shift elements (PSEs) that shift the phase of the macroscopic wave function in the superconductor circuit [12, 13]. Using PSEs in superconductor circuits reduces the power consumption and circuit area because it substitutes the PSE architecture with a conventional bias current architecture [14, 15]. The stabilization of a superconductor circuit operation can be achieved by employing a simple and symmetric circuit structure that utilizes the π-phase shift of the PSEs [14, 16].

In previous studies, researchers have adopted the following PSEs: superconductor loops with trapped flux quantum [17, 18], π-shifted Josephson junctions [19, 20], ferromagnetic patterns buried in superconductor circuits [12, 21], and a Josephson phase battery [22]. However, using ferromagnetic materials and a phase battery requires a significant modification of the circuit fabrication process. The application of a magnetic field during the circuit cooling process is required when flux trapping and magnetization of ferromagnetic materials are adopted. In all these methods the challenge is to achieve a precise and reproducible phase control. In addition, applying a magnetic field during the cooling process could induce an undesired flux trapping that deteriorates the superconductor circuit operation [23].

In this study, we propose a local magnetic flux biasing (LFB) to introduce a phase shift in the superconductor circuit. LFB can be used without modifying the circuit fabrication process. The arbitrary phase shift can be realized by controlling the applied magnetic flux. A similar approach of applying a magnetic field to improve the operation characteristics of the superconductor circuit was employed in flux-biased SQUIDs [24]. But in flux-biased SQUIDs [24] the magnetic field was used to adjust the operating point of SQUIDs and not to shift the phase. We have designed an SFQ based non-destructive read flip-flop with complementary outputs (NDROC) [13] and a delay flip-flop with complementary outputs (DFFC) by using LFB to reduce the circuit area and power consumption. We experimentally evaluated the LFB flip-flops and studied the circuit area reduction and power of an SFQ binary decoder by introducing LFB.

2 Local Flux Biasing for Phase Shift

Fig. 1 (a) illustrates an equivalent circuit diagram of a superconductor loop containing Josephson junctions with LFB. The inductance of the superconductor loop is magnetically coupled to the flux bias current I_{LFB}. The magnetic flux through the superconductor loop (Φ_{LFB}) induces a phase shift

of the inductance in the superconductor loop.

The phase shift θ_{LFB} versus Φ_{LFB} is illustrated in Fig. 1 (b). We calculated θ_{LFB} from simulated current value flowing through the superconductor loop using the Josephson integrated circuit simulator (JSIM) [25]. As shown in Fig. 1 (b), the phase shift θ_{LFB} can be controlled by adjusting Φ_{LFB}, which is induced by I_{LFB}. Assuming the phase shift to be π, half of Φ_0 is applied to the superconductor loop even in the initial state. By using the phase shift of π, the magnetic flux of approximately $\pm 0.5\Phi_0$ through the superconductor loop can be used to express two internal logic states. The internal state expression by the half flux quantum is suitable for designing an SFQ flip-flop with complementary outputs [16]. The circuit area can be reduced by inducing a phase shift in the LFB architecture because it does not require a high inductance to store the half flux quantum, whereas a conventional SFQ circuit needs a high inductance i.e., $LI_{\mathrm{C}} > \Phi_0$. Here, L is the inductance and I_{C} is the critical current for the Josephson junction in the superconductor loop to keep one flux quantum. The static power consumption of SFQ flip-flops can also be reduced by using LFB because the two logic states,$\pm 0.5\Phi_0$, can be expressed without applying a bias current [16], which is the static power consumption source for bias resistors.

LFB can induce a phase shift without modifying the circuit fabrication process and does not require an input current during the cooling process. We can shift the phase for each circuit part of the chip by simply applying a flux bias line. LFB can be applied to any superconductor circuit other than an SFQ circuit, such as a quantum flux parametron [15].

3 Design of SFQ flip-flops using the LFB

We designed an SFQ NDROC and a DFFC using the LFB architecture. SFQ NDROC and DFFC are the main circuit components in binary decoders [26, 27], dual rail logic systems [28, 29], etc. Therefore, the designed LFB-NDROC and LFB-DFFC have applications in decoders and other

various systems. They are designed to be compatible with SFQ cells in the CONNECT cell library [30].

3.1 NDROC

Fig. 2 presents an equivalent circuit diagram of the NDROC using LFB architecture (LFB-NDROC). The flux bias line is coupled to the three loops A, B, C with magnetic couplings of k_3, k_2, and k_1, respectively. The storage loop which stores the half flux quantum to express logic states is loop B as shown in Fig. 2. In the initial '0' state, the circulating current flows in the direction of the arrows in loops labeled A, B, and C in Fig. 2. Because these circulating currents increase the bias currents flowing through J_3, J_6, and J_9, these three junctions are easily switched. When the clock (clk) signal supplied to the LFB-NDROC in the '0' state, the output is obtained at the "doutc" port due to switching of J_9, but the output is not obtained at "dout" due to the switching of the escape junction J_6. When "din" signal is supplied in the '0' state, the direction of the circulating currents for loops A–C is reversed due to switching of J_3 and J_7. The input flux quantum is stored in the storage loop. This state corresponds to state '1'. When the "clk" is supplied in state '1', the output is obtained at the "dout" port due to switching of J_{10}, whereas the output is not obtained at "dout" due to the switching of the escape junction J_5. State '1' is maintained due to switching of J_8 after switching of J_{10}.

Due to the symmetrical nature of this operation relative to the internal state, the circuit structure and parameters are also symmetrical, as shown in Fig. 2. The LFB-NDROC can be designed using only one symmetric storage loop, whereas the conventional SFQ NDROC needs two storage loops to generate complementary outputs. Table 1 compares the static power consumption, area, and number of Josephson junctions between the LFB-NDROC and a conventional NDROC of the CONNECT cell library. It should be noted that the on-chip power consumption of I_{LFB} is zero

Table 1: Comparison of the static power consumption, area, and number of Josephson junctions between the LFB-DFFC and a conventional NDROC of the CONNECT cell library. These circuits are compared for the 10 kA/cm^2 Nb process.

	LFB-NDROC	Conventional NDROC
Static power consumption	2.25 μW	8.56 μW
Area	120 μm $\times$ 40 μm	120 μm $\times$ 120 μm
Number of Josephson junctions	15	33

because the on-chip resistor does not provide I_{LFB}. The area of the LFB-NDROC is 120 μm $\times$ 40 μm, whereas the area of the conventional NDROC is 120 μm $\times$ 120 μm. By introducing LFB, we can improve the circuit configuration of the NDROC and reduce the number of Josephson junctions. Therefore, we can design an LFB-NDROC which is approximately 67% smaller than a conventional NDROC. The static power consumption of the LFB-NDROC is also approximately 74% lower than a conventional NDROC.

3.2 DFFC

DFFC is a delay flip-flop that has complementary outputs. Fig. 3 presents an equivalent circuit diagram of DFFC using the LFB architecture (LFB-DFFC). The mutual couplings between the circuit inductance and flux bias line induces a phase shift of approximately π in the storage loop of the LFB-DFFC. In the initial '0' state, the circulating currents flow in the direction of the arrows in loops labeled A, B, and C as shown in Fig. 3. The circulating currents provide an easy switching of J_2, J_4, and J_6. When the clock (clk) signal is supplied to the LFB-DFFC in state '0', the output is obtained at the "doutc" port due to the switching of J_6 and no output is obtained at "dout" due to the switching of the escape junction J_4. The '0' state is maintained due to the switching

Table 2: Comparison of the static power consumption, area, and number of Josephson junctions between the LFB-DFFC and a conventional DFFC of the CONNECT cell library. These circuits are compared for the 2.5 kA/cm^2 Nb process.

	LFB-DFFC	Conventional DFFC
Static power consumption	1.5 μW	9.0 μW
Area	80 μm $\times$ 80 μm	120 μm $\times$ 160 μm
Number of Josephson junctions	11	33

of J_5 after switching J_6. When the "din" signal is supplied in the '0' state, the direction of the circulating currents for loops A–C is reversed due to the switching of J_2 and J_5. The input flux quantum is stored in the storage loop. This state corresponds to state '1' of the LFB-DFFC. When "clk" is supplied in state '1', the output is obtained at the "dout" port due to switching of J_7, but no output is obtained at "dout" due to the switching of the escape junction J_3. The state of '1' is reset to '0' because the LFB-DFFC does not have a non-destructive circuit configuration like the LFB-NDROC.

Table 2 compares the static power consumption, area, and number of Josephson junctions between the LFB-DFFC and a conventional DFFC of the CONNECT cell library. The area of the LFB-DFFC is 80 μm $\times$ 80 μm. By introducing LFB, we can reduce the circuit area and static power consumption of the DFFC by 67% and 83%, respectively.

4 Experimental results

4.1 LFB-NDROC

Fig. 4 illustrates a microphotograph of the LFB-NDROC fabricated by the National Institute of Advanced Industrial Science and Technology (AIST) 10 kA/cm^2 Nb process [31]. A flux bias line

is magnetically coupled to the inductance of the storage loop. The circuit was tested at 4.2 K. Fig. 5 presents the experimentally obtained voltage-time waveform for the LFB-NDROC low-speed test. The input to the circuit for SFQ signals was given using DC/SFQ converters [4]. We observed the output of the LFB-NDROC by monitoring the output voltages of the SFQ/DC converters with a toggle flip-flop [4] connected to the output ports of the LFB-NDROC. We confirmed the correct complementary output, as well as the non-destructive operation of the designed LFB-NDROC. Fig. 6 illustrates the dependence of the measured and simulated bias margins on the applied magnetic flux Φ_{LFB}. As shown in Fig. 6, the measured bias margin shifts towards the higher Φ_{LFB} side. This occurs because of circuit parameter variations and the incorrect coupling factor obtained from the designed layout. The maximum measured bias margin normalized by the designed bias voltage (2.5 mV, 0.889 mA) was between 69%–129% when the applied magnetic flux for LFB was $0.58\Phi_0$. This induces an approximate phase shift of π in the storage loop.

4.2 LFB-DFFC

Fig. 7 shows a microphotograph of the LFB-DFFC fabricated by the AIST 2.5 kA/cm^2 Nb process [32]. Fig. 8 presents the waveform of the LFB-DFFC obtained from the experiment. When "clk" signal was supplied, the output was obtained either at "doutc" or "dout" depending on the internal state. We verified the correct operation of the designed LFB-DFFC. Fig. 9 illustrates the dependence of the measured and simulated bias margins of the LFB-DFFC on the applied magnetic flux Φ_{LFB}. The maximum measured bias margin normalized by the designed bias voltage was between 115%–128% when the magnetic flux applied for LFB was $0.57\Phi_0$. The measured bias margin was lower than the simulation measurement due to the parasitic coupling or the asymmetric circuit layout. The asymmetric circuit layout could induce a circuit parameter variation, especially in the coupling strength between I_{LFB} and the storage loop.

Table 3: Comparison of the area of a 5-to-32 output decoder using LFB and a conventional decoder [33].

	Conventional	NDROC using LFB	DFFC using LFB
Area [mm^2]	0.36×1.95	0.18×1.95	0.28×1.31

5 Design of SFQ decoder using the LFB

One of the applications of the NDROC and DFFC is as a decoder, which is an indispensable device for building digital circuit systems. In the case of an 8-bit by 32-word SFQ shift register memory system, the decoder occupies 35% of the memory's circuit area [33]. The reduction in the circuit area of the SFQ decoder results in an improvement in the circuit area and latency of the SFQ memory system.

Fig. 10 (a) presents a simple layout of an LFB decoder. The N-output decoder is composed of (N-1) NDROCs/DFFCs with LFB, aligned in a binary tree shape. One flux bias line is wired to all the NDROCs/DFFCs for shifting the phase. We also introduced a compact decoder design [33] as shown in Fig. 10 (b). We can implement the LFB compact decoder using a short flux bias line as shown in Fig. 10 (b). The adaptation of a compact design decoder will also help in reducing the wiring in the decoder.

To verify the area efficiency of the decoder with LFB, we evaluated the area of a 5-to-32 decoder using LFB, and compared the results with a conventional memory system [33]. Table 3 compares the area of a 5-to-32 output decoder with LFB and that of a conventional decoder. In the 5-to-32 decoder, seven NDROCs/DFFCs are used. All decoders in Table 3 employ the compact circuit design mentioned above. Because the circuit area of the NDROC/DFFC with LFB is 1/3 of a conventional NDROC/DFFC, the area of the decoder is reduced by using LFB. As shown in table 3, by introducing LFB, we can design a decoder with an area that is approximately 60% of a

conventional decoder.

6 Conclusion

We proposed the introduction of LFB in superconductor circuits that shifts the phase without altering the circuit fabrication process and manipulating the current during the cooling process. Based on the concept of LFB, we designed an SFQ NDROC and a DFFC. LFB was effective in reducing the circuit area of the SFQ flip-flop with complementary outputs and in obtaining a large bias margin. The measured bias margins of the NDROC and DFFC with LFB architecture were between 69%–129% and 115%–128%, respectively. We designed a 5-to-32 output SFQ binary decoder using LFB and determined that the circuit areas of the decoder can be reduced by approximately 60% of a conventional decoder.

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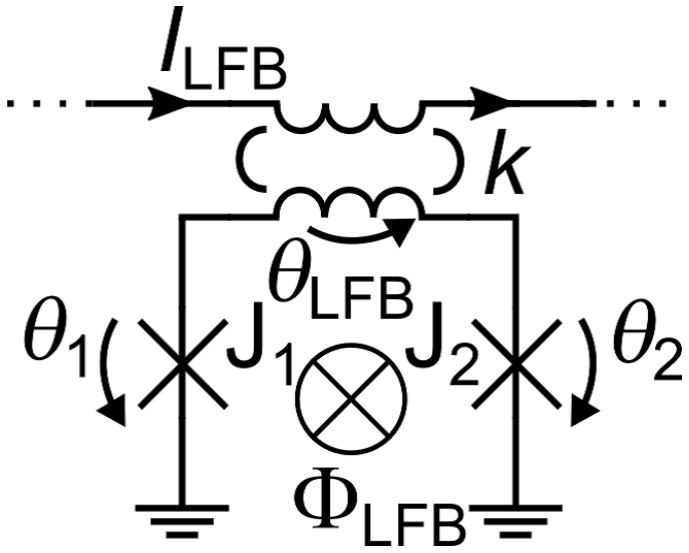
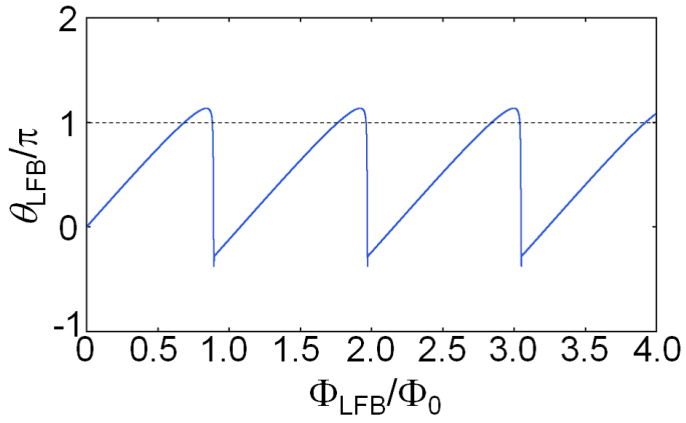


(a)



(b)

Figure 1: (a): Equivalent circuit diagram of a superconductor loop where LFB is introduced. The magnetic flux through the superconductor loop induces a phase shift in the inductance of the superconductor loop. (b): Phase shift θ_{LFB} versus the applied magnetic flux Φ_{LFB} in the superconductor loop. The magnetic flux applied is normalized by Φ_0. $J_1 = J_2 = 216$ μA. The inductance in the superconductor loop and flux bias line are both 10 pH. The coupling factor k is 0.5.

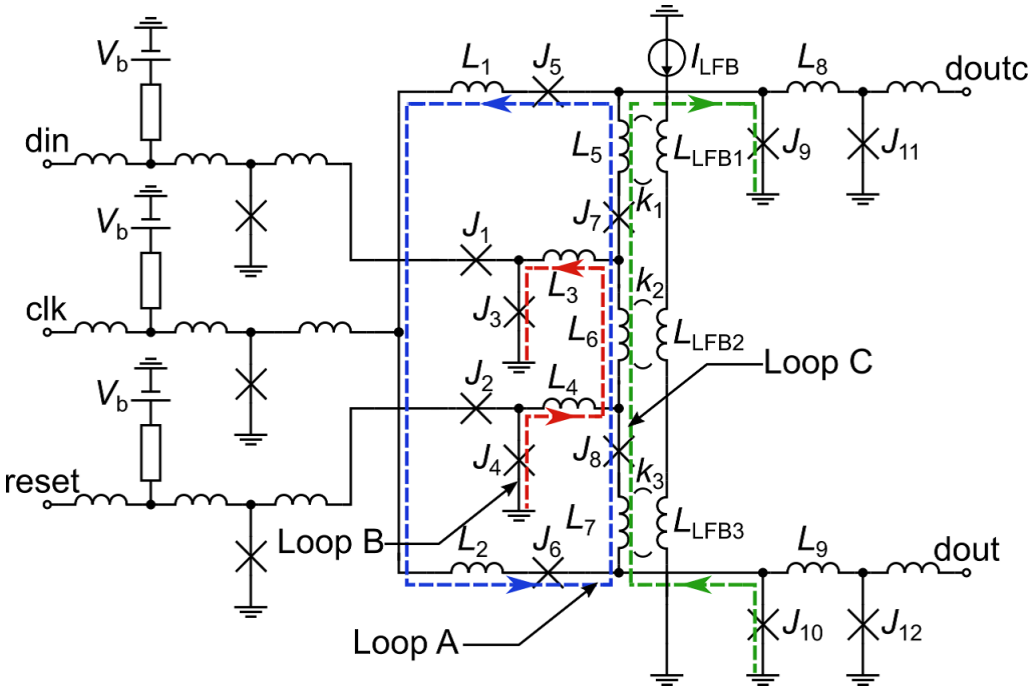


Figure 2: Equivalent circuit diagram of the NDROC using LFB. The storage loop is loop B. In the initial state, the current induced by LFB flows in the direction of the arrows. J_1 = J_2 = 213 μA, J_3 = J_4 = 139 μA, J_5 = J_6 = 169 μA, J_7 = J_8 = 88 μA, J_9 = J_{10} = 100 μA, J_{11} = J_{12} = 190 μA, L_1 = L_2 = 1.80 pH, L_3 = L_4 = 2.49 pH, L_5 = L_7 = 2.67 pH, L_6 = 2.53 pH, L_8 = L_9 = 4.73 pH, L_{LFB1} = L_{LFB2} = L_{LFB3} = 64.3 pH, k_1 = 0.0369, k_2 = 0.0918, k_3 = -0.0369, and I_{LFB} = 900 μA. The phase shift is induced by the mutual inductances k_1, k_2, and k_3.

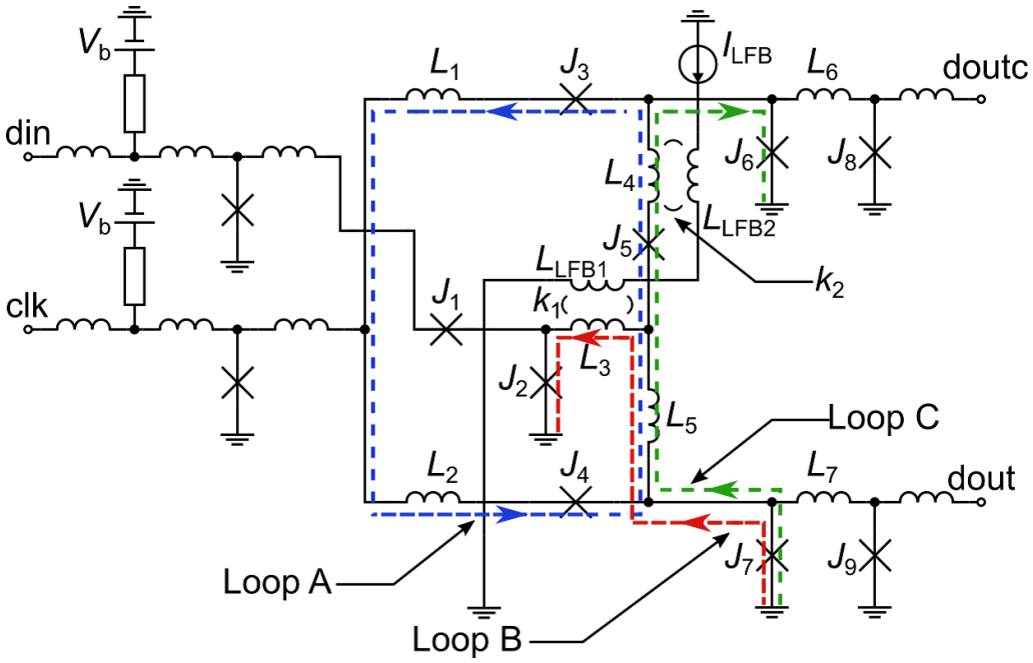


Figure 3: Equivalent circuit diagram of the DFFC using LFB. Each LFB applies a magnetic flux corresponding to $0.5\Phi_0$. The storage loop is loop B. In the initial state, the current induced by LFB flows in the direction of the arrows. J_1 = 186 μA, J_2 = 135 μA, J_3 = 107 μA, J_4 = 147 μA, J_5 = 84 μA, J_6 = 84 μA, J_7 = 105 μA, J_8 = 100 μA, J_9 = 151 μA, L_1 = 1.57 pH, L_2 = 1.16 pH, L_3 = 2.81 pH, L_4 = 2.33 pH, L_5 = 2.37 pH, L_6 = 5.22 pH, L_7 = 5.49 pH, L_{LFB1} = L_{LFB2} = 19.7 pH, k_1 = 0.300, k_2 = 0.352, I_{LFB} = 480 μA.

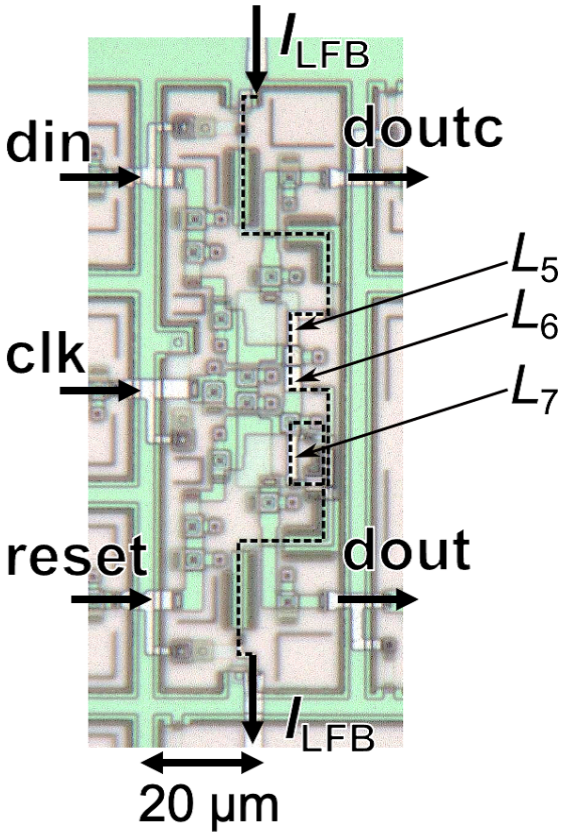


Figure 4: A microphotograph of the NDROC with LFB illustrated in Fig. 2 (10 kA/cm^2). The broken line represents trace of the flux bias line.

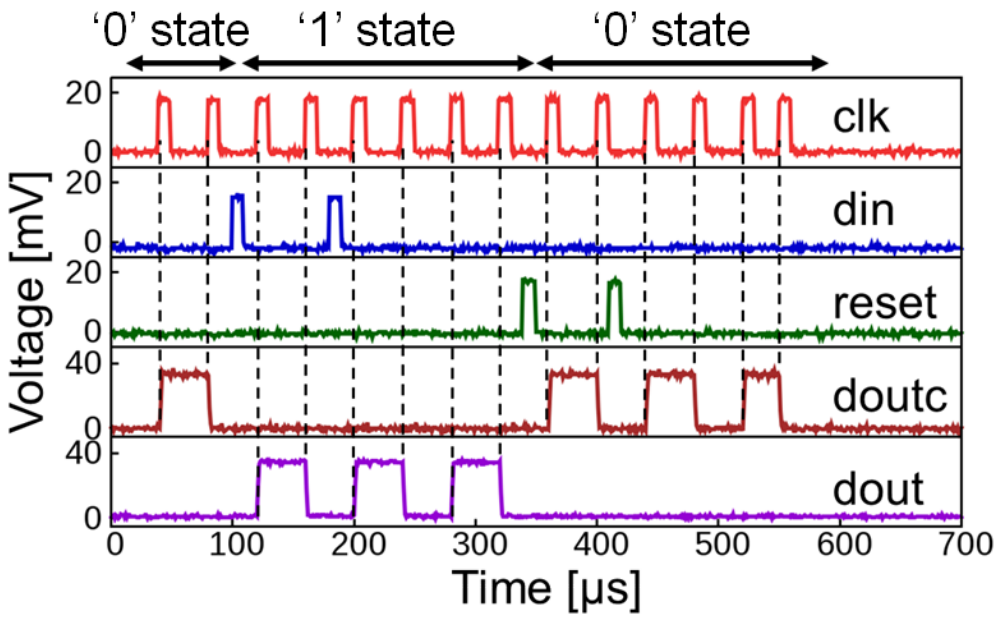


Figure 5: Low-speed test waveform of the NDROC with LFB. Two waveforms (dout and doutc) are outputs from SFQ/DC converters with a T flip-flop [4]. The voltage transitions represent SFQ signal outputs. ‘0’ and ‘1’ SFQ outputs, correspond to voltage transitions at “doutc ” and “dout ”, depending on the internal state, are obtained synchronized with the clock (clk) input.

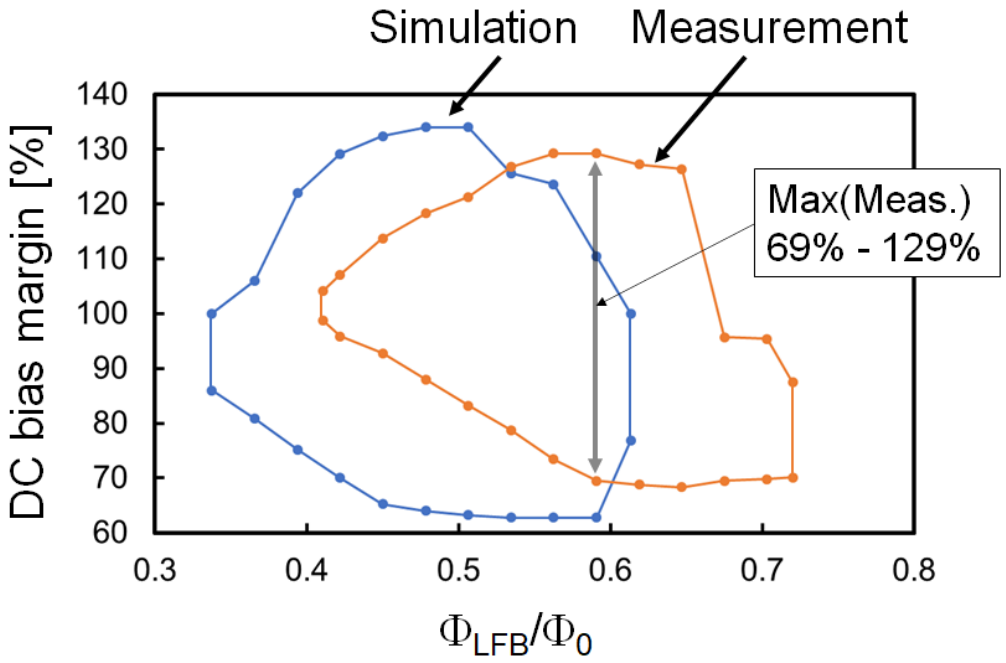


Figure 6: Measured and simulated bias margins for the NDROC (10 kA/cm^2) illustrated in 2 as a function of the applied magnetic flux Φ_{LFB}. The bias margin is normalized by the designed bias voltage of 2.5 mV.

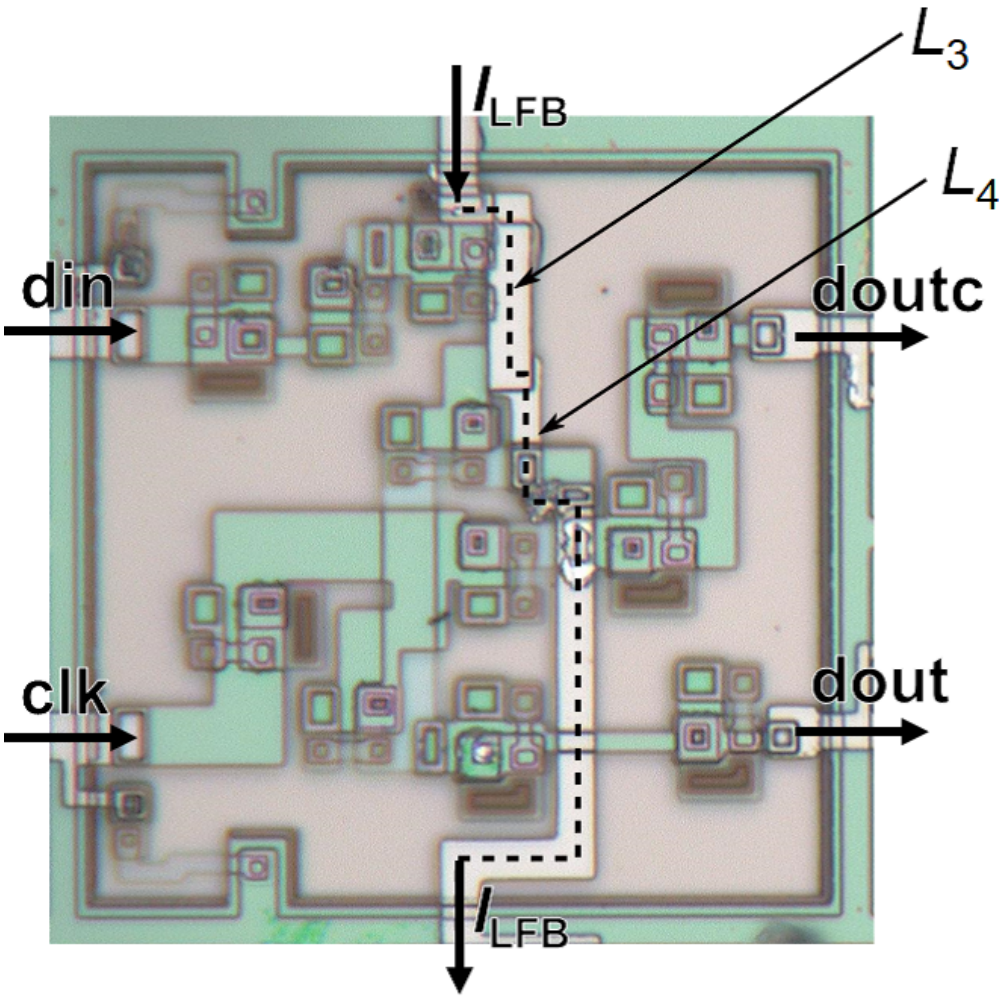


Figure 7: A microphotograph of the DFFC (2.5 kA/cm^2) using LFB illustrated in Fig. 3. The broken line represents trace of the flux bias line.

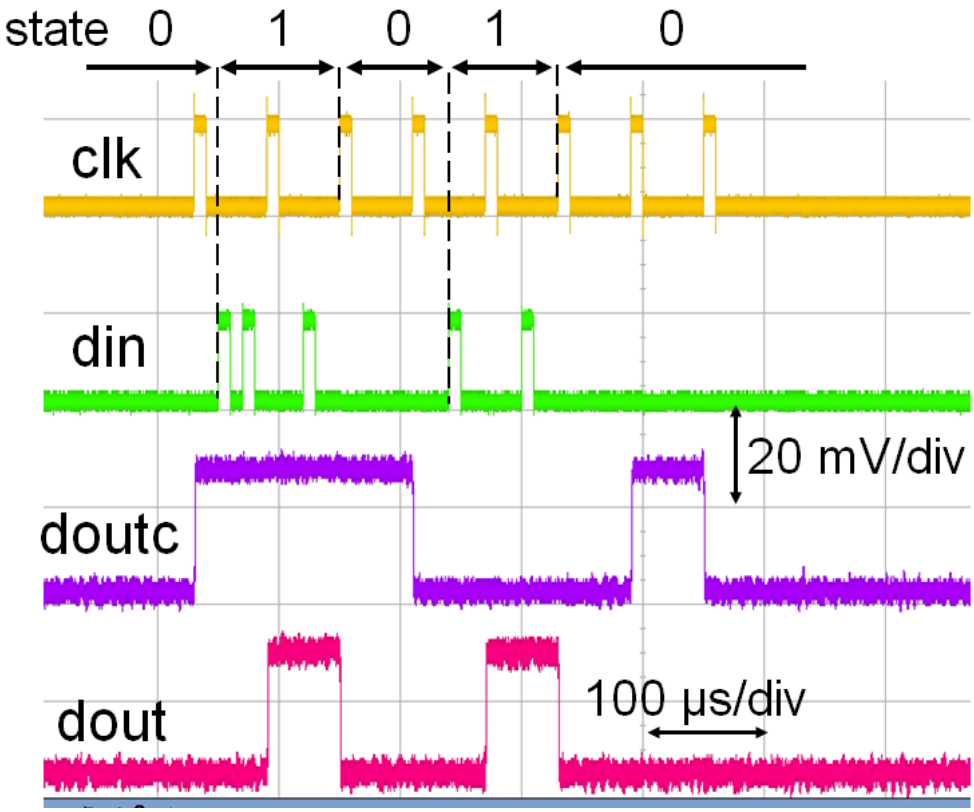


Figure 8: Low-speed test waveform of the DFFC with LFB. The two waveforms at the bottom (dout and doutc) are outputs from SFQ/DC converters with a T flip-flop [4]. The voltage transitions represent SFQ signal outputs. Output '1', which corresponds to the voltage transition at "dout" is synchronized with the clock (clk) input when the internal state is '1'. All waveforms are at the same scale (20 mV/div).

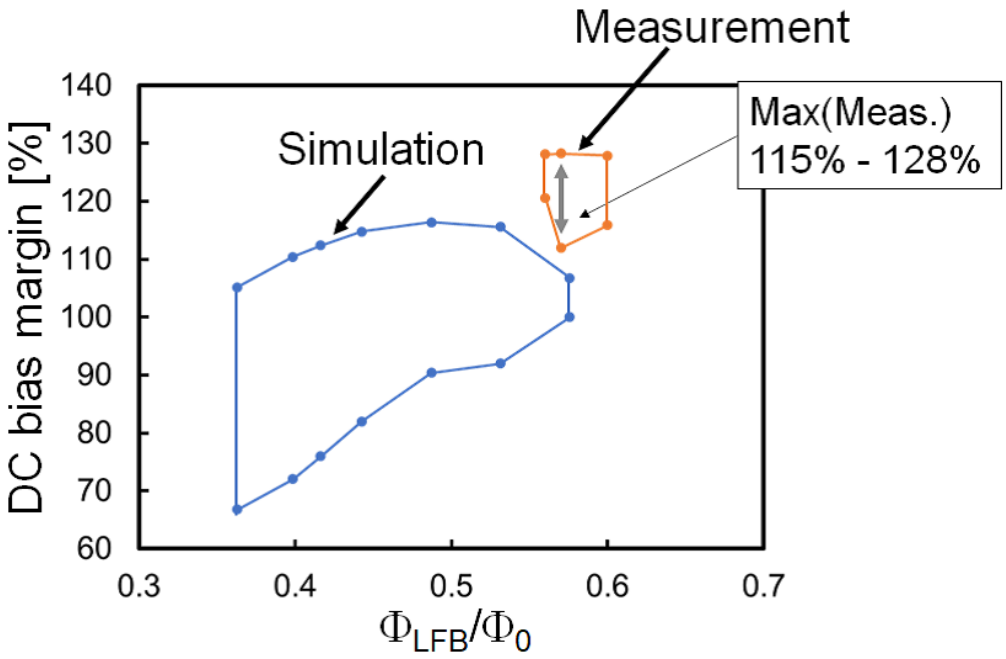
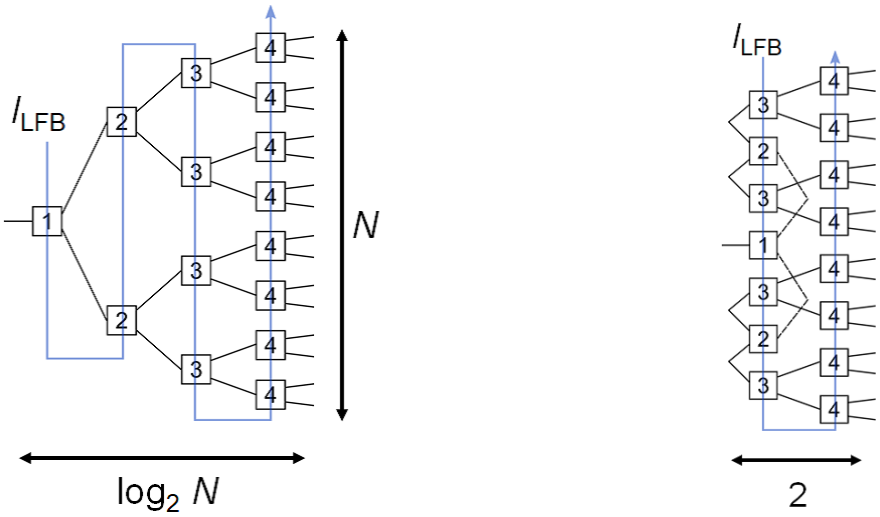


Figure 9: Measured and simulated bias margins for the DFFC (2.5 kA/cm^2) illustrated in Fig. 7 as a function of the applied magnetic flux Φ_{LFB}. The bias margin is normalized by the designed bias voltage of 2.5 mV.



(a) (b)

Figure 10: (a): Layout plan of the N-output decoder along with the NDROC/DFFC with LFB. Squares correspond to the NDROC/DFFC. (b): Layout plan of the compact decoder with folded design [33] and LFB. Here $N = 4$ is taken as an example.