# Compact Superconducting Lookup Table Composed of Two-Dimensional Memory Cell Array Reconfigured by External DC Control Currents

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***Abstract*—We investigated the hardware implementation of an area-efficient superconducting lookup table (LUT) based on a single flux quantum (SFQ) logic by using a newly proposed small memory cell. The memory cell is composed of a nondestructive read-out (NDRO) flip-flop with input circuits that convert the input dc current to an SFQ pulse signal. The datum can be written to the selected memory cell in the 2-D memory cell array by applying both *x*- and *y*-directional dc control currents. The data stored in the memory cell array can be reset simultaneously by applying a dc current to a common reset line. By employing the new memory cell, wiring for reconfiguring the data and resetting the memory cell array can be drastically simplified compared to that of the conventional SFQ LUT. We implemented and tested the memory cell and confirmed the correct operation with wide dc bias and input-current margins. We designed the 16-b LUT using the designed memory cells. The circuit area and the number of Josephson junctions of the 16-b LUT is reduced by approximately 24 and 41%, respectively, compared to those of the LUT based on the conventional architecture. We experimentally obtained the correct operation and reconfiguration of the 4-b LUT that uses the new memory cells with a normalized bias margin of –22 to +7%.**

***Index Terms*—Cryogenic memory, lookup table (LUT), memory cell, single flux quantum (SFQ) circuit.**

## I. Introduction

JOSEPHSON junction [1] (JJ) based superconducting circuits [2], [3] are attracting attention as an alternative technology to semiconductor integrated circuits because of its high-speed operation and superior energy efficiency [4], [5]. To date, the operation of large-scale superconducting digital circuits has been applied as information processing circuits [6]–[8]. Recently, superconducting field-programmable gate arrays (FPGAs) have been proposed as a flexible superconducting integrated circuit technology [9], [11]–[14]. A typical FPGA is composed of a logic block that has a lookup table (LUT), the logic function of which can be reconfigured, and a switch matrix that connects logic blocks [15]. In the previously implemented single flux quantum (SFQ) FPGAs, the LUT occupied a large circuit area of the SFQ FPGA [9]–[14]. The circuit area of the LUT composed of 2-input logic blocks implemented by 3-$\mu$m Nb process was 16 mm $^2$ [9]. One reason for a large LUT circuit area is the large memory cell circuit area. Because the typical cell size of the SFQ memory is several tens $\mu$ m square [16]–[20], the memory cell array occupies a large portion of the LUT circuit area. The other reason is that a complicated and dense wiring is needed to reconfigure the internal states of the memory cell array in the LUT for inputting SFQ signals to the memory cell. In the SFQ circuit, the wiring cost is high because the Josephson transmission line (JTL) or the passive transmission line (PTL) wiring [21] is needed. Because the typical width of the PTL for the latest superconducting circuit fabrication process is approximately 4 $\mu$m [22], [23], the wiring circuit occupies a significant portion of the circuit area. Moreover, the use of a PTL receiver is required for each memory cell in the case of PTL wiring.

In this article, we investigate an SFQ LUT architecture by employing a new compact memory cell, the internal state of which can be reconfigured and reset by applying dc control currents from the room-temperature instruments. In addition to the use of the compact memory cells, because the internal control wiring by JTL and PTL can be removed, the circuit area for LUT implementation can be significantly reduced. The internal state of all memory cells in the LUT can be reset simultaneously by applying a dc current to the common reset current line in the memory cell array. We report the design and test results of the new compact memory cell and the LUT composed of the memory cells. Additionally, we will compare the hardware cost of the LUT that employs the new memory cells with that of the conventional SFQ LUT.

## II. Compact SFQ LUT Architecture

Fig. 1 shows a conceptual diagram of the new memory cell and the $n \times n$ LUT architecture proposed in this study. The nondestructive memory cell is magnetically coupled to dc control lines $I_x$, $I_y$, and $I_{\rm reset}$ as shown in Fig. 1(a). Only when both $I_x$ and $I_y$ dc currents are activated, the datum "1" is input to the memory cell. The internal state of the memory cell is reset to "0" by applying the $I_{\rm reset}$ dc current. The detailed circuit structure and operational principle of the memory cell

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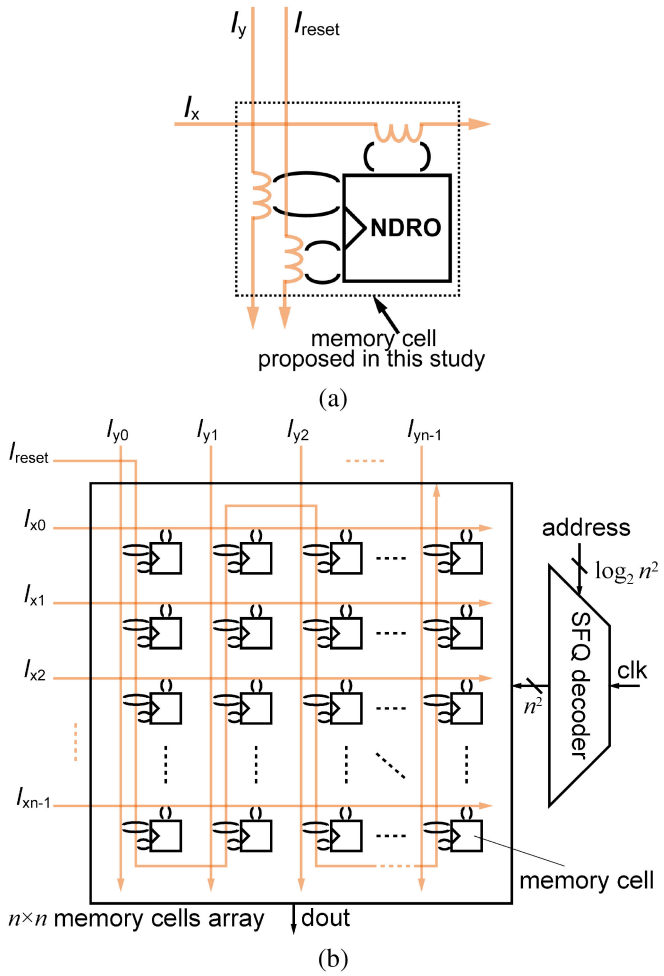


Fig. 1. (a) Memory cell proposed in this article and (b) architecture of the $n \times n$-bit LUT composed of memory cells in this study. DC control current lines of $I_x$, $I_y$, and $I_{reset}$ are magnetically coupled to conventional nondestructive read-out (NDRO) memory cells. LUT in which memory data can be written and reset by applying an external magnetic flux. Arrows of $I_{x0}$–$I_{xn-1}$, $I_{y0}$–$I_{yn-1}$, and $I_{reset}$ are dc control currents. The selected memory cell in the two-dimensional memory cell array can have the data written to it by applying both the $x$- and $y$-directional dc currents. By applying dc current to reset, we can initialize the data stored in the memory cells. By reconfiguring memory data using dc current, PTL or JTL wiring of data-writing and data-reset can be reduced more than the conventional SFQ LUT.

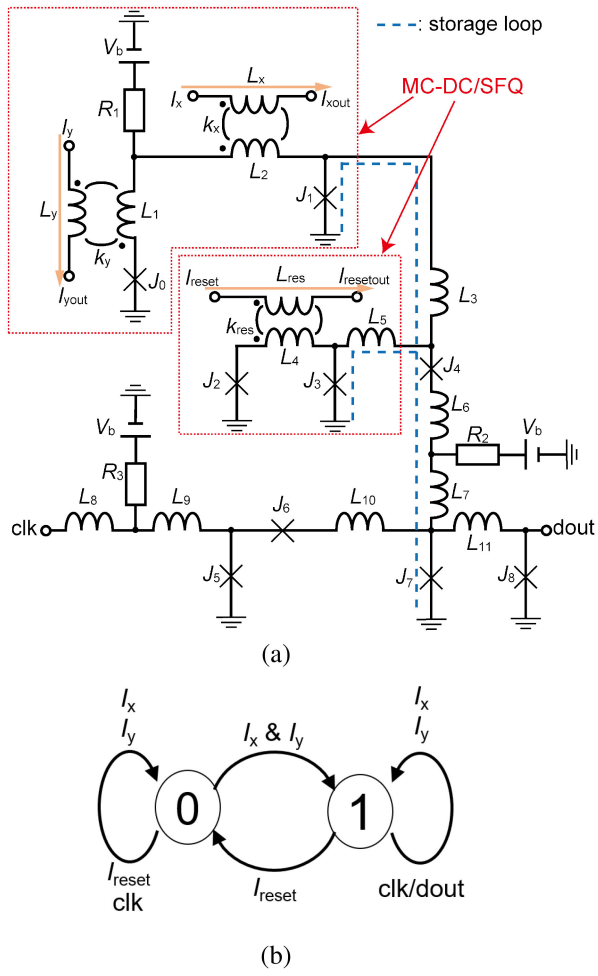


Fig. 2. (a) Equivalent circuit and (b) state transition diagram of the memory cell proposed in this article. "$I_x$," "$I_y$," and "$I_{reset}$" are dc control currents. "clk" and "dout" correspond to clock input and data output ports, respectively. Parameters in (a) are as follows: $L_x = 16.69$ pH, $L_y = 11.63$ pH, $L_{res} = 14.63$ pH, $L_1 = 3.68$ pH, $L_2 = 3.68$ pH, $L_3 = 4.21$ pH, $L_4 = 3.71$ pH, $L_5 = 2.79$ pH, $L_6 = 0.66$ pH, $L_7 = 0.87$ pH, $L_8 = 1.25$ pH, $L_9 = 1.43$ pH, $L_{10} = 2.89$ pH, $L_{11} = 5.33$ pH, $J_0 = 164$ $\mu$A, $J_1 = 178$ $\mu$A, $J_2 = 203$ $\mu$A, $J_3 = 202$ $\mu$A, $J_4 = 122$ $\mu$A, $J_5 = 216$ $\mu$A, $J_6 = 174$ $\mu$A, $J_7 = 176$ $\mu$A, $J_8 = 215$ $\mu$A, $R_1 = 13.82$ $\Omega$, $R_2 = 21.19$ $\Omega$, $R_3 = 8.34$ $\Omega$, $k_x = 0.19$, $k_y = 0.081$, and $k_{reset} = 0.10$. The McCumber parameters $\beta_c$ of JJs in this memory cell are all 0.89, which is the same as that of cells in the CONNECT cell library [26]. The bias voltage $V_b$ is 2.5 mV.

will be provided later. The LUT is composed of a memory cell array where the memory cells are two-dimensionally aligned and an SFQ decoder that selects the read-out memory cell as shown in Fig. 1(b). All dc control currents are supplied from the room-temperature instruments. The $x$- and $y$-directional control current lines are shared by all memory cells in the same row and column. The memory cell is selected and the datum "1" is written to the selected cell by applying the $x$- and $y$-directional control current simultaneously. The internal state of all the memory cells can be simultaneously reset by applying reset current to the reset line shared by all the memory cells. In this LUT architecture, the internal states of $n^2$ memory cells are reconfigured by $2n$ dc control current lines and one reset line. The number of the address lines input to the decoder to select the memory cell is $\log_2 n^2$. Because the internal wiring, which needs JTLs/PTLs for data reconfiguration and reset is not required, a dense integration of the memory cell array is realized compared to the conventional SFQ LUT [12]. Though the reconfiguration of the proposed LUT is slow, it is suitable for the FPGA LUT, which generally does not need dynamic reconfiguration during its operation. Note that the high-frequency read-out operation of the LUT at the frequency of several tens GHz is possible because the memory cell is read out by applying the SFQ signal to the memory cell selected by the SFQ decoder.

Fig. 2 shows the detailed equivalent circuit of the memory cell proposed in this study and its state transition diagram. This memory cell is composed of a simplified nondestructive read-out (NDRO) flip-flop with magnetically coupled dc/SFQ converters (MC-dc/SFQs) [24], [25] that convert the dc current input to the

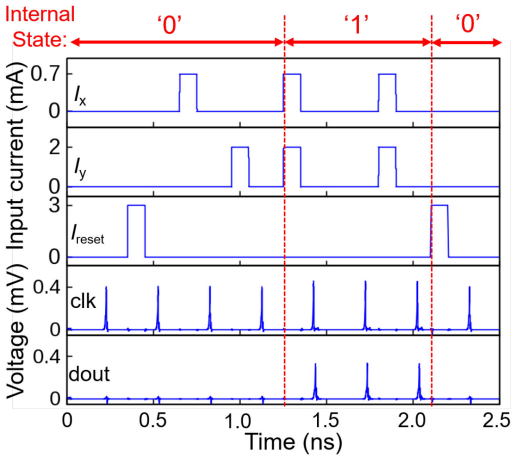


Fig. 3. Simulated memory cell waveforms.

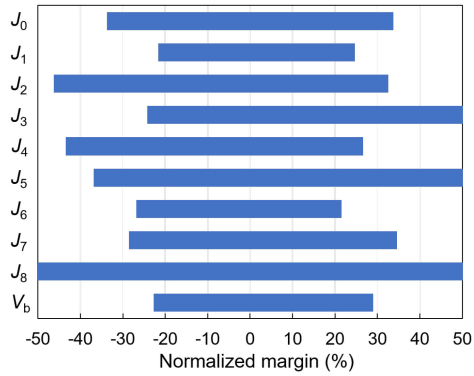


Fig. 4. Normalized margin of JJ critical currents and bias voltage in the designed memory cell.

SFQ pulse. The superconducting loop is composed of $J_1 - L_3 - J_4 - L_6 - L_7 - J_7$, and $J_3 - L_5 - J_4 - L_6 - L_7 - J_7$ is the storage loop, which stores one flux quantum when the internal state of the memory cell is "1." By tuning the magnetic coupling strength between the dc current lines and MC-dc/SFQs, the SFQ pulse for datum writing is input when both $I_x$ and $I_y$ are applied. When the internal state is "1" and the $I_{reset}$ is applied, the SFQ pulse input to the storage loop switches the escape junction $J_4$, the magnetic flux quantum in the storage loop escapes, and the internal state of the memory cell resets to the "0" state.

We optimized the circuit parameters of the memory cell using the JSIM analog circuit simulator [27] and the SCOPE circuit parameter optimization tool [28] to obtain wider operating margins. Fig. 3 shows the simulated transient analysis result of the memory cell assuming use of the AIST 10 kA/cm$^2$ Nb high-speed standard process (AIST-HSTP) [29]. One can confirm that the internal state of the memory cell is reconfigured and reset by the dc currents with an amplitude in the mA range. Moreover, the NDRO operation can be confirmed. Fig. 4 shows optimized margins of JJ critical currents and the bias voltage of the designed memory cell. The parameter margin of the critical JJ is –27 to +23%. The simulated bias margin of the memory cell is –23 to +29%. The input current margins of the $I_x$ and $I_y$ are 0.43–0.97 and 1.33–1.71 mA, respectively. The memory

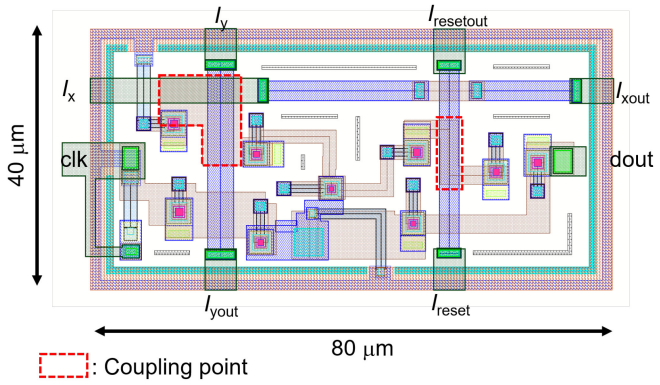


Fig. 5. Mask layout of the memory cell. Cell size is 80 $\mu$m × 40 $\mu$m. Magnetic coupling parts are represented by the dashed red square. Circuits are fabricated using AIST 10 kA/cm$^2$ Nb HSTP.

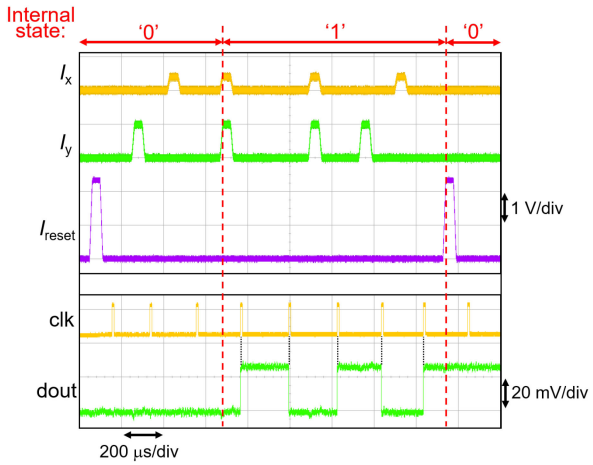


Fig. 6. Measured memory cell waveform at 4.2 K. The upper three waveforms are dc control currents. "clk" is the voltage input to the dc/SFQ converter. Therefore, the SFQ signal is input to the circuit at the "clk" voltage rise. "dout" is the output voltage of the SFQ/dc converter amplified by 100. Transition of the "dout" voltage corresponds to SFQ output.

cell can operate when $I_{reset}$ is larger than 2.25 mA. The reason for no upper margin limitation of the $I_{reset}$ is that the large $I_{reset}$ introduces multiple reset signal inputs to the storage loop, and successive high-speed reset inputs are canceled by the escape junction $J_4$.

## III. Circuit Implementation and Experiment

We designed and implemented the memory cell, described in the previous section, using the AIST-HSTP. Fig. 5 shows the memory cell mask layout. We used a three-dimensional inductance extraction tool InductEX [30] to extract the self-inductance and mutual inductance from the circuit layout. The designed memory cell size is 80 $\mu$m × 40 $\mu$m, which is the same as the NDRO cell in the CONNECT cell library [26]. We also designed the memory cell using the AIST 2.5 kA/cm$^2$ Nb standard process 2 (AIST-STP2) [31] on the same cell size.

We tested the memory cell implemented by the AIST HSTP. In measurements, test chips were cooled to 4.2 K in a liquid helium. Fig. 6 shows an example of the measured waveform.

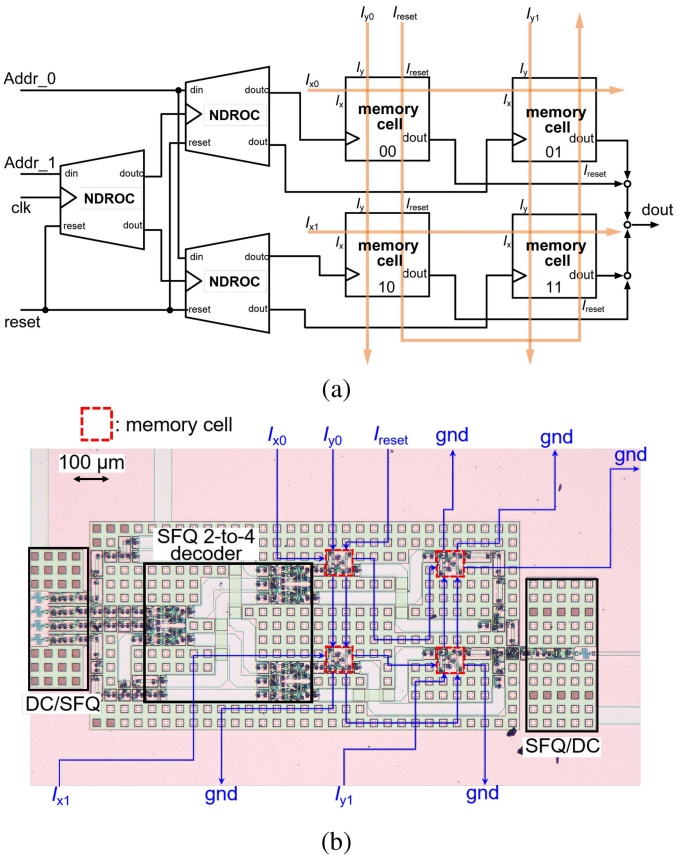


Fig. 7. (a) Block diagram and (b) microphotographs of the 4-b LUT. Red squares represent memory cell positions.

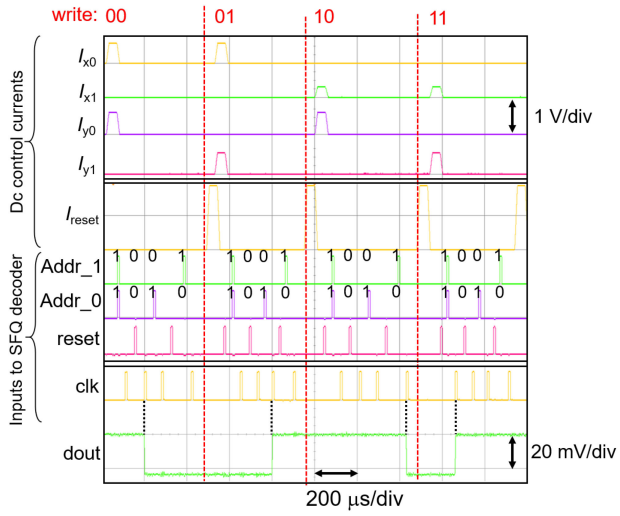


Fig. 8. Measured waveform of 4-b LUT at 4.2 K. Data were written to only one address in each sequence separated by red dotted lines.

The dc control current, $I_{\rm x}$, $I_{\rm y}$, and $I_{\rm reset}$, were applied by the application voltage generated by an arbitrary waveform generator triggered by a data generator to 1 kΩ room-temperature resistors. We confirmed the correct reconfiguration and resetting operation of the memory cell by the dc control currents. The measured bias margin of the memory cell was –29 to +7%. The measured dc current margins of $I_{\rm x}$ and $I_{\rm y}$ were 0.25–0.46 and 0.72–1.07 mA, respectively. The measured $I_{\rm reset}$ margin was 1.62–10 mA, which is limited by the maximum output voltage of the arbitrary waveform generator used in the measurement. The possible reason for the mismatch of dc control current margins between the simulation and measurement is a discrepancy of mutual inductance extracted from the layout.

We designed the 4-b LUT composed of four memory cells and an SFQ 2-to-4 decoder. Fig. 7 shows the block diagram and microphotograph of the 4-b LUT implemented by using the AIST-STP2. In this design, we used the 34-$\mu$m width PTL wiring [32] for read-out lines and merging the output from each memory cell. The SFQ 2-to-4 decoder is composed of a NDRO flip-flop with complimentary outputs (NDROC) tree [33], [34]. The Addr_1, Addr_0, and reset inputs determine the cell that is read out by the "clk" input. The dc control currents supplied to the LUT grounded at a location different from the circuit to avoid influences of the magnetic field generated by the dc currents. The quantity of JJs, designed bias current value, and circuit area of the 4-b LUT are 313, 38.14 mA, and 0.25 mm$^2$, respectively.

Fig. 8 shows the measured waveform of the 4-b LUT in the low speed test. In this test pattern, the datum "1" is written to the memory cell at addresses 00, 01, 10, and 11, in turn, by applying the corresponding dc currents. The outputs are correctly obtained from the corresponding address in each sequence separated by red dotted lines. The operating bias margins (normalized by designed value, 2.5 mV) of the memory cell was $-22\%$ to $+7\%$. The experimental operating current margins of $I_{\rm x0}$, $I_{\rm x1}$, $I_{\rm y0}$, $I_{\rm y1}$, and $I_{\rm reset}$ were 0.43–0.67, 0.18–0.36, 0.54–0.85, 0.61–0.85 mA, and greater than 1.86 mA, respectively.

## IV. Discussion

To quantitatively evaluate the effect of introducing the new memory cell into the LUT, we compared the hardware cost of the new LUT and that of the conventional LUT assuming use of the AIST-STP2. We compared the circuit area and the number of JJs. Fig. 9 summarizes the comparison. The number of JJs to implement the 16-b LUT can be reduced by 41% by employing the new memory cell compared to that of the conventional LUT design. The reduction ratio of the hardware cost of the new LUT compared to the conventional LUT is larger as the LUT size increases. This means the scalability of the new LUT employing the new memory cell is superior. The LUT can also be utilized as a reconfigurable combinational logic circuit that has an arbitrary logic function.

Although the 2-D memory cell array has scalability, one drawback of the LUT using the new memory cell is the number of cables required to connect the low-temperature and room-temperature stages. The number of required row and column dc control lines to reconfigure $n \times n$-bit LUT memory cell array is $2n$. This number is not negligible for implementation of a large-scale LUT. One possible solution is the introduction of the complementary metal oxide semiconductor (CMOS) decoder. By decoding the binary address signal input from the room temperature stage using the CMOS decoder, which can output the dc current to reconfigure the memory cell array located at

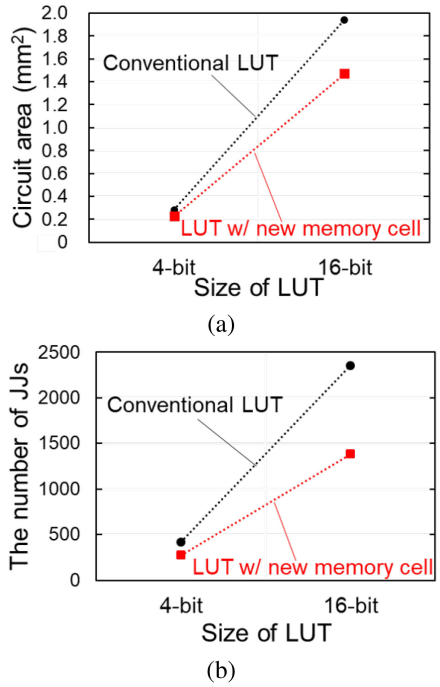


Fig. 9. Comparison of (a) circuit area and (b) number of JJs of the new LUT and those of the conventional LUT [12].

the low-temperature stage, the number of cables that connect the low-temperature and room-temperature stages can be reduced. Because once the memory cell array in the LUT is reconfigured, the bias voltage supplied to the CMOS circuit can be turned off and, therefore, using the CMOS circuit does not increase the power consumption of the LUT system during its operation. The SFQ/CMOS hybrid LUT system can be built using conventional circuit technologies [35]–[37].

## V. Conclusion

We investigated the compact and scalable SFQ LUT based on the new memory cell, the datum of which is written by applying dc control currents. The use of the new memory cell can remove the complicated wiring in the memory cell array for reconfiguring and resetting the LUT. We designed and experimentally confirmed the operation of the memory cells and the 4-b LUT with wide operating margins. We found that the area of the 16-b LUT that employs the new memory cell is smaller than that of the conventional 16-b LUT by approximately 25%. The area reduction ratio is estimated to be larger with an increase in the LUT bit-capacity. These results indicate the effectiveness of introducing the memory cell proposed in this study into the large-scale SFQ LUT.

## Acknowledgment

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