Design and Evaluation of 2-bit-input Single-flux-quantum Autocorrelator System for Astronomical Data Analysis

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***Abstract*— To improve the accuracy of astronomical data analysis, an increase in the number of output bits from the A/D converter is effective. We investigated a single-flux-quantum (SFQ) autocorrelator and an integrator that supports multiple-bit signal output from an SFQ A/D converter for astronomical data processing. The SFQ binary counter was used as the integrator that decimates the output from the SFQ autocorrelator for communication with equipment at room temperature. We designed the test circuits composed of 2-bit inputs, an autocorrelator, and an integrator that contains 5631 Josephson junctions using the 10 kA/cm^2 Nb process. We confirmed the correct operation of the test circuit with a normalized bias voltage margin of 102%–114% by the low-speed test. We obtained its correct high-speed operation up to a 55.1 GHz clock frequency. In terms of circuit design, scaling up the test circuit is easy. These results indicate the effectiveness of a high-precision and large-bandwidth radio astronomical observation using SFQ circuit technology.**

***Index Terms*— single-flux quantum, autocorrelator, superconducting integrated circuits**

I. Introduction

SINCE the discovery of cosmic radio waves [1], radio astronomy has played an important role in the development of astronomy. Millimeter- and submillimeter-wave observations have various excellent features that are not found in optical astronomical telescopes, which focus visible light to observe objects. The interstellar gas is extremely thin and contains a small number of molecules called interstellar molecules. Since the interstellar molecules cannot be observed in the visible light, they are observed by radio waves. An interference technique is easy to use for radio waves, so that they can be interfered with by a large number of distant antennas. Extremely high resolution can be achieved by adopting multi-receiver observation, called multi-beam. Because the noise temperature of the superconductor-insulator-superconductor (SIS) mixer approaches the quantum limit [2], the SIS heterodyne receivers have been used in the field of radio astronomy to observe spectra with the lowest noise temperature in millimeter-wave and submillimeter-wave wave observations [3, 4]. In 2000, a multi-beam receiver (25 Beam Array Receiver System: BEARS), which was constructed with 25 SIS mixers, was developed in the 100-GHz band and installed in the 45-m telescope in the Nobeyama Radio Observatory [5].

The typical low-noise amplifier for the SIS mixer consumes approximately 10-20 mW [6,7]. Furthermore, an amplifier with a power consumption of about 1.2 mW has been developed [8]. The number of SIS mixers integrated in one refrigerator is limited by the power consumption of the amplifiers and the cooling capacity of the refrigerator. To solve this problem, a digital autocorrelation system, where the SIS mixers, A/D converters, and autocorrelators based on the single-flux-quantum (SFQ) circuit technology [9, 10] are integrated in the refrigerator, was proposed [11]. Fig. 1 shows a prototype of the spectroscopic system based on the SFQ circuit that we are studying. Because the high-sampling-rate A/D converters and high-speed data processing circuits can be implemented using the high-sensitivity and high-speed characteristics of SFQ circuits, this approach is thought to be promising for increasing the number of SIS mixers of the multi-beam receiver system. The SFQ autocorrelator was implemented and its operation at 20.48 GHz was demonstrated [12].

To improve the accuracy of the data analysis in the radio astronomy, increment in the quantized levels of the A/D converter outputs is promising. The number of typical bits used in the A/D conversion of the current radio telescope is 2–3 bits [13]. In this study, we investigated a multiple-bit autocorrelator system based on an SFQ circuit. We designed and implemented an SFQ autocorrelator that can process the 2-bit digital signal

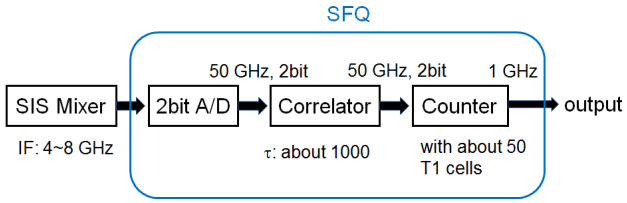

Fig. 1 The spectroscopic system we proposed. The 2-bit SFQ A/D converter digitizes the output of the SIS mixer. The number of time lags of the correlator is about 1000. The calculation results are read out at about 1 GHz.

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TABLE I
2-BIT AUTOCORRELATION FUNCTION

c_1c_0		y_1y_0			
		00	01	10	11
x_1x_0	00	11	10	01	00
	01	10	11	10	01
	10	01	10	11	10
	11	00	01	10	11

outputs from the SFQ A/D converter. We describe the detailed design and high-speed test results of the designed circuits. We tested the SFQ 2-bit autocorrelator at a high-speed test and confirmed some correct operations.

II. AUTOCORRELATOR DESIGN

By analyzing the spectrum of the radio waves emitted from the celestial body, we can obtain information about the target object. A radio spectrometer is a device that converts the input signal to the frequency-domain signal. The Wiener–Khinchine theorem [14] is used to obtain the spectrum of the radio wave. An autocorrelation function, which corresponds to similarity of two waveforms distant from time lag τ, is represented as

$$C(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} V(t)V(t+\tau)\, dt, \quad (1)$$

where T is the periodicity of the input wave and $V(t)$ is the voltage at time t of the input wave. The power spectrum is represented as:

$$P(f) = \frac{1}{2\pi} \int_{-\infty}^{\infty} C(\tau) e^{-j2\pi f\tau} d\tau\,, \quad (2)$$

where f is the frequency.

For digital signals, which deal with discrete time signals, the autocorrelation function and the power spectrum are represented as

$$C(\tau) = \frac{1}{N+1} \sum_{t=0}^{N} V(t)V(t+\tau) \quad (3)$$

where N is the sampling points of periodic signal. The power spectrum is represented as:

$$P(f) = \sum_{\tau=-\infty}^{\infty} C(\tau) e^{-j2\pi f\tau}\,. \quad (4)$$

An autocorrelator is used to calculate the autocorrelation function in (3). The autocorrelator can be designed using 3 circuit components, a shift register that adds a delay to the input wave and outputs $V(t+\tau)$, a correlator that calculates correlation $V(t)V(t+\tau)$, and a binary counter used as an integrator that decimates the output autocorrelation function for communication with equipment at room temperature.

The autocorrelation is calculated using the exclusive-OR gates because the hardware cost of exclusive-OR gates is low in the case of SFQ circuits. The SFQ autocorrelator is implemented by a simple circuit structure [15]. We designed component circuits of the autocorrelator, shift register, correlator, and binary counter of the autocorrelator. All circuit components were designed using the National Institute of Advanced Industrial Science and Technology 10 kA/cm^2 Nb advanced process 2 (ADP2) [16] and the cell library for the ADP2 [17, 18].

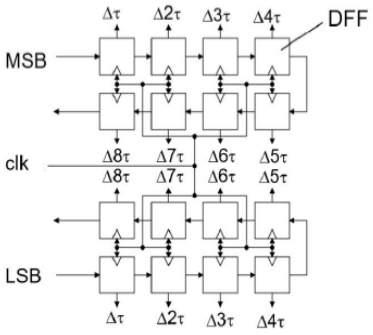

Fig. 2 Block diagram of the shift register for autocorrelator. Clock pulses reach all 16 DFFs simultaneously. Δτ is minimum time lag of the autocorrelator.

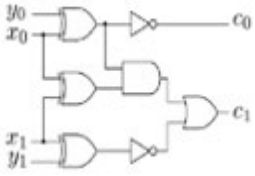

Fig. 3 Block diagram of the 2-bit-input correlator. It can calculate correlation function between two 2-bit digital data inputs. x_0 and y_0 are LSB outputs, and x_1 and y_1 are MSB outputs from shift register in Fig. 2.

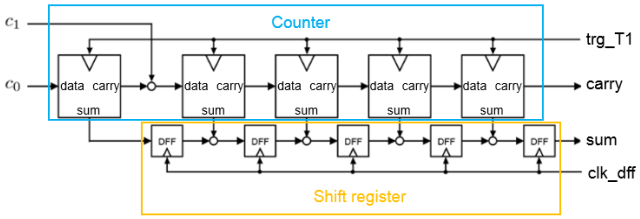

Fig. 4 Block diagram of the binary counter that supports 2-bit input. Squares in the counter are T1 flip-flops.

Fig. 2 shows the block diagram of the 4-channel 2-bit-input shift register for the autocorrelator. The 2-bit-input shift register comprises 16 delay flip-flops (DFFs) in this design. To enhance the throughput and the operating margin, we employed zero-skew clocking, where the clock is input to all DFFs simultaneously instead of employing both concurrent and counter-flow clocking [12]. Time lag τ of 1, 3, 5, and 7 clocks can be produced by this circuit. The number of Josephson junctions in the 2-bit shift register is 263. The bias margin normalized by 2.5 mV is 80%–125% at the target clock frequency of 50 GHz using the Verilog digital circuit simulation.

We designed a 2-bit-input correlator. In this design, the analog signal is assumed to be converted to quantization levels (2-bit). Table 1 shows the input-output characteristics of the 2-bit correlator. x_1x_0 and y_1y_0 are 2-bit digital input signals that are quantized as $V(t)$ and $V(t+\tau)$, respectively. c_1c_0 is the 2-bit output of the autocorrelator. Autocorrelation denotes similarity of two inputs. When the two 2-bit inputs are the same, the highest correlation, (c_1c_0) = 11 in this case, is output. When the

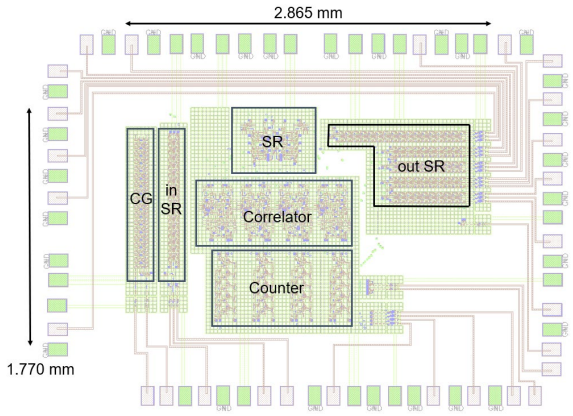

Fig. 5 The chip layout of 4-channel 2-bit autocorrelator. CG, in SR, and out SR represent the 12-bit clock generator, the 10-bit shift register for data input, and the and 10-bit shift register for output data monitoring, respectively.

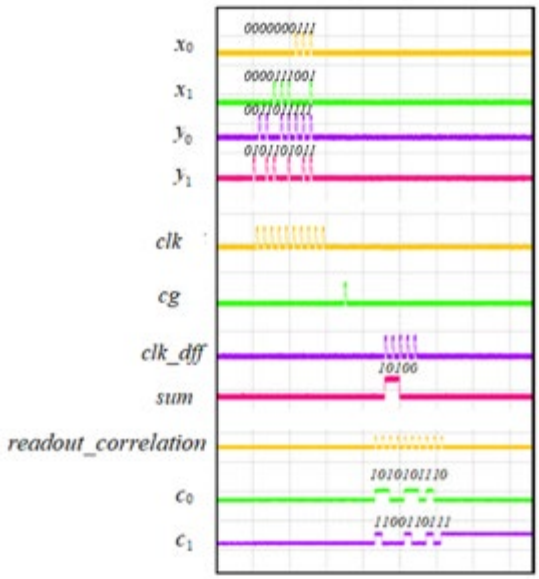

Fig. 6 The results for the circuit consisting of the 2-bit-input correlator and the 2-bit input binary counter. The "cg" signal is a trigger signal to generate a high-speed clock. c_0 and c_1 are the correlation function output from the 2-bit-input correlator. A signal "sum" is the integral of the correlation function $c_1c_0 = 11 + 10 + 01 + 00 + 11 + 10 + 01 + 11 + 11 + 10 = 10100$.

2-bit inputs are 11 and 00, the lowest correlation, $(c_1c_0) = 00$, is output. When the difference between two 2-bit inputs is 01 (1 quantized level) and 10 (2 quantized level), $(c_1c_0) = 01$ and $(c_1c_0) = 10$ is output respectively.

Based on the logic synthesis results shown in Table 1, we designed the 2-bit correlator. Fig. 3 shows the block of the 2-bit-input correlator. We employed concurrent flow clocking because of the data flow in one dimension. The number of Josephson junctions of the 2-bit-input correlator is 240. The digital circuit simulation shows that the bias margin of the correlator is 80%–125% at 50 GHz. We can design a 3- bit-input autocorrelator using the same method, although the number of logic gates, which are mainly exclusive-OR gates, increases.

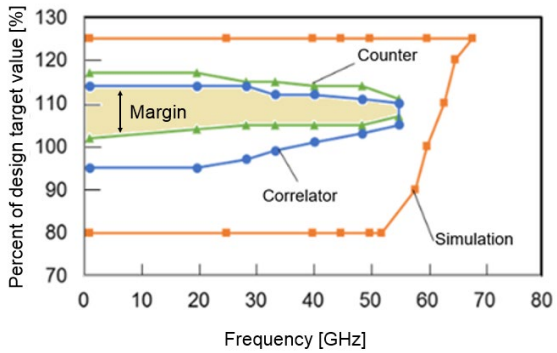

Fig. 7 The measured dependence of the measured bias voltage margin on the input frequency. The filled region corresponds to the bias margin of the system.

A standard binary counter, composed of T1 flip-flops connected in series, is used as an integrator. Fig. 4 shows the block diagram of the binary counter that supports 2-bit input. The binary counter is composed of five DFF and five T1 cells. The least-significant-bit (LSB) output from the autocorrelator c_0 is input to the first-stage T1 cell. The carry signal from the first stage T1 cell and the most-significant-bit (MSB) of the autocorrelator output (c_1) merge with the confluence buffer. By inputting the trigger signal for the T1-based counter (trg_T1 in Fig. 4), the integrated autocorrelation is output to the shift register composed of serially connected delay flip-flops (DFFs). The stored result in the shift register is read out serially from the MSB by inputting read-out clock (clk_DFF in Fig. 4). The number of Josephson junctions of the 2-bit correlator is 169. The digital circuit simulation shows that the bias margin of the counter is 80%–125% at a data input frequency of 50 GHz.

These circuits have good scalability. The number of bits can be increased by increasing the number of flip-flops used in the circuit design.

III. Experimental Result

We designed a 4-channel 2-bit-input autocorrelator system by combining all circuit component circuits described in the previous section. Fig. 5 shows the layout of a 4-channel 2-bit-input autocorrelator system including input/output circuitry for an on-chip high-speed test. The number of Josephson junctions of 4-channel 2-bit autocorrelators, including test circuits for the high-speed test, is 5631. The power consumption was 1.7 mW. The bias margin normalized by the designed bias voltage of 2.5 mV is 80%–125% at 50 GHz obtained using the simulation.

We tested the implemented circuit at 4.2 K in a liquid helium bath. Fig. 6 shows the measured waveforms obtained from the on-chip high-speed test [17]. In this sequence, the test circuit calculates the correlation function of 10 pairs of two 2-bit inputs and then integrates them. The output of the circuit, sum, is output synchronized by the readout clk_dff inputs. The correct integrated autocorrelation function was obtained.

Fig. 7 shows the dependence of the measured bias voltage margin on the input frequency. The difference between measured and simulated margins might be caused by discrepancy of circuit parameters between designed and fabricated devices. We confirmed its correct operation with a normalized bias voltage margin of 102%–114% using the low speed test, and we could obtain its high-speed operation up to 55.1 GHz clock frequency.

IV. Conclusion

We designed and evaluated the performance of an SFQ autocorrelator that supports multi-bit signal inputs for astronomical data analysis. We designed the test circuits of the SFQ autocorrelator system, which contains 5631 Josephson junctions. We confirmed the correct operation of the component circuits of the SFQ autocorrelator, the correlator, and the counter from the low-speed test, and we could obtain its correct operation up to 55.1 GHz clock frequency.

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