Simulation of the Margins in Single Flux Quantum Circuits Containing π-Shifted Josephson Junctions

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***Abstract*—We designed several single flux quantum (SFQ) flip-flops and logic gates composed of Josephson junctions (JJs) and π-shifted JJs (π-JJs) to quantitatively evaluate effectiveness of introduction of π-JJs into the SFQ logic circuit. One-output flip-flops and logic gates were designed on the basis of the circuit design methodology we built for the SFQ circuit containing π-JJs. The designed flip-flops and logic gates have wide operating margins, the dc bias margins of larger than ±30% and device parameter margins of ±18%, though the static power consumption are reduced compared to conventional ones composed of JJs. We found that the difference in the critical current density between JJs and π-JJs does not affect the operating margins of the SFQ flip-flop composed of JJs and π-JJs. We devised a circuit structure of the delay flip-flop with complementary outputs composed of JJs and π-JJs (π-DFFC). The analog circuit simulation shows the dc-bias margin of the π-DFFC is larger than ±33%. These results indicate that the large-scale SFQ logic circuit system can be implemented using the flip-flops and logic gates containing π-JJs.**

***Index Terms*— Single-flux-quantum (SFQ) circuit, π-shifted Josephson junction, flip-flop**

I. Introduction

ENERGY Consumption for Information and Communication Technology (ICT) has drastically increased for decades. Total energy consumption for ICT devices in the world has already reached 1 PWh/year in 2017, which is larger than annual energy consumption in Japan, and is estimated to keep increasing in the future [1]. However, semiconductor integrated circuit technology, which has been supporting the ICT development, is facing several obstacles [2]. Among the obstacles, power consumption is the most serious problem of the semiconductor complementary metal-oxide-semiconductor (CMOS) integrated circuit. In this sort of situation, beyond-CMOS devices that can overcome limitation of CMOS devices, have been studied [3]. Among various beyond-CMOS devices, superconducting digital devices, including single-flux-quantum (SFQ) devices [4,5] and its improved versions have a high-speed operation characteristic with ultra-high energy efficiency [6, 7] are regarded as one of practical candidates that can supplement CMOS devices.

Introduction of an intrinsic π-phase shifter, which shifts the phase of the macroscopic wave function in the superconductor by π across the device, into superconducting integrated circuits has been investigated to improve the circuit performance. The first concept of the superconducting integrated circuit using the π-phase shifter was proposed by Terzioglu and Beasley [8]. Introduction of the π-Josephson junction (π-JJ), the phase-current relation of which is shifted by the phase of π compared to conventional Josephson junction (JJ), into the SFQ circuits was proposed by Ustinov and Kaplunenko [9]. The inductance in an SFQ circuit can be reduced by using the intrinsic phase shift of the π-JJs [9, 10]. Because the dc bias current, injected to the SFQ circuits to build logic gates, can be removed by combining both JJs and π-JJs, static power consumption of the SFQ circuit can be reduced [11]. The operating stability of the SFQ circuits also can be improved by introducing π-JJs [12, 13]. Reduction in dynamic power consumption has been studied by replacing the JJs in the SFQ circuit into dc-SQUIDs composed of the JJ and the π-JJ [8, 14].

So far, design and demonstration of SFQ circuits composed of JJs and π-JJs have been mainly limited to the toggle flip-flops because of the ease of the design and implementation [10, 11, 13]. We have built the circuit design methodology that can be applied to designing any SFQ flip-flops other than the toggle flip-flop [15]. In this study, we quantitatively evaluate the effectiveness of introduction of the π-JJs into SFQ circuits through the design of several fundamental SFQ flip-flops on the basis of the design methodology we built. The influence of difference in the critical current density between JJs and π-JJs on the operation of the SFQ flip-flops is discussed. We also devised the SFQ delay flip-flop that has complementally outputs using π-JJs.

II. Design of SFQ Flip-Flops Containing Π-JJs

We designed several fundamental SFQ flip-flops by modifying the corresponding flip-flop cells in the CONNECT cell library [16]. Therefore, all flip-flops we designed in this study can be directly connected to cells in the CONNECT cell library. We replaced the storage loop in the flip-flops by a storage loop composed of both JJs and π-JJs (π-storage loop) and removed the bias current injection to the π-storage loop [15]. We performed transient analysis of the designed flip-flops using the analog circuit simulator PJSIM [15] assuming the criti-

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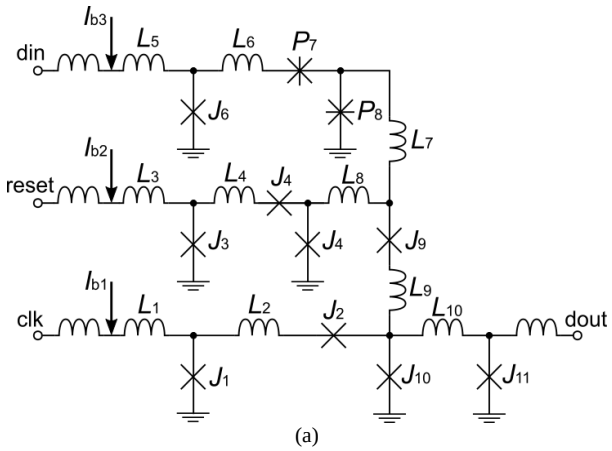

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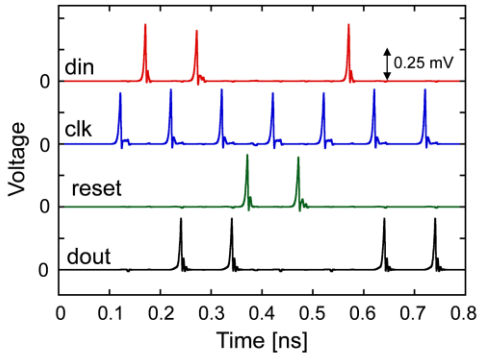


(b)

Fig. 1. (a) The equivalent circuit and (b) an example of the transient analysis of the π-NDRO. The circuit symbols used to express P_7 and P_8 correspond to p-JJs in this paper. The critical current values of JJs and π-JJs are as follows: J_1 = 210 μA, J_2 = 265 μA, J_3 = 218 μA, J_4 = 235 μA, J_5 = 135 μA, J_6 = 217 μA, P_7 = 230 μA, P_8 = 160 μA, J_9 = 145 μA, J_{10} = 130 μA, and J_{11} = 203 μA. L_1 = L_3 = L_5 = 2.457 pH, L_2 = 1.000 pH, L_4 = L_6 = 2.500 pH, L_7 = 4.000 pH, L_8 = 3.000 pH, L_9 = 0.500 pH, L_{10} = 5.486 pH, and I_{b1} = I_{b2} = I_{b3} = 300 μA.

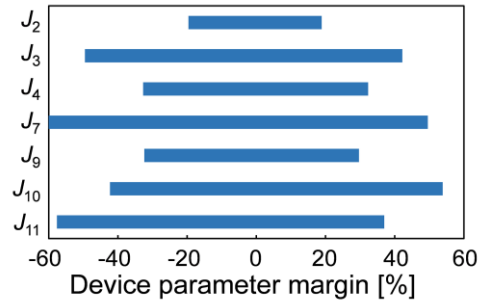


Fig. 2. Device parameter margins of each circuit element of π-NDRO.

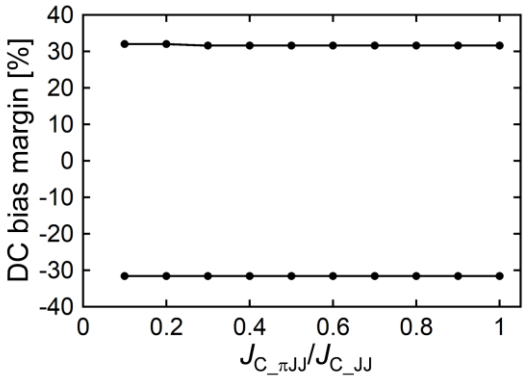


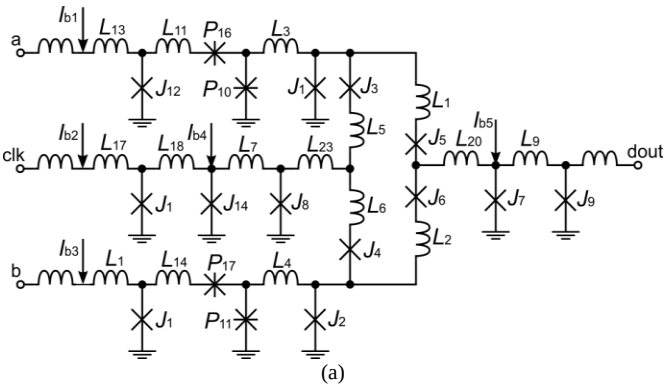
Fig. 3. Dependence of simulated dc bias margin of the π-NDRO on the ratio of critical current density of JJs and π-JJs.

cal current density (J_C) of both JJs and π-JJs are 2.5 kA/cm^2, which is the same J_C as that of the AIST Nb standard process 2 (AIST-STP2) [17, 18].

Fig. 1 shows the equivalent circuit of the non-destructive readout flip-flop containing π-JJs (π-NDRO) and the waveform obtained by the transient analysis simulation by PJSIM. Parasitic inductances of 0.2 pH between all JJs/π-JJs and the ground are considered in the simulation though they are not shown in Fig. 1 (a). The loop composed of P_8, L_7, L_8, and J_4 is the main π-storage loop. We implemented a simple device parameter margin extraction tool and roughly optimized the circuit parameters by repeating the critical margin method [19] three times. Extracted device parameters after the rough optimization are shown in the caption of Fig. 1. As shown in Fig. 1 (b), output SFQ signals (dout) are obtained synchronized by the clock (clk) inputs after data signal (din) input until the reset signal is input. Non-destructive operation is also confirmed by monitoring fourth 'dout' pulse. The simulated dc-bias margin of the π-NDRO at the clock frequency of 10 GHz is ±31.6%.

Because the bias current injected to the π-storage-loop can be removed, the static power of the π-NDRO dissipated by the on-chip bias resistors is reduced. The static power consumption of the π-NDRO is 2.25 μW at the designed bias voltage (2.5 mV). This static power consumption is reduced by 19.1% compared to the conventional NDRO cell composed of JJs. Fig. 2 lists the extracted parameter margin of the circuit devices that have parameter margins of less than ±50%. The critical circuit device is J_2 and the parameter margin is -19.6% to 18.9%. It should be noted that the π-JJs P_7 and P_8 have the wide device parameter margins of more than ±50%. We also evaluated the delay of the π-NDRO, which is time difference between 'clock' input and 'dout' output. The delay of the π-NDRO is 14.5 ps at the designed bias voltage 2.5 mV, whereas the delay of conventional NDRO cell in the CONNECT cell library is 15.5 ps. The reason of this slight improvement of delay is that we can decrease the inductance of the storage loop by using p-JJs [15].

At present, implementation of π-JJs with high critical current density (J_C), the same level as JJs implemented by the currently used SFQ circuit fabrication processes, is difficult [20–23]. To investigate how the difference in J_C between JJs and π-JJs affect the circuit operation, we evaluated the dc-bias margin of the π-NDRO by changing J_C of the π-JJs ($J_{C\_\pi JJ}$) and fixing J_C of JJs (J_{C_JJ}) of 2.5 kA/cm^2 by changing capacitance and normal resistance of the π-JJ per unit junction size of the device model in the netlist. Fig. 3 shows the simulated dependence of the dc-bias margin of the π-NDRO on the ratio of $J_{C\_\pi JJ}$ and J_{C_JJ}. No large change in the dc bias margin is observed as shown in Fig. 3. We believe this is useful for implementation of large-scale SFQ circuits composed of both JJs and π-JJs using future circuit fabrication process. Furthermore,



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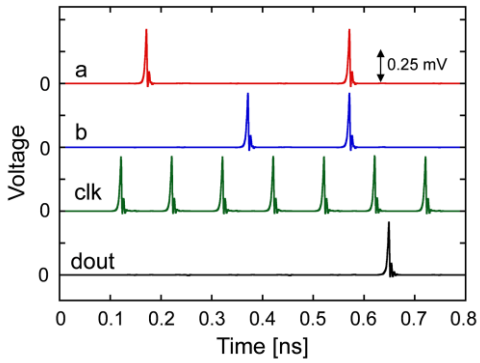


(b)

Fig. 4. (a) The equivalent circuit and (b) an example of the transient analysis of the π-AND. The critical current values of JJs and π-JJs are as follows: J_1 = J_2 = 110 μA, J_3 = J_4 = 140 μA, J_5 = J_6 = 100 μA, J_7 = 120 μA, J_8 = 138 μA, J_9 = 261 μA, P_{10} = P_{11} = 170 μA, J_{12} = J_{13} = J_{15} = 216 μA, J_{14} = 115 μA, and P_{16} = P_{17} = 180 μA. L_1 = L_2 = L_{11} = L_{12} = 3.000 pH, L_3 = L_4 = L_5 = L_6 = 5.000 pH, L_7 = 2.135 pH, L_{13} = L_{14} = L_{17} = 2.458 pH, L_{20} = L_{23} = 0.500 pH, I_{b1} = I_{b2} = I_{b3} = 300 μA, I_{b4} = 168 μA, and I_{b5} = 75 μA.

the product of the critical current (I_C) and normal resistance (R_n) of the JJ implemented by the AIST-STP2, which has J_C of 2.5 kA/cm^2, is approximately 1.7 mV. The maximum operating frequency of the circuit (~$I_CR_n/3\Phi_0$, where Φ_0 is the flux quantum in superconductor) with the J_C of 2.5 kA/cm^2 is roughly estimated to be 274 GHz [24]. Because the maximum operating frequency of the SFQ circuit is proportional to the square root of J_C, the maximum operating frequency of the circuit with J_C of 0.25 kA/cm^2 is 274*(0.25/2.5)$^{0.5}$ ~ 87 GHz, which is still high enough for 10 GHz operation. Therefore, we conclude that the difference in J_C between JJs and π-JJs does not affect the operating margin of the SFQ flip-flops

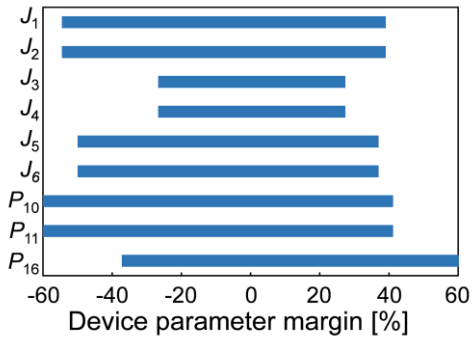
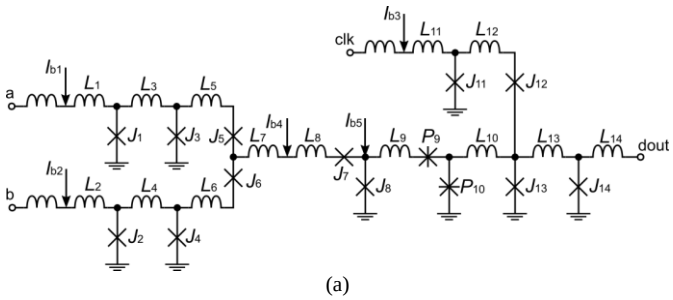


Fig. 5. Device parameter margins of each circuit element of π-AND.



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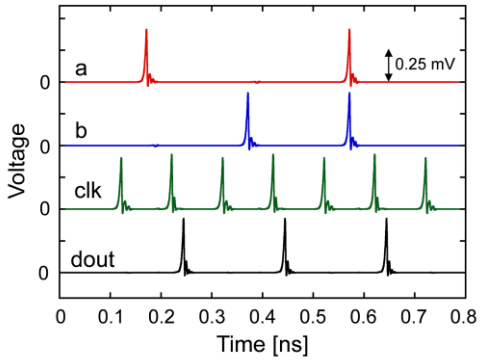


(b)

Fig. 6. (a) The equivalent circuit and (b) an example of the transient analysis of the π-OR. The critical current values of JJs and π-JJs are as follows: J_1 = J_2 = 216 μA, J_3 = J_4 = 247 μA, J_5 = J_6 = 163 μA, J_7 = 120 μA, J_8 = 138 μA, P_9 = 247 μA, P_{10} = 132 μA, J_{11} = 216 μA, J_{12} = 219 μA, J_{13} = 132 μA, and J_{14} = 216 μA. L_1 = L_2 = 3.000 pH, L_3 = L_4 = 3.656 pH, L_5 = L_6 = 1.789 pH, L_7 = 0.5 pH, L_8 = 5.182 pH, L_9 = 3.000 pH, L_{10} = 5.500 pH, L_{11} = 3.000 pH. L_{12} = 3.4 pH, L_{13} = 4.688 pH, L_{14} = 2.314 pH. I_{b1} = I_{b2} = I_{b3} = 300 μA, I_{b4} = 231 μA, and I_{b5} = 56 μA.

when the switching speed of the π-JJ is faster than the circuit operation.

Fig. 4 shows the equivalent circuit and the transient analysis result of the AND gate containing π-JJs (π-AND). The π-AND has two π-storage loops, contain L_3 and L_4, respectively. When the input 'a' and 'b' signals are input, one flux quantum stored in the corresponding π-storage loops. When the 'clk' is applied, the stored flux quantum in the π-storage loops are output simultaneously. The JJ J_7 switches only when two signals are input simultaneously. Therefore, 'dout' is obtained synchronized by the 'clk' input after both 'a' and 'b' are input. The dc-bias margin of the π-AND operating at 10 GHz is -43.2% to +44.0%. Fig. 5 shows the device parameter margins of devices that have margins of less than ±50%. The circuit devices that have the minimum device parameter margin of -26.7% to +27.4% are both J_3 and J_4.

Fig. 6 shows the equivalent circuit and the transient analysis result of the OR gate containing π-JJs (π-OR). The π-OR has one π-storage loop composed of P_{10}, L_{10}, and J_{13} in Fig. 6 (a). When either 'a' or 'b' is input or both 'a' and 'b' are input,

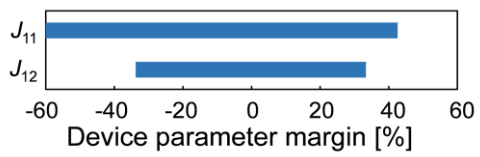


Fig. 7. Device parameter margins of each circuit element of π-OR.

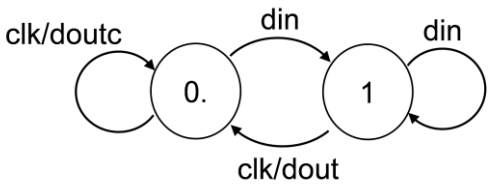


Fig. 8. State transition diagram of the DFFC.

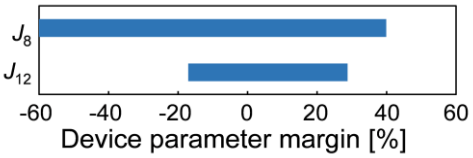
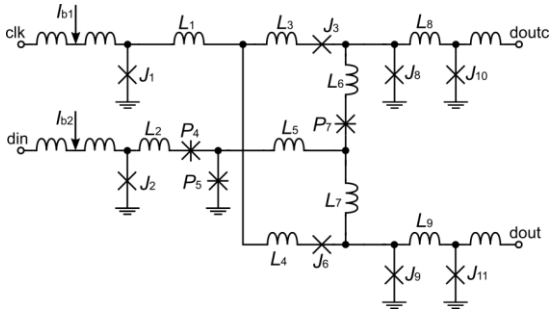


Fig. 10. Device parameter margins of each circuit element of π-DFFC.

one flux quantum is stored in the π-storage loop. Because the flux quantum in the π-storage loop is output when the 'clk' signal is input, the logical OR operation can be performed. The simulated dc bias margin of the π-OR is -35.6% to 44.8% for 10 GHz operation. Fig. 7 shows the device parameter margins of circuit devices of the π-OR that have margins of less than ±50%. The π-OR is relatively tolerant to parameter variation caused by the circuit fabrication compared to the π-AND. The critical circuit device is J_{12} that has the device parameter margin of -33.8% to +33.3%

All designed flip-flops and logic gates have the dc bias margins of ±30% and the critical margins of ±18%. This result indicates that introduction of π phase shift into SFQ flip-flops and logic gates is effective to enhance the operation stability of the circuit as discussed in [11] and [12].

We can implement the SFQ circuits containing π-JJs if the monolithic fabrication process, where both JJs and π-JJs are implemented on the same wafer, is available. However, building such monolithic process might be difficult at present. Another possible implementation method of circuit containing π -JJs is implementation of the circuit using controllable 0-π JJs [25]. By reconfiguring characteristics of specific 0-π JJs into its π-JJ mode, the SFQ circuits containing π-JJs can be implemented.



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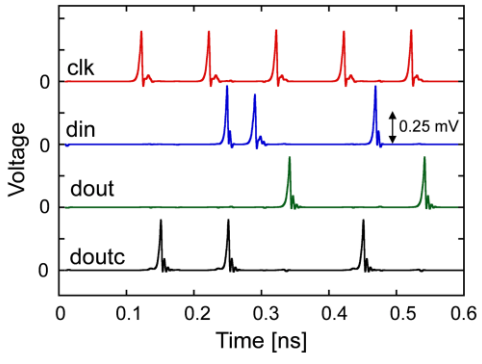

(b)

Fig. 9. (a) The equivalent circuit and (b) an example of the transient analysis of the π-DFFC. The critical current values of JJs and π-JJs are as follows: J_1 = J_2 = 216 μA, J_3 = 2.05 μA, P_4 = 184 μA, P_5 = 108 μA, J_6 = 204 μA, P_7 = 204 μA, J_8 = 100 μA, J_9 = 203 μA, and J_{11} = J_{12} = 203 μA. L_1 = 1.500 pH, L_2 = 3.000 pH, L_3 = L_4 = 0.500 pH, L_5 = 3.000 pH, L_6 = L_7 = 0.500 pH, and L_8 = L_9 = 5.486 pH, and I_{b1} = I_{b2} =300 μA.

III. Delay Flip-Flop with Complementally Outputs

SFQ circuits composed of JJs and π-JJs are thought to be suitable for building flip-flops with complementally outputs because of the physical and logical symmetry of the π-storage loop [15]. We devised a circuit structure of a delay flip-flop with complementally output (DFFC), which does not exist in the CONNECT cell library, composed of JJs and π-JJs. We already designed the non-destructive read flip-flop with complementally outputs containing π-JJs (π-NDROC). The operation of the π-NDROC is represented by the completely symmetric state transition diagram that outputs complementally outputs according to two internal logic states. Therefore, the π-NDROC can be implemented by the structurally and logically symmetric circuit structure using the π-storage loop [15]. However, the logic operation of the DFFC, which is represented by the state transition diagram as in Fig. 8, is not symmetric. Because of the asymmetricity of the logic operation of the DFFC, we have to introduce asymmetry in the circuit structure of the DFFC.

Fig. 9 shows the equivalent circuit and transient analysis result of the designed DFFC containing π-JJs (π-DFFC). To realize the asymmetric logic operation of the DFFC, π-JJ P_7 is inserted in the storage loop and the data (din) is applied asymmetrically. As shown in Fig. 9 (b), the correct operation of the DFFC can be confirmed. The dc-bias margin of the π-DFFC is -36.0% to +33.6%. Fig. 10 shows the device parameter margins of the circuit devices that have less than ±50%. J_{12} has the minimum parameter margin of -17.1% to +28.8%.

The DFFC is the important circuit component of the SFQ decoder, which is indispensable to build memory system [26–28]. The SFQ flip-flops with complementally outputs containing π-JJs can be also applied to processing dual-rail SFQ data [29–31]. Therefore, The SFQ flip-flops containing π-JJs are expected to play the important role in the large-scale SFQ memory systems and asynchronous and ultra-low power dual-rail SFQ logic circuits.

IV. Conclusion

We designed and evaluated the SFQ non-destructive readout flip flop, the AND gate, the OR gate, and the delay flip-flop with complementally outputs composed of JJs and π-JJs. The analog circuit simulation results indicate that all flip-flops and logic gates have wide operating margins and are tolerant to circuit parameter variation caused by the circuit fabrication process. We also found that the influence of the critical current density difference between JJs and π-JJs on the circuit operation is small. These results indicate that the implementation of large-scale system using the SFQ circuits containing π-JJs can be achieved.

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