Improvement of Operating Margin of SFQ Circuits by Controlling Dependence of Signal Propagation Time on Bias Voltage

Mikio Otsubo, Yuki Yamanashi, and Nobuyuki Yoshikawa, *Member, IEEE*

***Abstract*— Superconductive single flux quantum (SFQ) digital circuits can operate at a clock frequency of several tens of gigahertz. However, the operating margin of these circuits decreases with an increase in the operating frequency because a timing error occurs in the low bias region. In this study, a novel design method that enables a wide operating margin at a high operating frequency has been investigated. The proposed circuits incorporate an additional bias feeding line in addition to the conventional bias feeding lines of the conventional Josephson transmission lines (JTLs) and can control the dependence of signal propagation time on the bias voltage. We have shown experimentally that in our proposed JTLs, the signal propagation time becomes more sensitive to the bias voltage. Timing errors can be avoided by inserting proposed JTL cells in the critical data path of the SFQ digital circuits. Circuit simulation results indicate that the operating margin of a bit-serial SFQ full adder, designed assuming the 2.5 kA/cm^2 Nb process, can be improved by 15% as compared with the conventional design at a frequency of 20 GHz by employing our novel design method.**

***Index Terms*—Single flux quantum circuits, Josephson transmission line, Timing error, Full adder**

I. Introduction

CURRENT information and communication technologies (ICTs) have been built on the basis of the developments in the semiconductor integrated circuit technologies. However, these technologies are approaching their physical limits because the thickness of the gate insulating layer of current semiconductor MOS FET is almost the same as the size of a few atoms. Increasing power dissipation is also a serious problem. Building integrated circuit technology on the basis of a new device that can overcome the limitations of semiconductor devices is a natural approach for developing future ICTs. A superconductive single flux quantum (SFQ) circuit has been studied as a next-generation integrated circuit technology because of its high-speed and ultra-low-power operation [1, 2].

Thus far, several high-speed operations of SFQ logic digital circuits have been demonstrated [3, 4]. However, the operating margins of these circuits in the low frequency region are smaller than those in the high frequency region. At low bias voltage, the lower side of the operating margin shrinks with an increase in the operating frequency because of a timing error. Inserting dummy splitters to data and clock paths is one of solutions to prevent the shrink of the operating margin [5]. However, the signal propagation time of the splitter is relatively large and fine timing adjustment is impossible using only dummy splitters.

In this study, a timing design method that enables us to obtain a wide operating margin at a high operating frequency by precisely controlling the dependence of the signal propagation time on the bias voltage has been investigated. The circuit design and measurement results are shown.

II. Timing Error in SFQ Logic Circuit

Fig. 1-(a) shows a simple model of an SFQ logic digital circuit. SFQ logic gates are connected by a data path consisting mainly of Josephson transmission lines (JTLs). The SFQ clock signals are provided to each logic gate via a clock path that is mainly composed of JTLs and pulse splitters. Because the pulse splitter requires a larger driving force owing to the multiple fan-out, the bias dependence of the signal propagation time of the clock path becomes large as compared to that of the data line. Fig. 1 (b) shows typical dependences of

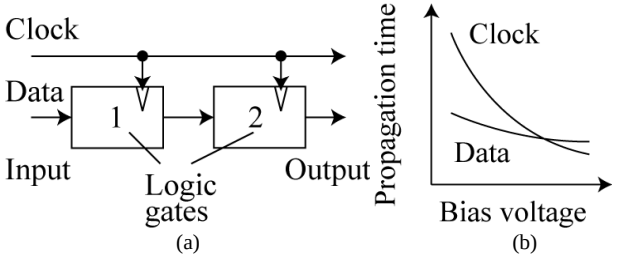

Fig. 1. (a) Schematic of an SFQ logic circuit. (b) Dependence of signal propagation time between the logic gate 1 and 2 on data and clock paths.

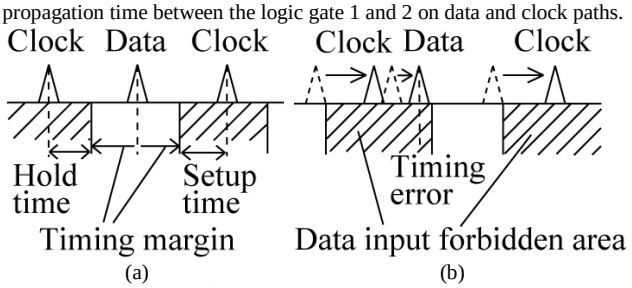

Fig. 2. Timing chart of input to the SFQ logic gate 2 with (a) designed bias voltage of 2.5 mV and (b) low bias voltage. In (b), data input timing violates the timing condition, and a timing error occurs.

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M. Otsubo, Y. Yamanashi and N. Yoshikawa are with the Department of Electrical and Computer Engineering, Yokohama National University, Yokohama 240-8501, Japan (corresponding author e-mail: otsubo@nashilab.dnj.ynu.ac.jp).

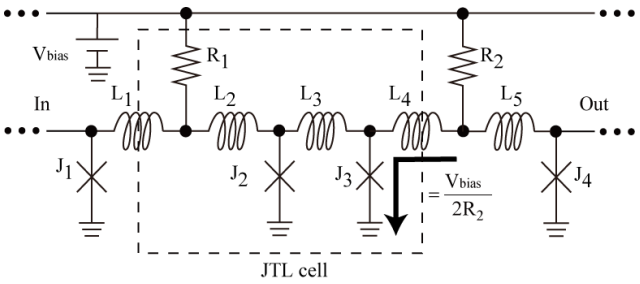

Fig. 3. Equivalent circuit of a normal JTL. The circuit surrounded within the dashed rectangle corresponds to a JTL cell. Ic_{J1} = Ic_{J2} = Ic_{J3} = Ic_{J4} = 216 μA, R_1 = 8.34 Ω, L_1 = L_2 = L_4 = L_5 = 2.5 pH, L_3 = 4.9 pH. Ic_{Ji} represents the critical current of the Josephson junction J_i.

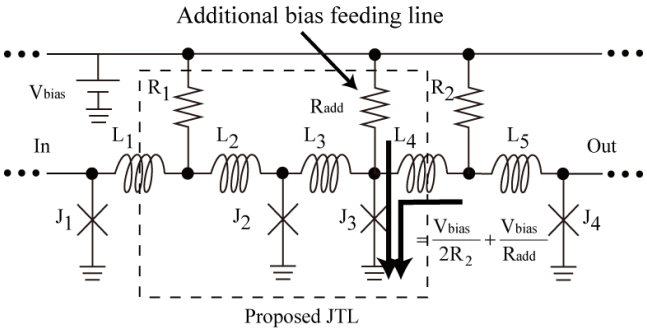

Fig. 4. Equivalent circuit of the proposed JTL

the signal propagation time on the bias voltage supplied to the circuit.

Precise timing adjustment is critical for high-speed operation of SFQ logic digital circuits [6]. Fig. 2 shows the timing chart of data and clock inputs to the SFQ logic gate. All SFQ logic gates have a data input forbidden time, which is the sum of their set-up and hold times. The time region, where data can be input is called the timing window. For high-speed operation of SFQ digital circuits, the data signal should be input near the center of the timing window as shown in Fig. 2-

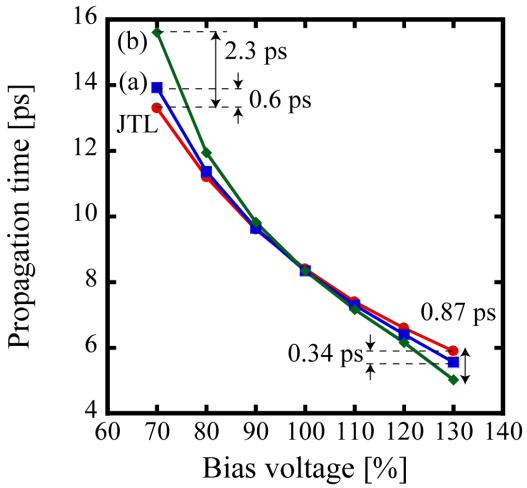

Fig. 5. Dependence of signal propagation times of JTL and the proposed JTLs on bias voltage. Bias voltage is normalized by the designed bias voltage, 2.5 mV. JTL curve corresponds to bias dependence of a normal JTL. Curve (a) Ic_{J3} = 252 μA R_{add} = 67 Ω, Curve (b) Ic_{J3} = 300 μA R_{add} = 27 Ω.

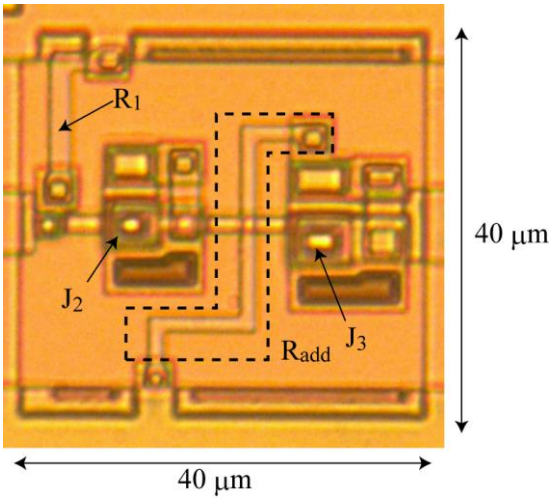

Fig. 6 Chip photograph of proposed JTL.

(a). However, the data input timing shifts when the bias voltage changes because the dependences of signal propagation time into JTLs and a logic gate on the bias voltage differ for the data and clock paths as shown in Fig. 2 (b). This timing shift causes a timing error for the SFQ logic gate, resulting in malfunction of SFQ logic digital circuits. The lower side of the operating margin of an SFQ digital circuit at a high-speed operating frequency is limited by this timing shift [3, 4].

III. Design of Timing Adjustable JTLs

Fig. 3 shows an equivalent circuit of the normal JTL cell in the CONNECT cell library [7]. In the initial state, where no signal is input, the bias current is supplied by the bias voltage source and a bias resistor flows in each Josephson junction (JJ). The propagation time of the SFQ pulse is mostly determined by the value of the initial bias current because the SFQ pulse in a circuit is driven by the current flowing in the JJs. The value of the initial bias current linearly increases with an increase in the bias voltage. Therefore, the signal propagation time of the JTL decreases with an increase in the bias voltage.

Fig. 4 shows an equivalent circuit of the proposed JTL, where a Josephson junction J_3 is current-biased by not only the bias resistor R_2 but also R_{add}. Owing to the additional bias feeding line, the dependence of the initial current flowing in J_3 on the bias voltage becomes different from the case of the normal JTL cell. Therefore, the signal propagation time of the proposed JTL cell becomes sensitive to the bias voltage, as compared with the normal JTL cell. By changing the circuit parameters Ic_{J3} and R_{add}, the dependence of the signal propagation time on the bias voltage can be adjusted at some level. The initial bias current flowing in the J_3 of the normal JTLs in Fig. 3 is represented as

$$I_{init} = \frac{1}{2R_2} \cdot V_{bias}, \quad (1)$$

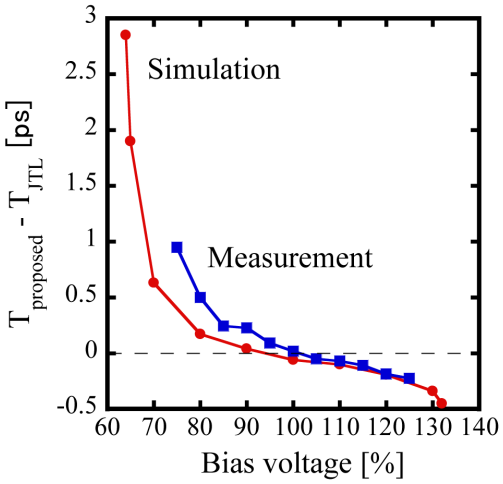

Fig. 7. Dependence of difference between propagation times for JTL and the proposed JTL (Ic_{J3} = 252 μA, R_{add} = 67 Ω) on bias voltage. The bias voltage is normalized by the designed bias voltage, 2.5 mV.

where V_{bias} is the bias voltage. On the other hand, the initial bias current flowing in the J_3 in Fig. 4 is represented by

$$I_{init} = \left(\frac{1}{2R_2} + \frac{1}{R_{add}} \right) \cdot V_{bias}. \quad (2)$$

Therefore, the increase of initial current of the proposed JTL is larger than that of the normal JTL by the term of $1/R_{add}$ in eq. (2) when bias voltage increases. The sensitivity of the signal propagation delay to the bias voltage can be controlled by adjusting the resistance R_{add}. To obtain the more sensitive dependence of signal propagation time on the bias voltage, the critical current of J_3 should be as large as possible to make R_{add} small. In this study, the critical current of J_3 was chosen to be 300 μA, which is the maximum critical current in the cells of the CONNECT cell library. In addition, the proposed JTL having the critical current of J_3 of 252 μA, is designed to confirm the critical current dependence of the signal propagation time. In addition, the value of resistance R_{add} was designed so that the signal propagation time of the proposed JTL at the designed bias voltage (2.5 mV) becomes equal to the value for a normal JTL.

Fig. 5 shows the simulated dependences of the signal

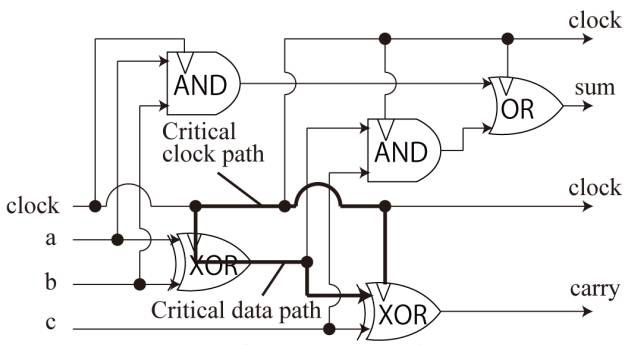

Fig. 8. Block diagram of a bit-serial SFQ full adder. The arrows represent signal propagation line composed of JTL cells and splitters.

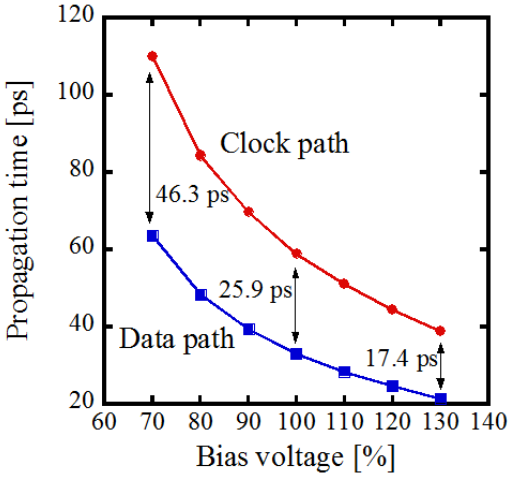

Fig. 9. Dependence of data path and clock path propagation times on bias voltage before inserting the proposed JTLs.

propagation time of the proposed JTLs on the bias voltage. In this simulation, the use of the SRL 2.5 kA/cm^2 Nb process [8] was assumed. As shown in Fig. 5, the propagation time becomes more sensitive to a change in the bias voltage when the critical current J_3 increases. Fig. 6 shows a photograph of a chip with the implemented proposed JTL cell. The proposed JTL cell could be implemented by simply replacing J_3 of normal JTL with JJ having larger critical current and adding an additional bias feeding line to the normal JTL cell.

We have designed a test circuit to measure the bias dependence of the signal propagation time of the proposed JTL cells. We have designed two ring oscillators: one is a simple SFQ ring oscillator consisting of normal JTLs, and the other comprises normal JTL cells and the proposed JTL cells. The oscillation frequencies were measured using the average output voltage method [9]. By comparing the measured oscillation frequencies of the two ring oscillators, the difference between the signal propagation times for the normal and the proposed JTL cells was measured. Fig. 7 shows the

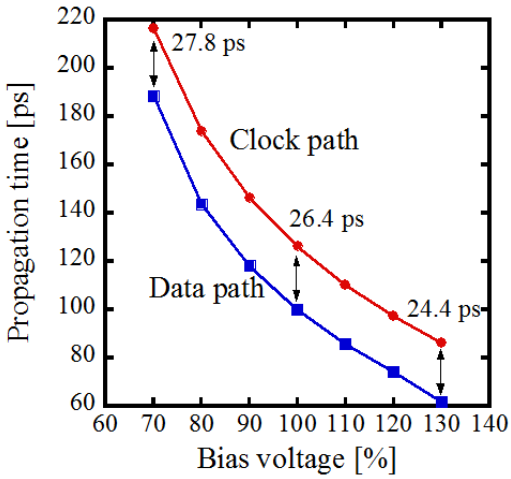

Fig. 10. Dependence of data path and clock path propagation times on bias voltage after inserting the proposed JTLs.

measured difference between the signal propagation times for the normal and the proposed JTLs as a function of the bias voltage. As shown in Fig. 7, the propagation time was found to be more sensitive to the bias voltage as compared with the normal JTL cell. The difference between the simulation and measurement was thought to be caused by a discrepancy between designed circuit parameters and fabricated parameters. This result indicates that we can control the dependence of the signal propagation time on the bias voltage in SFQ logic circuits using the implemented JTLs.

IV. Improvement of Operating Margin Using Timing Adjustable JTLs

To demonstrate the effectiveness of the investigated timing design method, we have designed and simulated a bit-serial SFQ full adder. Fig. 8 shows the block diagram of the SFQ full adder. Fig. 8 also shows its critical data and clock paths, which determine the lower operating margin of the adder for high-frequency operation. Fig. 9 shows the dependence of the propagation times of the critical data and clock paths on the bias voltage of the conventional SFQ full adder. In the conventional design, the difference between the signal propagation times for critical data and clock lines was 46.3 ps at 70% of the bias voltage, whereas this difference was 25.9 ps at the designed bias voltage.

We have designed a new bit-serial SFQ full adder using the proposed JTL cells. The difference between the signal propagation times for the critical data and clock lines at the voltage of 70% should be reduced by 20.4 ps (= 46.3 – 25.9 ps) to make the time difference between the bias voltages of 70% and 100% the same. Because the propagation time of the proposed JTL cell is larger than that of normal JTL cell by 2.3 ps at the bias voltage of 70%, nine proposed JTL cells were inserted to the data path. Fig. 10 shows the bias dependence of the signal propagation times of the critical data and clock paths optimized with the proposed JTL cells. We also designed the FA using only dummy splitters to compare the design result.

Table 1 summarizes the comparison between the conventional and the newly designed bit-serial SFQ full adders. Though inserting the proposed JTLs increase the circuit scale, the timing error in the low-bias region does not occur. Fig. 11 compares the dependences of the operating margins of the conventional and the newly designed full adders on the operating frequency. The lower operating margin, which is limited by the large difference between the dependences of the signal propagation times for data and clock paths, is improved by using the proposed JTL cells. At a clock frequency of 20 GHz, the operating margin of the newly designed SFQ full adder is improved by 15% as compared with the conventional adder.

TABLE I
Comparison of Conventional and Newly Designed Adders

	Circuit area	Number of JJs
Conventional full adder	0.136 mm^2	231
Full adder designed with splitters	0.251 mm^2	395
Full adder designed with proposed JTLs	0.355 mm^2	505

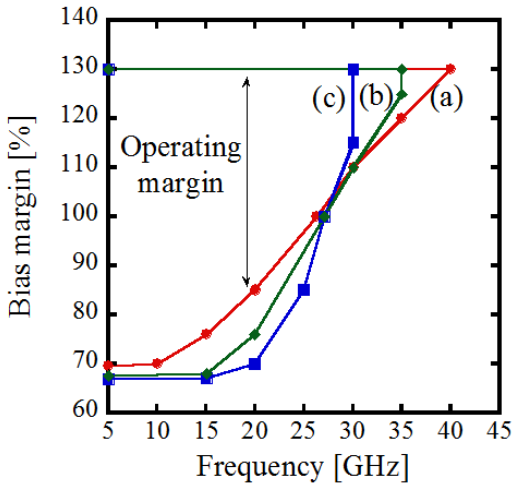

Fig. 11 Comparison of operating margins of (a) the original full adder (FA), (b) the FA designed using dummy splitters, and (c) the FA designed using the proposed JTLs in all data paths.

V. Conclusion

We have investigated a new design method for high-speed and stable operation of SFQ logic digital circuits. The bias dependence of the signal propagation time of a JTL can be controlled by adding an additional bias feeding line to a Josephson junction in the JTL. We have measured the signal propagation time of the resulting JTL with an SFQ ring oscillator and obtained reasonable characteristics that were similar to the simulation result. We demonstrated that the operating margin of the SFQ full adder can be improved by 15% as compared with a conventional design at a frequency of 20 GHz by employing our novel design method.

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