Improvement of Operation Speed of LR-Biased Low-Power Single Flux Quantum Circuits by Introduction of Dynamic Resetting of Bias Currents

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***Abstract*— We propose a new LR-biased low-power single flux quantum (SFQ) circuit that has a dynamic resetting mechanism of the bias current. Because the bias current returns to the initial state rapidly by switching of a Josephson junction in the bias circuit after circuit operation, the operating frequency of the LR-biased SFQ circuit can be improved. We simulated a Josephson transmission line (JTL) that employs the proposed biasing scheme and evaluated the bias current recovery time. Circuit simulation results show that the bias current recovery time of the proposed circuit is improved by 10%-20% compared to that of the conventional LR-biased JTL. We have designed and measured a 10-stage JTL and an 8-bit concurrent-flow shift register with the proposed biasing scheme. We have experimentally demonstrated operation of the JTL with the bias margin of ±29.4% at the operating frequency of up to 70.4 GHz and operation of the 8-bit shift register up to 12.3 GHz by the on-chip high speed test.**

***Index Terms*—Josephson junction, RSFQ, low-power circuit, LR-biasing.**

I. Introduction

A single flux quantum (SFQ) circuit can operate at a high clock frequency with ultra-low power consumption [1, 2]. However, if the cooling cost of the SFQ circuit-based systems is considered, the power consumption should be reduced furthermore to use the high energy efficiency of the SFQ circuit in practical applications.

So far, several low-power superconducting circuits have been proposed and implemented [3-7]. The low-power superconducting circuits are divided into DC-biased and AC-biased circuits. We think the DC-biased SFQ circuits are suitable for the high-speed and flexible circuit operation because they do not need high-frequency clock input from the room temperature electronics. In the conventional SFQ circuits, which is driven by DC bias currents, a large amount of power is consumed by on-chip bias resistors statically for proper bias current distribution. Reduction in static power consumption by decreasing on-chip bias resistances and the bias voltage is effective to reduce total power consumption of the SFQ circuit. Among DC-biased superconducting circuits, the eSFQ and the ERSFQ circuits do not need on-chip bias resistors and thus zero static power operation is possible [3, 4]. However, the eSFQ circuit needs Josephson junction pairs in not only logic gates but also in the bias network because the superconducting phase across all Josephson junction pairs have to increase by 2π every clock cycle to keep the appropriate bias current distribution [3]. The ERSFQ circuits needs an additional circuit to feed the constant bias voltage. These design restrictions might limit the flexibility of the circuit operation.

We have been studying an LR-biased SFQ circuit [8, 9], where the DC bias currents are supplied by small bias resistors and the low bias voltage. The LR-biased SFQ circuit can be implemented by simply replacing the bias circuit of the conventional SFQ circuits. Therefore, all circuits that are implemented by the conventional SFQ circuit can be designed using the LR-biased circuit. However, the operating speed of the LR-biased SFQ circuit is limited by the bias current recovery time determined by the LR time constant of the bias circuit [9]. The trade-off between the low-power characteristic and the operating speed of the LR-biased SFQ circuit has been discussed [10].

In this study, we propose a new LR-biased SFQ circuit that has a dynamic resetting mechanism of the bias current to improve the operation speed. We investigate bias current recovery time of the newly proposed LR-biased SFQ circuit on the basis of analog circuit simulation. The experimental results of a Josephson transmission line (JTL) and a shift-register (SR) designed by using the proposed biasing scheme are shown.

II. LR-Biased SFQ Circuit with Dynamic Resetting Mechanism

Fig. 1 shows an equivalent circuit and the simulation result of the conventional LR-biased Josephson transmission line (JTL) driven by the bias voltage of 0.2 mV. A bias current is supplied to the JTL by a low bias voltage V_b, a small bias resistor R_b, and a large inductor L_b. The static power consumption of the simulated JTL is reduced by 92% compared

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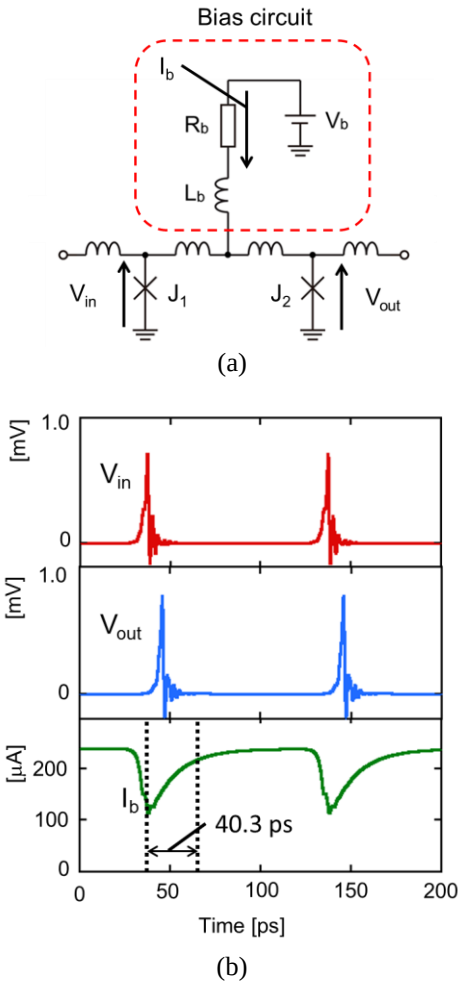

Fig. 1. (a) Equivalent circuit of a 1-stage LR-biased Josephson transmission line (JTL) and (b) its simulation result. J_1 = J_2 =216 μA, L_b = 10 pH, R_b = 0.84 Ω, V_b = 0.2 mV.

to conventional SFQ circuit driven by the 2.5 mV bias voltage [11]. After the SFQ pulse propagates, the bias current decreases by switching of the Josephson junction due to the low bias voltage. The bias current returns to the initial current value with the time constant of L_b/R_b. Because the following SFQ pulse input is not acceptable before the bias current recovering, the operating speed of the LR-biased SFQ circuit is limited by the ratio of the bias voltage and the time constant L_b/R_b [10]. Assuming the bias current recovery time as time required to return to the 90% of the initial bias current value, the bias current recovery time of the simulated LR-biased JTL is 40.3 ps.

Fig. 2(a) shows an equivalent circuit of the proposed LR-biased JTL that has a dynamic resetting mechanism. The JTL has an additional loop composed of a small resistor R_{loop} and a small Josephson junction J_{loop}. When the SFQ signal is input to the JTL, the SFQ signal is split and output to the output port and input to the additional loop. The input SFQ signal, which is input to the additional loop, is released from the loop by switching of J_{loop} and the bias current I_b returns to its initial value dynamically. The Josephson junction with the small critical current is used in the additional loop, though the critical

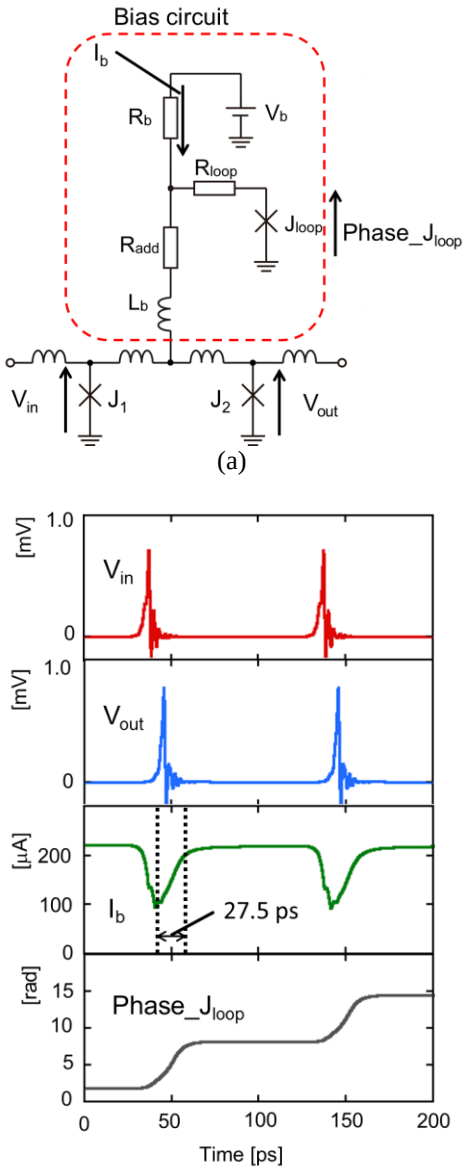

Fig. 2. (a) Equivalent circuit of a 1-stage LR-biased JTL with a dynamic resetting mechanism and (b) its simulation result. J_1 = J_2 =216 μA, L_b = 10 pH, R_b = 0.84 Ω, R_{loop} = 0.4 Ω, R_{add} = 0.05 Ω, J_{loop} = 45 μA, V_b = 0.2 mV.

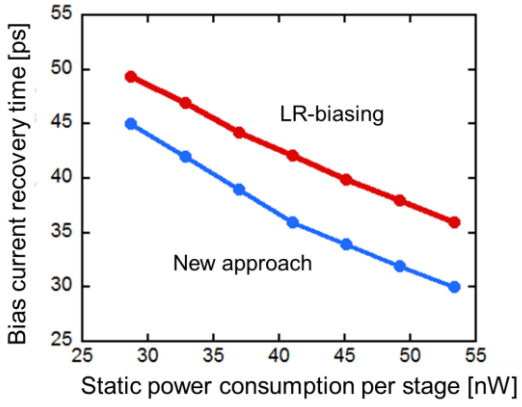

Fig. 3. Dependence of the bias current recovery time of conventional and new LR-biased JTLs on static power consumption per stage.

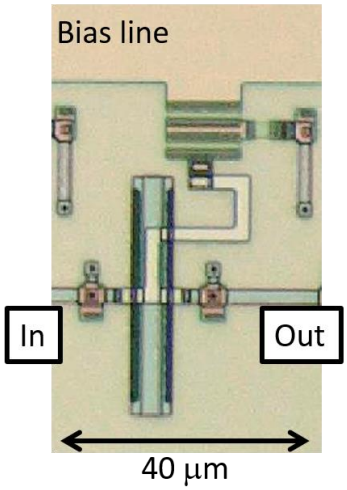

Fig. 4. Microphotograph of the 1-stage JTL with the proposed biasing scheme.

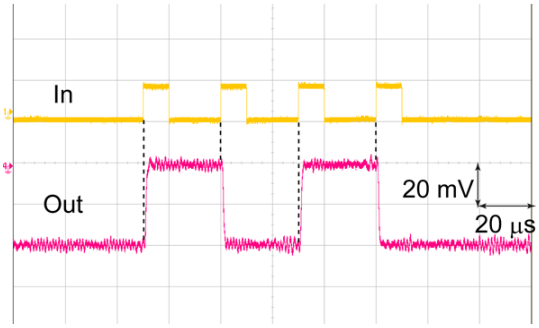

Fig. 5. Measured waveform of 10-stage JTL using the proposed biasing scheme.

current of the Josephson junction larger than 100 μA are usually used in the SFQ circuit to avoid the logical errors caused by thermal noises. However, the Josephson junction J_{loop} is used for releasing the stored flux quantum from the circuit and is not related to the logical operation of the SFQ circuit. Therefore, use of the small Josephson junction does not result in the logical error of the LR-biased SFQ circuit. Fig 2(b) shows the simulated input-output characteristics of the JTL and the bias current recovery process after the SFQ pulse propagation. In the simulation shown in Fig. 2(b), the bias current recovery time is 27.5 ps.

Because the total amount of bias current of the proposed LR-biased circuit increases by the additional loop, static power consumption of the JTL shown in Fig. 2 by approximately 10% compared to that of the conventional LR-biased JTL. In order to fairly compare the bias recovery time of conventional and proposed LR-biased circuits, we evaluate the bias current recovery time of the both circuits as a function of static power consumption of the JTL on the basis of analog circuit simulation. Fig. 3 shows the dependences of the bias current recovery time of the JTL on the static power consumption. As shown in Fig. 3, the bias current recovery time of the proposed LR-biased circuit is shorter than that of the conventional LR-biased circuit by 10%-20%.

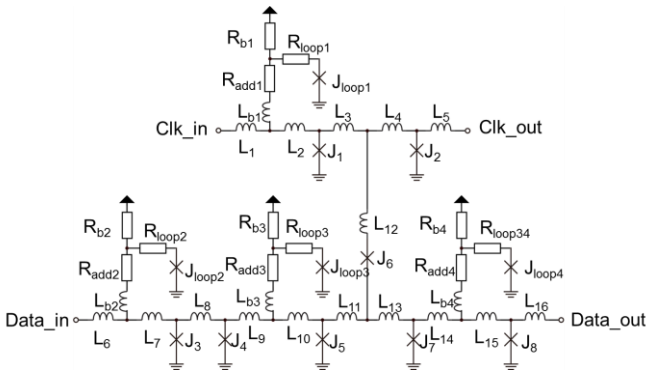

Fig. 6. Schematic diagram of shift register (SR) using the proposed biasing scheme. Bias voltage is 0.25 mV. $L_{b1} = L_{b2} = L_{b3} = L_{b4} = 15$ pH, $L_1 = 0.32$ pH, $L_2 = 2.3$ pH, $L_3 = 0.10$ pH, $L_4 = 6.4$ pH, $L_5 = 2.1$ pH, $L_6 = 0.3$ pH, $L_7 = 2.4$ pH, $L_8 = 2.7$ pH, $L_9 = 1.6$ pH, $L_{10} = 9.7$ pH, $L_{11} = 0.5$ pH, $L_{12} = 3.5$ pH, $L_{13} = 5.3$ pH, $L_{14} = 0.5$ pH, $L_{15} = 5.8$ pH, $L_{16} = 1.9$ pH, $R_{b1} = R_{b2} = 0.19$ Ω, $R_{b3} = 0.95$ Ω, $R_{b3} = 0.74$ Ω, $R_{loop1} = R_{loop2} = 1.71$ Ω, $R_{loop3} = 0.3$ Ω, $R_{loop4} = 0.6$ Ω, $R_{add1} = R_{add2} = R_{add3} = R_{add4} = 0.2$ Ω, $J_{loop1} = J_{loop2} = J_{loop3} = J_{loop4} = 50$ μA, $J_1 = J_2 = J_3 = 210$ μA, $J_4 = 157$ μA, $J_5 = J_6 = 100$ μA, $J_7 = 161$ μA, $J_8 = 200$ μA.

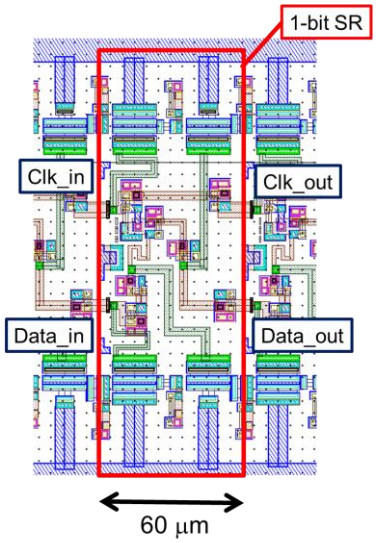

Fig. 7. Layout of 1-bit shift register using the proposed biasing scheme.

III. Circuit Design and Measurements

We have designed a 10-stage JTL with the proposed LR-biasing scheme using the AIST 10 kA/cm^2 Nb advanced process [12, 13]. The designed bias voltage of the JTL is 0.125 mV, which is 1/20 of the typical bias voltage of the conventional SFQ circuit [10]. Fig. 4 shows the microphotograph of the implemented JTL. The wide and short resistor layers are used to implement 0.05 Ω resistors in the additional loop. The circuit area of the JTL is larger than that of the conventional LR-biased circuit by approximately 50% because of use of the small resistors. We believe that the circuit area can be reduced by using the advanced circuit fabrication process that has a resistance layer with low-resistivity [14]. Fig. 5 shows a measurement result of the 10-stage JTL. We confirmed the correct operation of the 10-stage JTL at the frequency of 70.4 GHz by the high-speed test. The measured bias margin was ±29.4% independent of the operating

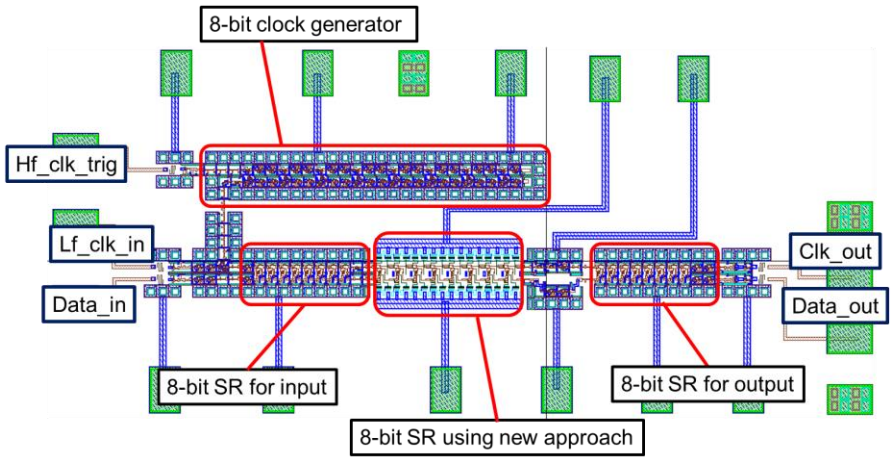

Fig. 8. Layout of the test circuit of the 8-bit SR using proposed technique and whole measurement circuits.

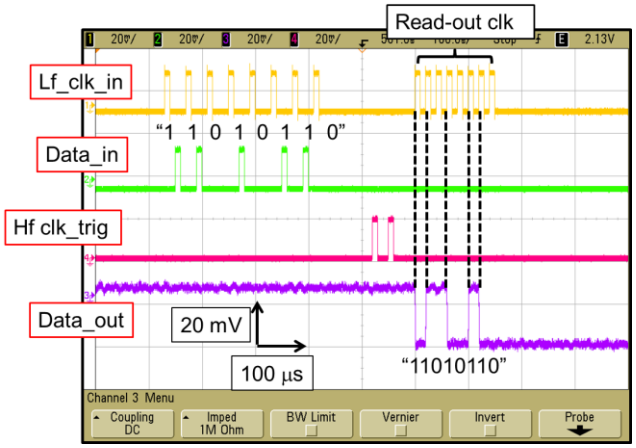

Fig. 9. Measurement waveform of 8-bit SR using proposed technique. The "Hf_clk_trig" is trigger signal for the 8-bit clock generator.

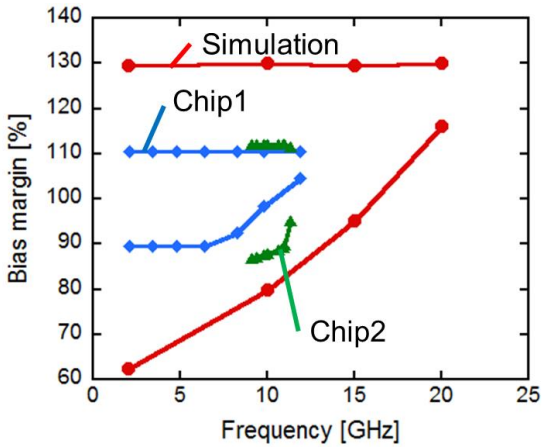

Fig. 10. Dependence of the bias margin of the operating frequency of 8-bit SR using proposed technique. The bias margin is normalized by the designed bias voltage, 0.25 mV.

frequency.

We also designed an 8-bit concurrent-flow SR using the proposed LR-biased SFQ circuit and the AIST 2.5 kA/cm^2 Nb standard process 2 [15]. Fig. 6 shows an equivalent circuit of the 1-bit SR cell. The 8-bit SR was designed by using eight SR cells. The designed bias voltage of the 8-bit SR is 0.25 mV. Analog circuit simulation shows the maximum operating frequency of the 8-bit SR is 20 GHz, which is higher than the conventional LR-biased SR driven by the same bias voltage by approximately 30%. Fig. 7 shows a mask layout of the 1-bit SR cell designed by using the proposed biasing scheme. The designed 8-bit SR contains 96 Josephson junctions. We employed the on-chip high-speed test method [16] to confirm the high-speed operation. Fig. 8 shows a mask layout of the test circuit. In this test circuit, the conventionally biased 8-bit SFQ clock generator and 8-bit SR are implemented. Fig. 9 shows a measured waveform of the 8-bit SR. After inputting the 8-bit data to the conventionally biased 8-bit SR for input using low-frequency clock inputs (Lf_clk_in), the 8-bit clock generator is triggered by the "Hf_clk_trig" signal and the data are input to the SR under test. The following trigger input (Hf_clk_trig) is used for data output form the SR under test. The 8-bit shift of the input data was experimentally confirmed and thus the high-speed input/output operation of the SR was demonstrated. Fig. 10 shows the measured and simulated dependences of the bias margin of the 8-bit SR on the operating frequency. The results of two chips (Chip 1 and Chip 2) are shown. The experimentally obtained maximum operating frequency of the SR was 12.3 GHz.

IV. Conclusion

We proposed a new biasing scheme for the LR-biased low-power SFQ circuit to improve the operating speed. The bias current is dynamically recovered after circuit operation by switching of the Josephson junction that releases the magnetic flux quantum from the bias circuit. The simulation results shows the bias current recovery time of the LR-biased SFQ circuits is improved by 10%–20% by introducing the new biasing scheme. We have designed the 10-stage JTL and the 8-bit SR that employ the proposed biasing scheme. We have experimentally confirmed correct high-speed operation of the 10-stage JTL and the 8-bit SR by the on-chip high-speed test.

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