High-Speed Experimental Demonstration of Adiabatic Quantum-Flux-Parametron Gates Using Quantum-Flux-Latches

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Abstract— We experimentally demonstrated high-speed logic operations of adiabatic quantum-flux-parametron (AQFP) gates through the use of quantum-flux-latches (QFLs). In QFL-based high-speed test circuits (QHTCs), the output data of the circuits under test (CUTs), which are driven by high-speed excitation currents, are stored in QFLs and are slowly read out using low-speed excitation currents. We designed and fabricated three types of QHTCs using QFLs with different circuit parameters, where the CUTs were buffer gates and AND gates. We confirmed the correct operation of buffer gates and AND gates at 1 GHz. The obtained bias margins of the 1 GHz excitation currents were more than $\pm 30\%$ for each QHTC, which is wide enough for high-speed logic operations of AQFP gates.

Index Terms— superconducting integrated circuits, Josephson circuits, AQFP, latch, high-speed operation, adiabatic logic

I. INTRODUCTION

ADIABATIC quantum-flux-parametron (AQFP) logic [1, 2] is one of the energy-efficient superconductor logics [3–5]. Among these devices, AQFP logic is very energy-efficient and can achieve sub- $I_c\Phi_0$ bit-energy operation because of adiabatic switching. We measured the energy dissipation of an AQFP gate with critically-damped Josephson junctions and showed that its bit energy is ~ 10 zJ at 5 GHz operation [6], which is only $170 k_B T$ at 4.2 K where k_B is the Boltzman constant and T is the temperature. Moreover, we simulated the energy dissipation of AQFP gates with underdamped junctions. The results indicated that the bit energy can fall below the thermal energy ($\sim 5.8 \times 10^{-23}$ J at 4.2 K), unless the entropy decreases [7].

We designed and implemented several AQFP logic circuits [8], including a majority gate and a full adder. In addition, we proposed and designed the quantum-flux-latch (QFL) [9, 10] as a novel latch for AQFP logic in order to achieve practical energy-efficient computing systems using AQFP logic.

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However, these gates were demonstrated only at a low speed of ~ 100 kHz, because of the lack of high-speed test circuits. In the present study, we propose a high-speed test circuit using QFLs and experimentally demonstrate high-speed logic operations of AQFP gates.

II. QUANTUM-FLUX-LATCH (QFL)

Figure 1 shows a circuit schematic of a QFL, which is composed of an AQFP gate, the input inductance of which is replaced by a storage loop. The storage loop includes a Josephson junction, J_0 , and is biased by the dc current, I_b . The internal state of a QFL is represented by the absence or presence of a single-flux-quantum (SFQ) stored in the storage loop. The read gate, which is driven by an excitation current, I_x , can non-destructively read out the internal state. The flux state in the storage loop changes only when an SFQ is stored or escapes. When both of the write gates are in logic state “1”, J_0 switches, and the storage loop stores an SFQ, which corresponds to “Write 1”. When both of the write gates are in logic state “0”, the stored SFQ escapes from the loop, which corresponds to “Write 0”. When the two write gates are in the different logic states, the QFL holds its current state, because the applied fluxes from the write gates cancel each other. A QFL is composed of only three junctions and requires only one clock cycle for both read and write. We reported an experimental demonstration of a QFL and a 1-bit shift register using QFLs in a previous study [10].

Fig. 1. Circuit schematic of a QFL gate. For the write gates, $\beta_L = 0.4$, $\beta_q = 5.5$ and $I_c = 100$ μ A. For the read gates, $\beta_L = 0.4$, $\beta_q = 3.2$ and $I_c = 100$ μ A. $\beta_L = 2\pi L_1 I_c / \Phi_0 = 2\pi L_2 I_c / \Phi_0$, $\beta_q = 2\pi L_q I_c / \Phi_0$. $L_{inb} = L_{inb} = 23$ pH, $k_a = k_b = 0.48$.

III. QFL-BASED HIGH-SPEED TEST CIRCUIT (QHTC)

In order to demonstrate the AQFP circuit at high speed (in the GHz range), we use QFLs to hold and readout data. Figure 2 shows a block diagram of a QFL-based high-speed test circuit (QHTC), where circuits under test (CUTs) are driven by high-speed excitation currents, I_{xhi} , and the QFLs and readout buffers are driven by low-speed excitation currents, I_{xlo1} and I_{xlo2} , respectively. Three-phase high-speed excitation currents, I_{xhi1} , I_{xhi2} , and I_{xhi3} , are generated using a power divider, which also adds a dc-offset to each excitation current, and are terminated by on-chip $50\ \Omega$ resistances. The output data of CUTs are latched by QFLs after split by splitter (SPL) gates. The latched data are read out at low speed using dc-SQUIDS, where we inserted the readout buffers in order to reduce backactions from the dc-SQUIDS to the QFLs. The dc-SQUIDS turn into voltage states when the states of readout buffers are “1”.

We designed three types of QHTCs, α , β , and γ , by means of the 3D inductance extractor, InductEx [11], and fabricated the QHTCs using the Nb Josephson process, the AIST standard process (STP2) [12], with a critical current density of $2.5\ \text{kA/cm}^2$. In α , the CUT is a buffer gate, and the QFL has $J_0 = 40\ \mu\text{A}$. In β , the CUT is a buffer gate, and the QFL has $J_0 = 30\ \mu\text{A}$. In γ , the CUT is an AND gate, and the QFL has $J_0 = 40\ \mu\text{A}$. We used two J_0 settings because J_0 and I_b are the critical parameters in a QFL. Figure 3 shows a micrograph of these three QHTCs.

Figure 4 shows the high-speed measurement results at 1 GHz, where we applied ac bias currents, I_{sq} , to the dc-SQUIDS in order to reduce backactions to the readout buffers, and V_{out} is the output voltage of the dc-SQUIDS amplified by 200 times through the use of differential amplifiers. Figure 4a shows the three-phase high-speed excitation currents at 1 GHz generated by a power divider, where the small oscillations are due to reflections between the power divider and an oscilloscope. Figure 4b shows the measurement results for α , and Fig. 4c

Fig. 2. Block diagram of a QHTC. The output data of the CUT operating at high speed are stored in QFLs and read out at low speed. dc-SQUIDS are used to read out the internal states of QFLs.

Fig. 3. Micrograph of QHTCs. The three-phase high-speed excitation currents, I_{xhi} , are provided externally and are terminated by the $50\ \Omega$ on-chip resistances.

shows the measurement results for γ . In both α and γ , the CUTs operated correctly at 1 GHz. We also confirmed correct operation in β at 1 GHz. The bandwidth of the probe that we used was $\sim 1\ \text{GHz}$, which prevented demonstrations at a higher operation frequency.

Table I shows the obtained margins for each bias current. Here, I_{xhi} has wide bias margins of more than $\pm 30\%$ in all QHTCs, and I_b has a small margin of only $\pm 5.3\%$ in α , which is much smaller than the simulation results of $\pm 17\%$. We believe that this is because J_0 was larger than the designed value in this fabrication. In fact, in β with smaller junctions, the measured margin increased to $\pm 16\%$. Therefore, we can obtain reasonably wide margins of I_b by reducing the junction size of J_0 , even if the parameter variation is larger than expected.

IV. CONCLUSION

We proposed the QHTC as a high-speed test circuit for AQFP logic gates, where the output data of CUTs, operating at high speed, are stored in QFLs and are read out at low speed. We experimentally demonstrated high-speed operation of AQFP buffer gates and AND gates at 1 GHz. Obtained margins of high-speed excitation currents were more than $\pm 30\%$, which is wide enough for practical systems using AQFP logic gates. The margin of the dc bias currents to QFLs was smaller than expected but increased to $\pm 16\%$ by reducing the size of the junctions in QFLs.

Fig. 4. High-speed measurement results at 1 GHz. (a) Three-phase excitation currents at 1 GHz generated by a power divider. (b) α : the CUT is a buffer gate. (c) β : the CUT is an AND gate.

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TABLE I
MEASURED BIAS MARGINS OF EACH QHTC

	α	β	γ
I_{xhi}	$\pm 31.0 \%$	$\pm 34.9 \%$	$\pm 31.0 \%$
I_{xlo1}	$\pm 43.8 \%$	$\pm 37.2 \%$	$\pm 45.0 \%$
I_{xlo2}	$\pm 31.2 \%$	$\pm 30.7 \%$	$\pm 27.5 \%$
I_{sq}	$\pm 18.1 \%$	$\pm 15.8 \%$	$\pm 17.4 \%$
I_b	$\pm 5.3 \%$	$\pm 16.2 \%$	$\pm 6.3 \%$

(AIST) with the standard process 2 (STP2). The AIST-STP2 is based on the Nb circuit fabrication process developed in International Superconductivity Technology Center (ISTEC). The authors would like to thank Coenrad Fourie for improving the 3D inductance extractor, InductEx that we used during the layout design of the circuits.

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