Study of LR-Loading Technique for Low-Power Single Flux Quantum Circuits

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Abstract—A single-flux-quantum (SFQ) circuit is thought to be very suitable as a peripheral circuit for superconducting quantum bits (qubits), which can manipulate and detect the qubit state at a temperature state similar to qubits. Even though the power consumption of SFQ circuits is extremely small, it is still sufficient to heat the substrate at a temperature below 1 K. We have investigated and demonstrated low-power SFQ circuits for this application, using the LR-loading technique, which can reduce the static power consumption of the SFQ circuits. Simulation results show that the ratio of the switching speed to the time constant of the bias circuit is important for the stable operation of low-power SFQ circuits. The static power consumption of SFQ circuits can be reduced to the same order as the dynamic power consumption through optimization of the circuit parameters. We have designed and tested a low-power SFQ clock generator using the LR-loading technique and confirmed its stable operation at 4.2 K, where the power consumption is reduced by 93% compared with ordinary biased circuits.

Index Terms—Josephson logic, quantum bit, SFQ circuit, superconducting devices, superconducting integrated circuits.

I. INTRODUCTION

A QUANTUM computer can perform tasks far more efficiently than classical computers by using the quantum states of quantum bits (qubits). Superconducting qubits, which utilize macroscopic quantum effects in superconductors, are very promising candidates for practical qubit applications, because they are solid-state devices and can be easily integrated using conventional fabrication processes [1], [2].

To realize a quantum computer composed of a large number of qubits, high-speed manipulation and highly accurate detection of the qubit states is required. For superconducting qubits, a single flux quantum (SFQ) circuit [3] is attractive for that purpose, because of its excellent ability in terms of speed, power and sensitivity. Compatibility of the materials and operating temperature is also an advantage. To date, several methods for the manipulation and detection of the superconducting qubits states using SFQ circuits have been proposed and demonstrated [4]–[6]. These methods are useful for the scaling up of quantum computers, because the direct connection between qubits and room-temperature electronics can be reduced considerably, resulting in the decrease of thermal noise and heat flow from the room temperature environment.

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Even though the power consumption of SFQ circuits is very small compared with semiconductor circuits, it is still quite large for the qubit application to prevent thermal influence to the qubits and maintain a sufficiently low operating temperature. In this study, we have investigated a method to decrease the static power consumption of the SFQ circuits using a LR-loading technique.

II. LR-LOADING TECHNIQUE

Power consumption of SFQ circuits is divided into static and dynamic parts. Dynamic power consumption P_D arises from the switching event at the Josephson junction itself. The P_D at a junction is denoted as

$$P_D = \Phi_0 I_C f, \quad (1)$$

where Φ_0 is the quantum flux ($= h/2e$), and I_C and f are the critical current and switching frequency of the Josephson junction, respectively. Dynamic power consumption is essential for circuit operation and cannot be reduced without reducing the circuit performance. Typical parameter conditions used for the qubit application were as follows: $I_C = 10 \mu\text{A}$ and $f = 10 \text{ GHz}$, so that $P_D = 0.21 \text{ nW}$ can be obtained. Static power consumption P_S is caused by on-chip bias resistors, which supply a constant bias current to the circuit. The P_S at a bias circuit is given by

$$P_S = I_b V_b, \quad (2)$$

where I_b and V_b are the bias current and voltage of the bias circuit, respectively. If we assume $I_b \sim 0.7 I_C$ and $V_b \sim 7 I_C R_s \sim 2.50 \text{ mV}$, we obtain $P_S = 18 \text{ nW}$, where R_s is the shunt resistance of the junction. P_S is typically two orders of magnitude larger than P_D . Therefore, a reduction of the static power consumption of the SFQ circuits to the same level as the dynamic power consumption is a reasonable goal for the low-power SFQ circuit design.

Fig. 1 shows a schematic of an equivalent circuit of a Josephson transmission line (JTL) from our cell library [7] for operation at 4.2 K. The bias current I_b is supplied to the junction by an off-chip bias voltage V_b and an on-chip bias resistor R_b . The bias voltage V_b is 2.5 mV, which is selected as much larger than the amplitude of the voltage pulse at the junction, in order to supply a constant current I_b to the circuit. The simple reduction of the bias resistance reduces the static power consumption at the bias resistor. However, it results in the impulsive decrease of the bias current and causes deterioration of the circuit operation and the interaction between circuits.

Fig. 1. Schematic of an equivalent circuit for a JTL with a conventional bias circuit.

Fig. 2. Schematic of an equivalent circuit for a LR-loaded JTL. A large inductance L_b is inserted to the bias circuit.

For stable operation of low-power SFQ circuits, we have investigated the LR-loading technique [8]. Fig. 2 shows a circuit schematic of a LR-loaded JTL. In this circuit, a large inductance L_b is inserted in the bias circuit to prevent the impulsive decrease of the bias current. The bias current is determined by $I_b = V_b/R_b$, and the static power consumption is given by $P_s = R_b I_b^2$, which scales down with the decrease in R_b when I_b is constant.

In the LR-loaded SFQ circuits, the time constant of the bias circuit $\tau (= L_b/R_b)$ must satisfy the following relationship,

$$\Delta t \ll \tau \quad (3)$$

and

$$\tau \ll T, \quad (4)$$

where Δt is the SFQ pulse width, which has a typical value of 2 ps for a 2.5 kA/cm² Nb process, and T is the clock period. Equation (3) is the condition to avoid the impulsive decrease of the bias current during the switching event at the junction. Equation (4) ensures the average bias current for the circuit when the SFQ pulses propagate the junction at high frequency.

In addition, the bias inductance L_b must be much larger than the circuit inductance L , so that the SFQ pulses will not escape to the bias circuit,

$$L \ll L_b. \quad (5)$$

Fig. 3. Block diagram of the simulated circuit.

Fig. 4. The dependence of the propagation delay for a 100-stage LR-loaded JTL with various values of the bias resistance R_b . $I_{c1} = I_{c2} = 216 \mu\text{A}$, $I_b = 300 \mu\text{A}$, $L = 4.8 \text{ pH}$ in Fig. 2. The SRL 2.5 kA/cm² Nb standard process is assumed.

III. OPTIMIZATION OF CIRCUIT PARAMETERS

Equations (3) and (4) provides the parameter conditions for the time constant τ of the bias circuits, which is $2 \text{ ps} \ll \tau \ll 100 \text{ ps}$ for the $f = 10 \text{ GHz}$ and 2.5 kA/cm^2 Nb process. In this section we will investigate the dependence of the circuit operation properties on the time constant τ using circuit simulations. Fig. 3 shows a block diagram of a simulated circuit, which is composed of a 100-stage LR-loaded JTL. In the simulation, two SFQ pulses with 100 ps time intervals are input to the JTL array, and the propagation delay and the change of the time interval between two SFQ pulses have been calculated.

Fig. 4 shows the dependence of the propagation delay on the time constant τ for various values of R_b . Note that the R_b for the conventional JTL from our cell library is 8.35Ω . It can be seen that the propagation delay steeply increases when the time constant τ approaches the pulse width $\Delta t \sim 2 \text{ ps}$. This is because the impulsive decrease of the bias current deteriorates the circuit operation. It can also be seen that the increase in the propagation delay is larger for a smaller R_b , because the condition of (5) is not satisfied for a smaller R_b .

Fig. 5 shows the dependence of the time interval ΔT on the time constant τ for various value of R_b . The time interval between two SFQ pulses increases after the propagation through the LR-loaded JTL array when the time constant approaches the initial time interval $\Delta T_0 = 100 \text{ ps}$. This increase in the time interval is due to the reduction in the bias current for the second SFQ pulse. Because it takes time for the bias current to return to the initial condition after junction switching, the second SFQ

Fig. 5. The dependence of the time interval ΔT between two SFQ pulses on the time constant τ for the various value of R_b after propagating a 100-stage LR-biased JTL. The initial time interval is $\Delta T_0 = 100$ ps. The used circuit parameters are same to those of Fig. 4.

pulse has a smaller bias current when τ is large. These tendencies become remarkable when the bias resistance R_b is small.

It should be noted here that further reduction of the power consumption is possible by reducing the critical current of the junction. If the critical current I_C of each junction is reduced, the inductances L and L_b have to be increased to keep the LI_C product constant and from the (5). The bias resistor R_b also has to be increased to keep τ constant from the (3) and (4). As a result, the static power consumption $P_s = R_b I_b^2$ is decreased in proportion to I_C .

IV. DEMONSTRATION OF LR-LOADED SFQ CIRCUITS

We have designed several basic cells using the LR-loading technique. Fig. 6 shows a mask layout of the LR-loaded JTL cell. It should be noted that a low-power SFQ circuit is implemented only by modifying the bias circuit of existing cells from our cell library for 4.2 K operation. Therefore the critical current of the Josephson junction, which is approximately 200 μ A in the JTL, is not reduced in this study. According to the simulation results from the preceding section, all cells are designed so that the time constants of the bias circuits become 40 ps, when a 20% increase in the propagation delay is allowed at 10 GHz operation. Table I lists the simulated and measured DC bias margins for several basic cells, where the simulation results assume 10 GHz operation, whereas the experimental results were obtained using low-speed tests. It can be seen that all cells have DC bias margins larger than $\pm 20\%$, which is large enough for the circuit application.

To evaluate the stability of low-power SFQ circuits, the error rate of a low-power SFQ clock generator was measured. Fig. 7 shows a block diagram of the SFQ clock generator investigated. The system is composed of a ring-oscillator type clock generator with a SFQ pulse counter, which generates high-frequency 2^8 SFQ pulses [3], [10]. The frequency of the output SFQ pulse train is 14.6 GHz at the designed bias point. The clock generator contains 242 Josephson junctions and the power consumption is estimated to be 4.3 μ W. Note that the power consumption of the

Fig. 6. Mask layout for a LR-loaded JTL cell. The circuit is designed using the SRL 2.5 kA/cm² Nb standard process [9]. The time constant for the bias circuit ($\tau = L_b/R_b$) is designed to be 40 ps. $R_b = 0.6$ Ω , and L_b is 24 pH.

TABLE I
DC BIAS MARGINS OF BASIC CELLS USING THE LR-LOADING TECHNIQUE

Cell Name	DC Bias Margins at 10 GHz by simulations	DC Bias Margins by low-speed measurements
JTL	-30 to +45 %	-65 to +41 %
DFF	-27 to +45 %	-44 to +38 %
RTFF	-27 to +39 %	-26 to +25 %
NDRO	-10 to +27 %	-22 to +21 %

Fig. 7. Block diagram of a low-power clock generator with a pulse counter. RTFF denotes a resettable T flip-flop.

same clock generator using the conventional biasing technique is 61.1 μ W.

In order to measure the error rate of the clock generator, the number of output SFQ pulses was counted by another SFQ pulse counter designed using a conventional biasing technique. The 2^8 -pulse generation and error check were repeated many times and the bit error rate of the clock generator was estimated [10]. Fig. 8 shows the bit-error-rate of the low-power clock generator as a function of the bias current at 4.2 K. No error is observed at the optimum biasing point, which corresponds to a bit error rate less than 10^{-10} . The test result indicates that the low-power SFQ

Fig. 8. Bit-error-rate for a SFQ pulse generator with control circuits as a function of the DC bias current. Fitting curves are obtained using the error function [11]. The DC bias current is normalized by the design value.

circuit has stable operation, although the power consumption is reduced by 93% compared with that of ordinary biased circuits.

V. CONCLUSION

We have investigated and demonstrated low-power SFQ circuits using the LR-loading technique, which reduces the static power consumption of SFQ circuits. Simulation results indicate that the relation of time scales, that is, the pulse width, the operating frequency, and the time constant of the bias circuit, are very important for stable operation of the circuit. Based on the simulation results, we have implemented several basic cells using the LR-loading technique, and have experimentally shown their large DC bias margins. The power consumption of the cells is reduced by 93% compared with conventional SFQ cells. Further reduction of the power consumption is possible by reducing

the critical current of the junction for low-power operation. The bit-error-rate of the low-power clock generator was also measured, and was lower than 10^{-10} . This technique reduces the static power consumption of SFQ circuits to the same level as the dynamic power consumption and enabled the implementation of large-scale SFQ circuit system into a dilution refrigerator for control of superconducting quantum bits.

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