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Improvement of Time Resolution of the Double-Oscillator Time-to-Digital Converter using SFQ Circuits

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Abstract

We have designed, fabricated and tested a time-to-digital converter (TDC) using SFQ logic circuits. The proposed TDC consists of two sets of ring oscillators and binary counters, and a coincidence detector (CD), which detects the coincidence of the arrival of two SFQ pulses from two ring oscillators. The advantage of the proposed TDC is its simple circuit structure with wide measurement range in addition to the high resolution

and the high sensitivity of the SFQ TDC compared to semiconductor TDCs. The time resolution of the proposed TDC is limited by the resolution of the CD. In order to improve the resolution, we have developed a dynamic AND (DAND) gate, which can detect two simultaneous SFQ signal inputs with high accuracy. It was demonstrated that the time resolution of the TDC using the DAND gate is improved to be ± 4 ps.

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Keywords: SFQ circuits, superconducting devices, superconducting integrated circuits delay estimation, TDC, Josephson device measurement applications

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1. Introduction

Time is the most universal physical quantities. Almost all physical units like a position, a weight, a pressure and a temperature can be captured by a time measurement.

The time-to-digital converter (TDC) is a device, which measures the time delay and converts it directly to a digital binary code. TDC is used in many application fields including the TOF (time of flight) measurements [1], the RF synthesis [2] and the X-Ray imaging acquisition system [3]. Commercially available TDCs are made by CMOS circuits. The resolution of the state-of-the-art TDC is about 10 ps [4].

We have been developing the TDC using single-flux-quantum (SFQ) circuits [5]. The advantage of SFQ TDC is extremely high energy-sensitivity compared to the CMOS TDCs. It enables the elimination of the pre-amplification of small signals from sensors resulting in the improvement of the accuracy of time measurements. The other advantage is high time resolution due to the high-speed operation of the SFQ circuits. Moreover a wide-range time measurement with small circuit area is possible by using the proposed double-ring-oscillator architecture [5].

The time resolution of the proposed TDC is limited by the resolution of a coincidence detector (CD), which detects the coincidence of the arrival of two SFQ pulses from two ring oscillators. Previous study shows that the time resolution of the

SFQ TDC using an NDRO-based CD is about ± 10 ps.

In this study we have developed a dynamic AND (DAND) gate, which can detect two simultaneous SFQ signal inputs with high accuracy [6], in order to improve the time resolution of the SFQ TDC. We have experimentally evaluated the time resolution of the SFQ TDC system using the DAND gate by measuring the propagation delay of a Josephson transmission line (JTL).

2. Architecture of the TDC

The proposed TDC consists of two sets of NDRO-based ring oscillators [7] and T1-flip-flop-based binary counters [8], and a coincidence detector (CD). A block diagram and a timing chart of the TDC is shown in Fig. 1 and Fig. 2, respectively.

Oscillation periods T_1 and T_2 of the ring oscillator 1 (RO1) and the ring oscillator 2 (RO2) differ slightly. In operation, the RO1 starts its oscillation when a “Start” signal is applied as a trigger. After a delay time, the RO2 starts its oscillation at which a “Stop” signal is applied. The SFQ pulses generated by the RO1 and the RO2 are sent to the binary counter 1 and 2, respectively, and each counter counts the number of output SFQ pulses. At the same time, SFQ pulses from the ring oscillators are sent to the CD, which detects the coincidence of the arrival of two SFQ inputs. Because the oscillation period

of the RO1 and the RO2 is slightly different each other, the time difference of the SFQ pulses coming from two oscillator is varied by $\delta T = T_1 - T_2$ every oscillation cycle and finally it becomes almos zero. When the CD detects it, an “ROstop” signal is generated from CD, which stops the oscillation of the RO1 and the RO2. After that, “Trg” and “Read” signal is applied to the system to read out the values of each counter.

The measured delay time T_D can be calculated by

$$T_D = (N_1 - 1)T_1 - (N_2 - 1)T_2, \quad (1)$$

where N_1 and N_2 are the SFQ pulse number counted in the binary counters 1 and 2, respectively.

In this study, we have designed and implemented the TDC using the CONNECT cell library [9] and the SRL 2.5 kA/cm² Nb process [10].

Fig. 3 shows a schematic diagram and a timing chart of the DAND gate [6]. The DAND gate generates the output pulse “A&B” only if two input pulses “A” and “B” arrive at the gate within a time interval ΔT . Otherwise the internal state of the DAND is reset to the initial state. We have optimized the circuit parameter of the DAND gate using the MJSIM [11] and obtained the time resolution $\Delta T = \pm 2.2$ ps with the dc-bias margin ranging from -20% to 20% .

3. Timing jitter of the TDC

In the proposed TDC architecture, it is necessary to examine the timing jitter caused by the ring oscillators. It has to be less than the resolution of the DAND gate, otherwise the time resolution of the TDC is limited by the timing jitter of the ring oscillators. We have estimated the timing jitter of the ring oscillators as a function of the delay time that will be measured by the TDC. The result is shown in Fig. 4. According to the experimental results on the timing jitter of the JTL [12], we have calculated the timing jitter T_j of the ring oscillator using the following formula,

$$T_j = 0.1 \times \sqrt{m} \quad (ps), \quad (2)$$

where m is a number of Josephson junctions in the JTL along which the SFQ pulse propagates during the delay measurement. Because the total timing jitter T_{JT} of the TDC is the sum of the jitter of two ring oscillators, T_{JT} is given by

$$T_{JT} = \sqrt{(T_{j1})^2 + (T_{j2})^2}, \quad (3)$$

where T_{j1} and T_{j2} is the timing jitter of RO1 and RO2, respectively. If the delay time measured by the TDC is less than the oscillation period T_1 of RO1, the total timing jitter increases rapidly with the increase of the delay time because the two ring oscillators oscillate many cycle before the coincidence of the two pulses from the oscillator is detected. However, when the delay time reaches T_1 , the total timing jitter suddenly

decreases. The resultant delay-time dependence of the total timing jitter becomes saw-toothed shape as shown in Fig. 4. It can be seen from the figure that the total timing jitter caused by the ring oscillators is less than the time resolution of the DNAND gate when the delay time is less than 1 ns.

4. Experimental results

The time resolution of the DAND gate was evaluated experimentally at first. Fig. 5 shows a block diagram of the test circuit. In the test circuit, two input signals “A” and “B” are generated by splitting a common input signal “IN”. One of the two branches contains an additional JTL, whose delay can be varied by adjusting its bias current. As a result the time difference of the arrival time ΔT of the SFQ pulses at the node “A” and “B” can be controlled precisely. We have calculated the probability that the output signal “A&B” appears as a function of ΔT by repeating the measurement many times. The time difference of the arrival time ΔT caused by the JTL is evaluated from the simulation.

Fig. 6 shows the dependence of the output probability of the DAND gate on the time difference ΔT . One can see that the output probability gradually changes from 0 to 1 and vice versa. The width of the transition region is about 2 ps and is thought to be

due to the thermal noise. If we define the time resolution as a width of the 50% transition points, one obtains $\pm 2.5\text{ps}$ as the time resolution of the DAND gate. This nearly equals to designed value.

Next we have implemented the TDC using the DAND gate to investigate its time resolution. The total junction number and the area of the test system is 583 and $0.84\text{ mm} \times 1.34\text{ mm}$, respectively. The bias current dependence of the propagation delay of a 16-stage JTL was measured. The oscillation frequencies of the two ring oscillators were determined by measuring the average voltage of the ring oscillators.

Fig. 7 shows the bias current dependence of the delay of a 16-stage JTL measured by the TDC. Circuit simulation results are also shown in Fig. 6 for comparison. It can be seen from the figure that the test results agree well with the simulation results. The difference between the simulation and measurement results are estimated to be less than $\pm 4\text{ps}$.

5. Conclusion

In order to improve the resolution of the SFQ TDC, we have developed a DAND gate, which detects two simultaneous SFQ signal inputs with high accuracy. Tests results indicate that the highly accurate CD whose resolution is about $\pm 2.5\text{ps}$ is

obtained using the DAND gate. We have implemented the SFQ TDC system using the DAND gate and demonstrated the time resolution of about 4 ps.

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Figure Captions

Fig. 1. A block diagram of the proposed time-to-digital converter.

Fig. 2. A timing chart of the proposed time-to-digital converter.

Fig. 3. A schematic diagram and a timing chart of the DAND gate.

Fig. 4. The timing jitter of the ring oscillators as a function of the delay time.

Fig. 5. A block diagram of the test circuit for the DAND gate.

Fig. 6. The dependence of the output probability of the DAND gate on the time difference ΔT between two inputs signals.

Fig. 7. The bias current dependence of the propagation delay of a 16-stage JTL measured by the TDC and obtained by circuit simulations. A 100% bias current corresponds to the center of the bias condition.

Fig. 1

Fig. 2

Fig. 3

Fig. 4

Fig. 5

Fig. 6

Fig. 7