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Design and Implementation of Low-Power SFQ Circuits using LR-load Biasing Technique

T. Nishigai^{1,2}, S. Yamada^{1,2}, N. Yoshikawa^{1,2,*}

¹ Department of Electrical and Computer Engineering, Yokohama National University,
79-5 Tokiwadai, Hodogaya-ku, Yokohama 240-8501, Japan

² CREST-JST, Honcho 4-1-8, Kawaguchi, Saitama, 332-0012, Japan

Abstract

We have considered LR-load biasing technique to reduce power consumption of SFQ circuits for the application of control circuits of superconducting qubits. In this technique a current bias circuit is composed of a large inductance L_b , a small resistance R_b and a small voltage source V_b . In order to demonstrate the validity of this technique, we have designed a low-power 8-bit SFQ clock generator (CG), which produces 2^8 SFQ pulses at 14.6 GHz. By employing the LR-load biasing technique, the power consumption of the CG was reduced to about 10% of its original version, which is biased using large bias resistance. We have implemented a test circuit of the CG using NEC 2.5 kA/cm² Nb standard process and tested its operation and error rates. We have confirmed its correct operation with the dc bias margin of $\pm 14.8\%$ and obtained low enough error rates for the circuit application.

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Keywords: inductance load; superconducting qubit; superconductive circuit; SFQ circuits; power consumption

*Corresponding author.

Dr. Nobuyuki Yoshikawa

Postal address: Department of Electrical and Computer Engineering, Yokohama National University, Tokiwadai 79-5, Hodogaya-ku, Yokohama 240-8501, Japan

Phone: +81-45-339-4259

Fax: +81-44-338-1157

E-mail address: yoshi@yoshilab.dnj.ynu.ac.jp

1. Introduction

Single flux quantum (SFQ) logic circuits have great potentialities to realize future high-speed digital systems with low power consumption [1]. SFQ circuit technology is also very attractive for the quantum-computing application, because it has a possibility to perform accurate and high-speed control of a superconducting qubit [2]. If SFQ circuits are placed close to the qubit and operated at very low temperatures of several milli K, however, further reduction of the power consumption is required to keep it within the cooling limit of refrigerators and to decrease the thermal influence to the qubit.

At present, most SFQ circuits are usually driven by constant-current sources which consist of an off-chip voltage source and bias resistors integrated on the chip. The power dissipation in SFQ circuits is the sum of the dynamic dissipation P_D due to junction switching and the static dissipation P_S at bias resistors. In present typical SFQ circuits, P_S dominates the total power and thirty or forty times larger than P_D . Therefore, the reduction of P_S is essential for the further reduction of total power consumption of SFQ circuits. Several methods have been proposed to reduce or eliminate the power dissipation at the bias resistors, P_S [3][4].

One way to reduce the power consumption at the bias circuits is to use an LR-load biasing technique, where large bias resistance is replaced with large inductance and small resistance [5]. The advantage of this method is similarity and compatibility with the conventional circuit design. We can reuse a lot of existing design properties developed up to now in this method by simply modifying the circuit structure of their bias circuits. We believe that this method is useful not only for the qubit application but also for large-scale circuit applications where the low power consumption of the circuit is essential. In order to demonstrate the validity of this technique, we have designed and

implemented a low power 8-bit SFQ clock generator (CG). In this paper, we will describe its design and test results.

2. LR-load biasing technique

Figure 1(a) shows a conventional Josephson transmission line (JTL) which is biased by a constant-current source composed of a bias resistor R_{bias} and a voltage source V_{bias} . In order to ensure the correct operation and wide bias margins of the circuit, V_{bias} , and hence R_{bias} , must be sufficiently large compared with the amplitude of SFQ voltage pulses to keep the bias current constant and to reduce the interaction with other junctions during junction switching. This condition makes the static power at the bias current substantially large.

Figure 1(b) represents a JTL, which is biased by using an LR-load biasing technique [5]. In this technique, a constant-current source is composed of a large inductance L_b , a small resistor R_b and a small voltage source V_b , where R_b and V_b are much smaller than R_{bias} and V_{bias} , but supplies the same value of bias current $I_{\text{bias}} = V_b/R_b$ as conventionally biasing method as shown in Fig. 1(a).

In order to ensure the correct operation of the SFQ circuits using LR-load biasing, the following relationship have to be satisfied regarding the time constant of the bias circuits,

$$\tau \ll L_b/R_b < T, \quad (1)$$

where τ is the width of SFQ pulses and T is the clock period. The left condition is necessary to eliminate the interaction between junctions in the circuit during junction switching, and the right condition is needed to maintain enough value of the average bias current to the bias circuit.

3. Design of 8-bit SFQ CG

In order to demonstrate the validity of the LR-load biasing technique, we have designed a low-power 8-bit SFQ clock generator (CG) [6] [7]. In this design, we used LR-load-biasing cells, which are modified from the standard cells in the CONNECT cell library [8]. In our design the value of the voltage source V_b is reduced to about 10% of the conventionally biasing circuits. The time constant L_b/R_b at the bias circuit is set to be 40 ps assuming the pulse width $\tau \sim 2$ ps and the clock period $T \sim 60$ ps.

Figure 2(a) shows a block diagram of the CG. When a “Trigger” signal is applied to the CG, a non-destructive read-out (NDRO) cell is set to the “on” state. At the same time an SFQ pulse starts to go around the loop to generate high-speed SFQ clock pulses from “Output” until a “Stop” signal is output to reset the NDRO cell into the “off” state. The control circuit is composed of resettable T flip-flops (RTFF) and delay flip-flops (DFF), which sends a “Stop” signal after counting 2^8 SFQ pulses. The frequency of the CG can be varied by changing its bias current.

Figure 2(b) represents the simulation results of the CG using the LR-load biasing technique. We have confirmed the generation of 2^8 SFQ pulses from the CG by counting the SFQ pulses from the circuit by using eight stages of TFFs. It can be seen that just a “Stop” signal is generated from the control circuit, when a “check” signal, which corresponds to the generation of 2^8 SFQ clock pulses, is correctly generated. We have estimated by the circuit simulations the frequency and the power consumption of the CG to be 14.6 GHz and 4.3 μ W, respectively, at the designed bias current, and its bias margin to be $\pm 15\%$. The frequency and the power consumption of the conventionally biased CG were also estimated to be 16.6 GHz and 59.6 μ W, respectively, and its bias margin to be $\pm 21\%$. The difference of the bias margin and the operation speed

between the LR-load biased and the conventionally biased CGs are due to the slight reduction of the average bias current in the LR-load biased circuit. These results indicate that LR-load biasing technique enables us to reduce the power dissipation of SFQ circuits without large degradation of the bias margin and operation speed. In this study, we could reduce the power dissipation of the CG to about 7% of the original version.

4. Test results

We have designed and implemented the test circuit of the 8-bit SFQ CG with LR-load biasing using the CONNECT cell library and NEC 2.5 kA/cm² Nb standard process. The block diagram of the test circuit is shown in Fig. 3, which is composed of the 8-bit CG with LR-load biasing, an 8-bit binary counter (BC) using the TFFs with a non-destructive readout function [9], and a comparator using the conventionally biased cells in the CONNECT cell library. The test circuit contains 818 Josephson junctions, occupies the area of 1.50 mm x 1.24 mm, and dissipates 174.3 μ W (the CG dissipates 4.3 μ W). The frequency of the CG can be varied by changing its bias current, because its bias line is isolated from the other circuits.

The test of the CG is carried out at 4.2 K as follows. At first, a “Reset” signal is applied to the CG in order to reset its internal state, and a “Set” signal is applied to load initial data, “10000001”, to the BC. When a “Trigger” signal is applied to the CG, the CG generates 2⁸ high-speed pulses and sends them to the BC. The BC counts up 2⁸ pulses and go back to the initial state, “10000001”. Finally, “Read” signal is applied to the BC and the initial data and the data on BC are compared each other by the comparator to check the error. If an error occurs in the test circuit, an “Error” signal is

detected. In this case, if the probability of the error is much smaller than unity, we can assume that only one error have occurred in one test cycle. In order to simplify the design of the comparator, we used a fixed initial data, “10000001”, this time.

Measured output waveforms are shown in Fig. 4, when the bias current of the test circuit is in the optimal condition. We observed the SFQ output in “Out1” and “Out8”, which are the LSB and MSB of the output from the BC, respectively, and no “Error” signal. This indicates the correct operation of the CG. The bias margin of the CG was found to be $\pm 14.8\%$, which agrees well with simulation results.

We also measured the error rate of the CG with the bias current of the BC in the optimal condition. One sequence of the error test described above is repeated at the frequency of 19.2 kHz. The “Error” signal is detected by the frequency counter at room temperature through an SFQ/DC converter.

Figure 5 shows the clock frequency dependence of the error rate of the CG, where the clock frequency of the CG was estimated by the circuit simulation. It can be seen that the error rates of the CG are low enough for the circuit applications.

5. Discussions

A bit-error-rate (BER) of the CG can be calculated by dividing the error rate in Fig. 5 by 2^8 , because the CG generates 2^8 pulses in each sequence of the error test. The results are shown in Fig. 6. We also plot fitting curves for comparison in Fig. 6, which are the theoretical BER of a small circuit element given by

$$\text{BER} = \frac{1}{2} \text{erfc} \left[\sqrt{\frac{R}{8k_B T B}} |I_b - I_m| \right], \quad (2)$$

where R and I_b are the resistance and the bias current of the circuit element under

consideration, respectively, I_m is the value of bias current such that the error rate of the circuit is 50%, k_B is the Boltzman constant, T is an effective temperature and B is the bandwidth of the system [10]. It can be seen that the measured BER agrees well with the calculated results. In the CG, the NDRO cell is thought to limit the operation of the CG, because its bias margin is smaller than any other circuit element. In the parameter fitting, if we assume that $R = 0.08 \Omega$ and $I_b = 1.11 \text{ mA}$, which are the total resistance and bias current of the NDRO cell, and $B = 163 \text{ GHz}$, which is the plasma frequency of the Josephson junction, we can evaluate the effective temperature to be 4.4 K and 16.1 K for lower and upper edges of the bias margin, respectively. Right now we don't have a reasonable explanation of why the effective temperature of the upper edge of the bias margin is significantly larger than the operating temperature, 4.2K. The effective temperatures are varied in chip-to-chip and ranges from 4.4 K to 20 K in our circuits.

6. Conclusions

We have considered the LR-load biasing technique to reduce the power consumption of the SFQ circuits for the control circuit of a superconducting qubit, in which the bias current source is composed of a large inductance L_b , a small resistance R_b , and a small voltage source V_b . This technique enables us to reduce the power consumption of SFQ circuits easily without large degradation of the circuit bias margin compared with the conventionally biased circuit. In order to demonstrate the validity of this technique, we have designed a low-power 8-bit SFQ CG. The power dissipation of the CG was reduced to be about 7% of its conventionally biased version. We have also implemented the test circuit of the CG using NEC Nb standard process and tested its error rates. We have confirmed its correct operation and obtained low enough error rates for the circuit

application.

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Figure Captions

Fig. 1. An SFQ circuit using (a) a conventional biasing circuit and (b) an LR-load biasing technique.

Fig. 2. (a) A block diagram and (b) simulation results of 8-bit SFQ clock generator using LR-load biasing technique.

Fig. 3. A block diagram of the tested circuit.

Fig. 4. Measured output waveforms, “Out1”, “Out8” and “Error” when the bias current of the CG and the Counter are in the optimal condition. For the “Trigger”, “Set” and “Read” signals, rising edges correspond to the input of SFQ pulses. For the “Out1”, “Out8” and “Error” signals, transitions are the output of SFQ pulses.

Fig. 5. The clock frequency dependence of the error rate of the CG .

Fig. 6 The bias current dependence of the BER of the CG and fitting curves obtained from Eq. (2).

(a)

(b)

Fig. 1

(a)

(b)

Fig. 2

Fig. 3

Fig. 4

Fig. 5

Fig. 6