FDP-73 / ISS2007

Submitted 5 November 2007

Revised 26 December 2007

Novel Serial-Parallel Converter Using SFQ Logic Circuits

H. Park^{a,*}, Y. Yamanashi^a, K. Taketomi^a, N. Yoshikawa^b, A. Fujimaki^b, N. Takagi^c

^aDepartment of Electrical and Computer Engineering, Yokohama National University,

Tokiwadai 79-5, Hodogaya, Yokohama, 240-8501, Japan

^bDepartment of Quantum Engineering, Nagoya University,

Furo-cho, Chikusa, Nagoya, 464-8603, Japan

^cDepartment of Information Engineering, Nagoya University,

Furo-cho, Chikusa, Nagoya, 464-8603, Japan

Abstract

Ultra-fast operation with ultra-low power consumption and ballistic transmission of signals are attractive features of single-flux-quantum (SFQ) circuits for building large

scale digital systems. We have been designing SFQ circuits based on the bit-serial architecture, which can reduce the circuit area and timing error induced by clocking skew. In the bit-serial circuits, a serial-parallel converter, which is one of key circuits, is used for I/O interfaces, address decoders, multipliers and so on. In this paper, we propose a novel architecture for the SFQ serial-parallel converter whose latency is very small compared with conventional one. And, we have designed some SFQ circuits suitable for the proposed circuit. As an example, we have implemented and tested SFQ 4-bit multifunctional buffers using the SRL 2.5 kA/cm² niobium standard process. We have successfully confirmed all functions of the multifunctional buffer at low speed.

PACS codes: 85.25 Hv, 85.25 Na

Keywords: SFQ; serial-parallel converter; buffer; superconducting integrated circuits; Josephson logic

* Corresponding author.

Heejoung Park

Postal address: Yoshikawa Laboratory, Department of Electrical and Computer Engineering, Yokohama National University, Tokiwadai 79-5, Hodogaya, Yokohama,

240-8501, Japan.

Phone: +81-45-339-4269

Fax: +81-45-338-4269

E-mail address: park@yoshilab.dnj.ynu.ac.jp

1. Introduction

Ultra-fast operation with ultra-low power consumption and ballistic transmission of signals are notable features of single-flux-quantum (SFQ) circuits for building large-scale integrated circuits (LSIs) [1]. An SFQ circuit is thought to be a promising technology for future LSIs, because of these attractive characteristics. Recently, a lot of researches on SFQ digital circuits, such as SFQ cross-bar switches and SFQ microprocessors, have been carried out extensively [2,3]. However, it is difficult to build large-scale parallel circuits because a current integration level of SFQ circuits is so far very low. To overcome this problem, we have been designing SFQ circuits based on a bit-serial architecture, which can reduce the circuit area and timing error induced by clocking skew [4]. Though circuits designed by using the bit-serial architecture are inferior to the bit-parallel ones in terms of performances, we can make complex circuits on very small circuit areas with low power consumption. Moreover, we can realize high-performance circuits by utilizing the ultra high throughput of SFQ circuits. The performance of the whole system can be enhanced by using a lot of bit-serial small circuits.

This idea, a circuit design based the bit-serial architecture, is very useful for not only SFQ LSIs but also recent high-frequency Si LSIs. Some Si digital signal processors

(DSP) are designed based on bit-serial architecture [5].

We have started developing of an SFQ processor for high-end computing [6]. The heart of the proposed system is a very large-scale reconfigurable data path (LRDP) using SFQ circuits. Fig. 1 shows a block diagram of the LRDP. It is composed of a number of bit-serial SFQ floating-point units (FPU), which are connected each other by SFQ reconfigurable network switches. In this computation system, the memory bandwidth, which generally restricts the performance of the system, can be reduced because multiple calculations are performed in the LRDP with one memory access.

The bit-serial SFQ FPU, which is the main circuit block of the LRDP, is composed of several circuit components, such as a first-in-first-out buffers (FIFO) which synchronize timing of input data, a shifter which is required for floating-point calculation and a serial-parallel converter. Among these circuit components, the serial-parallel converter is very important because latency of serial-parallel conversion is relatively larger than that of the other circuits. Several types of SFQ serial-parallel converters have been proposed and demonstrated so far. However the circuit delay is proportional to the length of the input data, resulting in the deterioration of the latency of the system.

In this study, we propose a novel architecture for the serial-parallel converter, which

can drastically reduce the circuit delay compared with the conventional ones. We will show some practical circuits using the proposed serial-parallel converters, and estimate their performances. We will also implement a multi functional buffer using the proposed serial-parallel converter and demonstrated its correct operation.

2. Serial-parallel converter

Conventional serial-parallel conversion is performed using a shift register consists of D2 flip-flops (D2ffs) as shown in Fig. 2(a). It has two clock lines, one is for inputting the data to shift-register in serial, and the other is for outputting the data from shift-register in parallel. In other words, N-bit serial data are input and stored in the D2FF-based shift-register before the serial-parallel conversion. Internal data stored in the shift-register are output when the trigger signal is input. Fig. 2(b) shows the time chart of the conventional serial-parallel conversion. In this converter, at least N clocks must be supplied to perform the serial-parallel conversion.

In the conventional serial-parallel converter, all parallel data are output simultaneously synchronized by the trigger signal. And large latency is required to realize this function. However, in some circuits the most important point is not simultaneous output, but small latency. We propose a serial-parallel converter that

realizes smaller latency compared with conventional serial-parallel converters. Fig. 3(a) shows a block diagram of the novel serial-parallel converter. It is composed of a shift register (SR), which stores the “Control_Signal”, and an array of AND gates, which works like a switch. At first, the “Control_Signal” is stored in the first DFF of the SR, and the “Input_Data” is distributed to all AND gates. Then a clock signal (“Write_Clk”) is supplied to the SR, and one of the DFF of the SR outputs the “Control_Signal” to the AND gate. Among the AND gates, only one gate, to which the “Control_Signal” is input, turns on and the input data is output from the turned-on AND gate. At the same time, the “Control signal” is shifted to the next DFF synchronized by the clock signal. Fig. 3(b) shows the time chart of the proposed serial-parallel conversion. Latency of the proposed serial-parallel converter is very small because the datum, input to AND gates first, can be read out from the selected AND gate immediately.

3. Applications of proposed serial-parallel converter

In the proposed serial-parallel converter, latency of the serial-parallel conversion is very small, and converted data are output successively, while all data are output simultaneously in the conventional serial-parallel conversion. There are several applications suitable for using the proposed converter. We have designed some SFQ

circuit using the proposed serial-parallel converter, and estimated the performance of the circuits.

3.1 Multiplier

The serial-parallel multiplier is widely used in the field of SFQ LSIs [7]. In this algorithm, the multiplicand is input in a bit-parallel form, and the multiplier is input in a bit-serial form from LSB (the least significant bit) to MSB (the most significant bit). Fig. 4 shows a block diagram of the serial-parallel multiplier. This multiplier is composed of the conventional serial-parallel converter, AND gates and bit-serial adders (BSAs), where partial-products are calculated by the AND gates and a summation of the partial-products is calculated by the BSAs. The latency of the serial-parallel multiplier itself is small, however it takes time in the serial-parallel conversion of data A. N clocks is necessary for the serial-parallel conversion of N -bit data. Therefore, the total latency of the multiplication is proportional to the length of the digits of the multiplicand.

On the other hand, latency of the serial-serial multiplier, which uses the proposed serial-parallel converter, is proportional to the logarithm of the length of the digits [8]. Fig. 5 shows a block diagram of the serial-serial multiplier. It is composed of three blocks, that is, the proposed serial-parallel converter, shift registers and NDRO gates

generating the partial-products and a BSA tree calculating a summation of the partial-products. In this multiplier, the multiplication doesn't need to wait the serial-parallel conversion due to the immediate conversion of the serial-parallel converter. And, partial-products of same the digit are created at the same time. Consequently, the parallel addition of the partial-products is possible by arranging BSAs in a tree shape. The latency can be reduced to the logarithm of the length of the data.

Moreover, from the Fig. 4 and Fig. 5, one can see that there are few differences in the circuit component in these multipliers. The only differences are their formation.

3.2 Buffer

Recently high-speed and large-scale SFQ circuits have been realized. However, such circuits, which contain several thousand JJs and operate at tens of GHz, have a risk of data collisions in the data-path, because of high-frequency signal transmission and a lot of long interconnections. To avoid the data collision, SFQ buffers like FIFO buffers are inserted between each circuit component [9].

Conventional SFQ buffers can be fabricated in very small circuit areas, because they are made by modifying a DFF based shift register [10]. However, the latency required in serial-parallel conversion linearly increases with increase of the length of the buffer

stage, i.e. buffer size. This long latency results in the increase of the latency of the whole system. And its bias margin is narrow, because its circuit operation is complicated and its bias margin varies depending on the internal states of storage loops [10]. In the FIFO buffer, small latency is strongly desired for preventing the decline of the performance.

In this section, we introduce the novel buffer based on the proposed serial-parallel converter. Fig. 6 shows a block diagram of the buffer circuit. It is composed of three blocks, the proposed serial-parallel converter, array of resettable-DFFs (RDFF) storing the parallel data with a shift-register, and a tree of confluence buffers (CBs).

Storing the data in parallel brings about some merits. As indicated in the previous section, input data to the proposed serial-parallel converter can be read immediately. The latency of the FIFO buffer is, therefore, determined by the other circuit components like splitters and CBs. Because these circuits are arrayed in tree shape, the latency of the FIFO buffer is proportional to the logarithm of the length of the buffer stage. There are no interactions between the internal states of each bit. So we can obtain wide bias margin. Moreover, read and write operation can be performed simultaneously because the write clock and read clock are completely separated. By using the proposed buffer, we can obtain FIFO buffer with small latency.

3.3 Multifunctional buffer

Moreover the proposed buffer can be extended to a buffer which has a lot of functionalities including FIFO buffer, last-in first-out (LIFO) buffer and shift operations with simple circuit structures. Fig. 7 shows a block diagram of the multifunctional buffer. The function of LIFO can be obtained by adding a shift register that has the opposite propagate direction to the output control circuit. And, by inserting the CB between the DFFs of the shift register and the control circuit, we can shift the input data by arbitrary number of bits by inputting the control signals to an appropriate DFF in the SR. These functionalities can be integrated in a buffer at the same time.

4. Test results

We have implemented the 4-bit multifunctional buffer using the SRL 2.5 kA/cm² niobium standard process [11] and the CONNECT cell library [12]. The test circuit is composed of 709 JJs and the circuit size is 0.92 mm × 1.12 mm. Fig .8 shows the chip photograph of the 4-bit multifunctional buffer.

We have successfully confirmed all functions of the multifunctional buffer at low speed. Fig .9 shows the example of the measured waveform. One can see that the FIFO

operations, the shift operations and the LIFO operation. The DC bias margin was -15% ~ +28%.

5. Discussion

Though the proposed serial-parallel converter is useful for bit-serial circuits in terms of the latency, there are some disadvantages. The proposed buffer (70 JJs/bit) is very large compared with a shift register (10 JJs/bit). And the maximum operation frequency is limited by the propagation delay between DFFs. We simulated the dependence of the dc bias margin on the clock frequency. Fig. 10 shows a simulated result. As shown in the figure, lower margin is not sufficient for the stable operation at high operating frequency. We believe that it will be improved by developing the special cell with smaller numbers of junctions.

6. Conclusions

We proposed a novel architecture for the SFQ serial-parallel converter whose latency is very short. We introduced the examples of practical circuits using the proposed serial-parallel converters. As an example, the SFQ 4-bit multifunctional buffer, which is suitable for using the novel serial-parallel converter, was investigated. We have

designed, implemented and tested the multifunctional buffer, and successfully obtained its complete operation with a bias margin of $\pm 22\%$ at low speed.

Acknowledgments

This research was supported by CREST, Japan Science and Technology Agency.

The authors would like to thank all the CONNECT members consisting of SRL-ISTEC, NICT, Nagoya University and Yokohama National University.

References

- [1] K. K. Likharev, V. K. Semenov, IEEE Trans. Appl. Supercond. 1 (1991) 3.
- [2] M. Dorojevets, P. Bunyk, and D. Zinoviev, IEEE Trans. Appl. Supercond. 11 (2001) 326.
- [3] Y. Kameda, S. Yorozu, Y. Hashimoto, H. Terai, A. Fujimaki, N. Yoshikawa, IEEE Trans. Appl. Supercond. 15 (2005) 6.
- [4] A. Fujimaki, Y. Takai and N. Yoshikawa, IEICE Trans. Electron. E85-C (2002) 612.
- [5] M. Nakajima, H. Noda, K. Dosaka, K. Nakata, M. Higashida, O. Yamamoto, K. Mizumoto, H. Kondo, Y. Shimazu, K. Arimoto, K. Saitoh, T. Shimizu, ISSCC Digest Technical Papers (2006) 1616.

- [6] N. Takagi, K. Murakami, A. Fujimaki, N. Yoshikawa, K. Inoue, H. Honda, IEICE Technical Report SCE2006-36 106 37.
- [7] R. F. Lyon, IEEE Trans. Commun. (1976) 418.
- [8] H. Park, Y. Yamanashi, K. Taketomi, N. Yoshikawa, A. Fujimaki, N. Takagi, International Superconductive Electronics Conference, Washington, DC, USA, June 2007.
- [9] M. Tanaka, T. Kawamoto, Y. Yamanashi, Y. Kamiya, A. Akimoto, K. Fujiwara, A. Fujimaki¹, N. Yoshikawa, H. Terai, S. Yorozu, Supercond. Sci. Technol. 19 (2006) 344.
- [10] H. Hara, Y. Nobumori, N. Yoshikawa, A. Fujimaki, Y. Hashimoto, H. Terai, International Superconductive Electronics Conference, Washington, DC, USA, June 2007.
- [11] S. Nagasawa, Y. Hashimoto, H. Numata, S. Tahara, IEEE Trans. Appl. Supercond. 5 (1995) 2447.
- [12] S. Yorozu, Y. Kameda, H. Terai, A. Fujimaki, H. Yamada, S. Tahara, Physica C 378-381 (2002) 1471.

Figure Captions

Fig. 1 Block diagram of the reconfigurable data path (LRDP) using SFQ circuits.

Fig. 2 Conventional serial-parallel converter. (a) Block Diagram (b) Time chart

Fig. 3 Novel serial-parallel converter. (a) Block Diagram (b) Time chart

Fig. 4 Block diagram of the serial-parallel multiplier based on the conventional serial-parallel convertor.

Fig. 5 Block diagram of the serial-serial multiplier using the proposed serial-parallel converter

Fig. 6 Block diagram of the novel buffer circuit using the proposed serial-parallel converter

Fig. 7 Block diagram of the multifunctional buffer using the proposed serial-parallel converter

Fig. 8 Chip photograph of 4-bit multifunctional buffer. The buffer is made up of 709 JJs and the circuit size is $0.92\text{ mm} \times 1.12\text{ mm}$.

Fig. 9 Example of low speed test results of the 4-bit multifunctional buffer. Input data pattern is [1011] from LSB to MSB. All functions of the 4-bit multifunctional buffer are confirmed. In the former five sequences, we tested the FIFO and the shift functions. In

the latter four sequences, we tested the LIFO and the shift functions.

Fig. 10 Dependence of the dc bias margin of the proposed multifunctional buffer on the clock frequency obtained by circuit simulations. The operating frequency is limited by the propagation delay of signals between DFFs.

Fig. 1

(a)

(b)

Fig. 2

(a)

(b)

Fig. 3

Fig. 4

Fig. 5

Fig. 6

Fig. 7

Fig. 8

Fig. 9

Fig. 10