Component Development for a 16 Gb/s RSFQ-CMOS Interface System

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Abstract—We have been developing an RSFQ-CMOS interface system. The system consists of three modules: a 1 to 32 bit DDST demultiplexer which converts a 16 Gb/s SFQ data input into a 32-channel 500 Mb/s output, asynchronous stacked-SQUID amplifiers which amplify an SFQ data input into a 5 mV voltage level output, and 77 K CMOS amplifiers which amplify a 5 mV voltage level input into a 5 V output at 500 MHz. We have implemented the asynchronous stacked-SQUID amplifier and the 77 K CMOS amplifier using the HYPRES 1 kA/cm² Nb process and the ROHM 0.6 μ m CMOS process, respectively. It was demonstrated that the 24-stage asynchronous stacked-SQUID amplifier amplifies an SFQ data input into a 2.0 mV voltage level at 600 MHz. The 77K CMOS amplifier was shown to amplify a 5 mV voltage level input into 5 V at 500 MHz from the simulation, and a 175 mV voltage input into 3.5 V at 90 MHz from the experiment.

Index Terms—RSFQ, interface, SQUID amplifier, CMOS amplifier

I. INTRODUCTION

One of the key elements in the RSFQ digital electronics technology [1] is the interface circuit, which converts high-speed small-amplitude SFQ data into the low-speed high-voltage data processable by CMOS logic circuits. The Josephson-CMOS hybrid memory system [2] is a promising approach to overcome the lack of the high-density memory in the RSFQ logic circuit, where the RSFQ-CMOS interface system plays an important role.

Fig. 1 shows a 16 GHz RSFQ-CMOS interface system that we have been developing. The system consists of three modules: a 1 to 32-bit DDST demultiplexer, an asynchronous stacked-SQUID amplifier, and a 77 K CMOS amplifier. The demultiplexer converts 16 GHz serial data from the RSFQ circuits into 32-channel 500 MHz parallel data. The stacked-SQUID amplifier amplifies the SFQ input signal into the 5 mV dc voltage output, which can be detectable with the semiconductor amplifier at a low error rate. These modules operate at 4.2 K. The 77K CMOS amplifier amplifies the 5 mV voltage input into the 5 V CMOS logic level output at 500 MHz.

We have developed each sub-module separately before assembling them. In this paper we describe the details of the components and demonstrate their operation.

II. ASYNCHRONOUS DEMULTIPLEXER

We have developed a demultiplexer by using a data-driven self-timed (DDST) architecture [3]. In this asynchronous architecture, no global clock is used, but a localized clock is used within the DDST basic module. The constraint on the physical timing between the clocks and data was considerably reduced by the DDST architecture. Fig. 2 shows the block diagram of the 2-bit DDST demultiplexer. It consists of two D₂ flip-flops with complementary outputs and a T flip-flop. In operation, complementary input data are at first stored in both D₂ flip-flops. Then, the T flip-flop triggers the D₂ flip-flops alternately, resulting in alternating output of the complementary data. A larger demultiplexer system can be produced simply by connecting the 2-bit demultiplexer modules in a tree structure. We have implemented 4-bit and 8-bit demultiplexer system and reported the successful operation at low speed [3]. A high-speed test has been also performed using the DDST on-chip high-speed test system [4], and 18 Gb/s operation of the 2-bit system has been demonstrated [5]. In our interface system, we will use a 32-bit DDST demultiplexer.

Fig. 1. A 16 Gb/s RSFQ-CMOS interface system.

Fig. 2. A block diagram of a 2-bit DDST demultiplexer.

III. ASYNCHRONOUS STACKED-SQUID AMPLIFIER

So far, several types of superconducting voltage amplifiers have been investigated. One approach utilizes a series-parallel stack of under-damped Josephson junctions [6].

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Though its output voltage level and driving ability are high, it requires an rf power supply. Another approach uses a stack of over-damped DC SQUIDs [7]. Though the stacked-SQUID amplifier doesn't need an rf power supply, it is difficult to get a large enough output voltage due to its low current driving ability. Its maximum output voltage is limited to the order of mV range even if the number in the stack is increased. In order to overcome the voltage saturation effect, we will use a parallel array of the stacked-SQUID amplifiers, by which the effective impedance of the amplifier is decreased.

A schematic of the asynchronous stacked-SQUID amplifier is shown in Fig. 3. It is composed of m parallel connection of N stacked-SQUID cells. For high-speed operation we also consider an output load impedance Z_0 .

The dependence of the output voltage V_{out} and maximum operating frequency f_{max} of the amplifier on the series cell number N for various parallel cell number m are shown in Fig. 4a, where f_{max} is the frequency at which V_{out} decreases by one-half. In our design of the SQUID cells, the critical current is 125 μ A and the loop inductance is 8.0 pH. From Fig. 4a, one can observe the voltage saturation effect when $N > 12$ in case of $m = 1$, whereas it is improved for larger m . In order to find an optimum m value in the amplifier, we re-plotted the Fig. 4a. Fig. 4b shows the dependence of V_{out} on the total SQUID cell number $N \times m$. One can see that the optimum condition to get 3.5 mV amplitude is the combination of $N = 24$ and $m = 2$ for instance. On the other hand, the reduction of f_{max} for large N and m is due to the increase of the parasitic capacitance between the SQUID cell and the ground.

Fig. 3. Schematic of the asynchronous stacked-SQUID amplifier. Triangles denoted "J" are two-junction JTL stages.

The stacked-SQUID amplifier was implemented using the HYPRES 1 kA/cm² Nb process. The layout for $N = 24$ and $m = 2$ is shown in Fig. 5. Its dimension is approximately 3.6 x 1.4 mm. Fig. 6 shows test results of the amplifier with $N = 24$ and $m = 1$ when input frequency is 600 MHz. An output load impedance for the amplifier is $Z_0 = 50 \Omega$. Note that the amplifier includes an SFQ/DC converter of the T flip-flop

kind [1]. Therefore, the output frequency is divided by two. The output voltage amplitude of 2 mV from the measurement quantitatively agrees with the simulation results given in Fig. 4. We tested the output amplitude of the amplifier at higher frequency and had 1.6 mV at 1 GHz input frequency and 0.8 mV at 2 GHz. The reduction of the output voltage amplitude is thought to mainly arise from attenuation in the probe.

Fig. 4. (a) Simulated output voltage amplitude V_{out} and maximum operating frequency f_{max} of the asynchronous stacked-SQUID amplifier as a function of the series cell number N for various parallel cell number m . (b) Dependence of V_{out} on the total SQUID cell number $N \times m$.

Fig. 5. Layout of the 24-stage stacked-SQUID amplifier ($m = 2$).

Fig. 6. Test results of the 24-stage stacked-SQUID amplifier ($m = 1$) at 600 MHz.

IV. A CMOS HIGH SPEED AMPLIFIER

Fig. 7 shows the schematic of the CMOS amplifier operating at 77 K. The circuit structure is similar to that proposed by UC Berkeley [8], where we have modified the input part and have optimized the circuit parameters for 77 K operation. The circuit consists of pipelined multistage dynamic differential amplifiers, where the output signals are obtained after 1.5 clock period from the signal input.

Fig. 7. Schematic of the 77 K CMOS high-speed amplifier

A. A Principle of the Circuit Operation

The circuit consists of three blocks. First block (M3-M17) and second block (M18-M32) are composed of a high sensitivity differential amplifier made of a clocked flip-flop and a pair of dynamic latches. The third blocks are the

edge-triggered D flip-flops using TSPC latches to drive the output circuits.

The operation modes of each block corresponding to the clock phase Φ are summarized in Table I. At first, when the clock is low ($\Phi = 0$), M3 and M9 precharge the flip-flop up to V_{DD} . Then, when $\Phi = 1$, the input voltage is amplified by the first stage flip-flop. The output signal of the flip-flop is latched by the dynamic latches at the falling edge of the clock. In the next $\Phi = 0$ phase, the signal propagates to the second block and is amplified again, then latched by the dynamic latch at the raising edge of the clock. Finally, the output signal from the second block is evaluated by the TSPC latch at the next $\Phi = 1$ phase.

TABLE I OPERATION MODES OF EACH BLOCK IN THE CMOS HIGH SPEED AMPLIFIER.

Clock	Block1	Block2	Block3
High	Evaluation	Precharge	Evaluation
Low	Precharge	Evaluation	Precharge

B. Circuit Optimization and Simulation Results

We have extracted device model parameters for the 77 K CMOS by measuring the static and dynamic characteristics of the CMOS device at 77 K. We will use a ROHM 0.6 μm CMOS process for the implementation of the amplifier. All simulations and optimizations in this study are based on these 77 K CMOS devices model parameters.

The optimization of the circuit is mainly performed with the differential flip-flop in the first block, which has the largest influence on the sensitivity of the amplifier. For instance, the sizes of the NMOS (M4, M10, M11) and the PMOS (M3, M9) are optimized to increase the sensitivity.

Fig. 8 shows the simulation results of the amplifier at 77 K. As a consequence of the optimization, the sensitivity of the amplifier becomes 5 mV at 77 K for the input frequency of 500 MHz from the simulation. Note that the sensitivity at room temperature is 18 mV for the 500MHz operation.

Fig. 8. Simulated transient response of the 77K CMOS high-speed amplifier at 500 MHz.

C. Test Results

Fig. 9 shows a photograph of the amplifier, which is implemented using a ROHM 0.6 μm CMOS process. The circuit is a prototype, therefore it is not perfectly optimized like the circuit in Fig. 8. The entire size of the amplifier is 600 μm in height and 900 μm in width.

Fig. 9. Photograph of the 77K CMOS high-speed amplifier

Fig. 10 shows test results of the amplifier measured at 77K, where the clock frequency is 70MHz. Unfortunately, there is large amount of input noise which arises from the cross talk between the clock input and the signal input terminals on the test fixture. Therefore, input sensitivity is limited by the noise level at present. However, one can clearly see that 350 mV input signal is amplified up to 3.5 V at 70 MHz. We measured the sensitivity of the circuit at clock frequencies ranging from 5MHz to 100MHz at room temperature and at 77 K. The test results are listed in Table II. It is found from the table that the sensitivity of the amplifier increases at lower temperature at every frequency. We believe that the intrinsic sensitivity of the amplifier is much better than the test results because the sensitivity is limited by the input noise level by the cross talk at present.

Fig. 10. Test results of the 77K CMOS high-speed amplifier at 70MHz

TABLE II
SENSITIVITY OF THE CMOS HIGH-SPEED AMPLIFIER AT 77K AND AT 300K

Clock Frequency	Sensitivity at 300K	Sensitivity at 77K
100MHz	3.5V	350mV
90MHz	1.11V	175mV
60MHz	350mV	111mV
5MHz	55mV	11mV

V. CONCLUSION

We have developed the components for an RSFQ-CMOS interface system. It was demonstrated that a 24-stage asynchronous stacked-SQUID amplifier amplifies the SFQ output voltage into 2 mV at 600 MHz. 77K CMOS high speed amplifier amplifies the 5 mV input voltage into 5 V at 500 MHz from the simulation, and the 175 mV input voltage into 3.5 V at 90 MHz from the experiment.

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