Cell Based Design Methodology for BDD SFQ Logic Circuits: A High Speed Test and Feasibility for Large Scale Circuit Applications

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Abstract—We have proposed a cell-based design methodology for SFQ logic circuits based on a binary decision diagram (BDD) and implemented a BDD SFQ standard cell library using a Hypres Nb process. In this design methodology, any logic function can be implemented by connecting binary switches. Since the circuits are dual rail logic and don't need a global clock, difficulty in the timing design is reduced considerably. In our cell-based design approach, the cell library is composed of only five kinds of basic cells, whose circuit parameters are optimized so as to remove the inter-cell interaction. In the layout level, the cells have the identical size so that circuits can be implemented by simply embedding the basic cells. In this study we have performed an on-chip high-speed test of the BDD SFQ logic circuits. The test system consists of two four-bit data-driven self-timed (DDST) shift registers with a ladder type clock generator. We have confirmed 12 GHz operations of the BDD SFQ logic circuit. We have also examined circuit size dependence of the DC bias margin of large BDD SFQ circuits.

Index Terms—Binary decision diagram, cell base design, cell library, RSFQ, superconducting circuits.

I. INTRODUCTION

ONE of the important technologies for realization of large-scale SFQ integrated circuits [1] is design methodologies, as well as fabrication process technologies. Because of unique properties of the SFQ circuits compared with semiconductor digital circuits, the development of new design methodologies, which are suitable for the SFQ circuits and bring out their ultimate ability, is desirable [2].

We have proposed a cell-based design approach [3] based on a binary decision diagram (BDD) [4] and made a BDD SFQ standard cell library [5]. A top-down CAD environment [6] is also developed to assist the large-scale circuit design. In our design approach, logic functions are at first represented and synthesized by the BDD, which is a directed graph composed of binary switches. After the logic synthesis, the BDD is implemented by using the BDD SFQ basic cells. Any logic function can be implemented by simply placing the limited number of square-shaped basic cells.

In this paper, we have investigated a high-speed performance of the BDD SFQ basic cells by a data-driven self-timed (DDST) on-chip high-speed test system [6], [7]. We have made a test

Fig. 1. (a) A binary decision diagram, and (b) symbols of the basic cells in the BDD SFQ standard cell library.

system itself by using the BDD SFQ logic circuits. We have also examined the DC bias margin of the large BDD SFQ circuit to show the availability of this design approach to the large-scale circuit application.

II. BDD SFQ LOGIC CIRCUITS AND CELL LIBRARY

The BDD is a way to represent a logical function by a directed graph, which is composed of binary switches with one input and two outputs. Fig. 1(a) shows an example of the BDD which represents the logical function $x_1 x_2 + \overline{x_3}$. Each node has one input ("root") and two outputs ("branch0" and "branch1"), which switches the SFQ pulse entering to the "root" into one of two directions, "branch0" or "branch1." The boxes denoted by "0" and "1," correspond to the calculation results. Any logic function can be represented by the BDD, and logic synthesis algorithm is well established in the semiconductor circuit field [5].

We have proposed that the BDD is effectively implemented by using SFQ circuits replacing the binary switch with the D2 flip-flop [4]. The advantages of the BDD SFQ logic circuit are the limited number of primitive gates, the dual-rail and DDST operation, small gate number compared with the conventional SFQ logic style, and small latency due to the asynchronous operation.

We have developed a cell-based design approach for the BDD SFQ logic gate [3], and made a BDD SFQ cell library for the Hypres standard Nb process [8]. The BDD cells have also been added to the CONNECT cell library [9] for the NEC Nb standard process. Our BDD SFQ cell library is composed of five kinds of basic cells as shown in Fig. 1(b). The Bina cell has a

Manuscript received August 6, 2002. This work was supported by the Ministry of Education, Culture, Sports, Science and Technology under an SFQ project.

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Digital Object Identifier 10.1109/TASC.2003.813923

Fig. 2. A circuit schematic of a 4-bit DDST shift register using the BDD SFQ standard cell library.

function of the binary switch. Its internal state “1” or “0” is set by an input of an SFQ pulse into the complementary inputs “s1” or “s0,” respectively. Then, when an SFQ pulse is applied to the “root (r)” terminal, an SFQ is switched into one of two terminals, “branch1 (b1)” or “branch0 (b0),” depending on its internal state. In the circuit level, the parameters are optimized so as to remove the interaction between cells by reducing the inter-diffusion DC current between the cells. In the layout level, all cells have identical height and width, and positions of input/output terminals and supply lines are fixed.

III. ON-CHIP HIGH-SPEED TEST

A. DDST Shift Register

One important building block of the DDST on-chip high-speed test system is a DDST shift register, which stores and reads out the data at any speed determined by the input data frequency. In the DDST system, the timing information is carried by the data themselves [6]. When the data reach the DDST system, internal clock is recovered locally from the complementary input data by using logical OR function. The clock is then distributed within the block but is limited to a small region to control clock skew and racing.

Fig. 2 shows a circuit schematic of the 4-bit DDST shift register made of the BDD SFQ basic cells. The shift register is composed of four Bina cells. In the figure, the number of arrows in the Line cell indicates the number of 2-junction Josephson transmission line (JTL) stages, which is used to adjust the internal timing between the clock and data paths. When data enter to the shift register from the complementary inputs “In” and “In-bar,” internal clock is generated by the Joins cell, and provided to four Bina cells. This internal clock shifts every bit of the shift register forward by one bit before the datum reaches to the first Bina cell. At the same time a complementary output is generated by the fourth Bina cell and forwarded to outside of the register through the complementary outputs “Out” and “Out-bar.” Because of the dual rail nature of the Bina cell itself, the DDST shift register can be made by simply connecting the Bina cells in series.

The internal timing of the shift register was optimized for the input data rate of 10 GHz assuming a Nb Josephson process with the critical current density of 1 kA/cm². This target frequency was chosen to obtain a large DC bias margin larger than -30% ~ +30%. One important timing condition in the shift register is that in every Bina cell the clock signal has to be reached to the terminal “r” before the data signal enters to the terminals “s0” or “s1.” To satisfy this condition, the Line cells with three JTL stages are inserted between the Bina cells. The resultant DC

Fig. 3. The dependence of the operating range of the 4-bit DDST shift register for the global bias changes on operating frequency derived from circuit simulations.

In	1	0	0	1	0	0	0	0	0
In-bar	0	1	1	0	0	1	1	1	1
CG_In	0	0	0	0	1	0	0	0	0
Out	0	0	0	0	*	1	0	0	1
Out-bar	0	0	0	0	*	0	1	1	0

*: Output too fast

(b)

Fig. 4. (a) Block diagram of the DDST on-chip high-speed test system, and (b) an example of input and output data patterns.

bias margin is -32% ~ +36% for global bias changes. Fig. 3 shows the dependence of the operating range of the 4-bit DDST shift register for the global bias changes on operating frequency obtained by circuit simulations. One can see that lower margin gradually decreases with increase of the frequency, while the upper margin does not depend on the frequency. The decrease of the margin arises from discrepancy of the relative timing between the clock and the data at low bias voltage. The upper frequency limit is determined by the maximum operating frequency of the Bina cell itself.

B. DDST On-Chip High-Speed Test System

We have used the DDST on-chip high-speed test system developed previously to examine the high-speed operation of the BDD SFQ basic cells [7]. The block diagram of the DDST on-chip high-speed test system is shown in Fig. 4(a). The system is composed of two 4-bit DDST shift registers and a 4-bit 10 GHz clock generator. In the test, data “1001” are loaded into the input shift register at low speed at first, and initial values in the output shift register “0000” are shifted out on the output

Fig. 5. A layout of the DDST on-chip high-speed test system for the BDD SFQ cells. The circuit dimension is $1300 \mu\text{m} \times 2340 \mu\text{m}$.

Fig. 6. Low-speed test results of a series array of two 4-bit DDST shift registers. Each rising edge corresponds to an input of an SFQ pulse for “In” and “ $\bar{\text{In}}$,” and each transition corresponds to an output of an SFQ for “Out” and “ $\bar{\text{Out}}$.” The input data pattern is (1010 1011 1110 0000 1000 1001 0100 1101 0010). The output data pattern is shifted by eight bits from the input data pattern.

terminal. Then, a trigger signal “CG_In” is sent to the clock generator, which produces four bits of “0” to drive the loaded data “1001” out from the input shift register into the output shift register at high frequency. Simultaneously, high-speed output data “0000” are shifted out on the output terminal. Because this output signal is too fast, no output is observed by a low speed oscilloscope. Finally, when the read out data “0000” are applied at low frequency, data stored in the output register can be read out as “1001.” Resultant input and output signals are shown in Fig. 4(b).

C. Test Results

The on-chip high-speed test system was designed by using the BDD SFQ cell library and fabricated using the HYPRES standard Nb process with the critical current density of $1 \text{ KA}/\text{cm}^2$. The mask layout of the test system is shown in Fig. 5, whose dimension is $1300 \mu\text{m} \times 2340 \mu\text{m}$.

Fig. 6 shows test results of the on-chip high-speed test system without a trigger for the clock generator. Therefore it is just

Fig. 7. Test results of BDD SFQ cells at high frequency (12 GHz). Each rising edge corresponds to an input of an SFQ pulse for “In” and “ $\bar{\text{In}}$,” and each transition corresponds to an output of an SFQ for “Out” and “ $\bar{\text{Out}}$.” The input data pattern is (1001 0000) as described in Fig. 4(b). Correct operations are observed with output data patterns of (0000 1001) with the clock trigger signal “CG_In.”

similar to a series array of two 4-bit DDST shift registers. The input data pattern is (1010 1011 1110 0000 1000 1001 0100 1101 0010). One can see that correct operation is observed with the output data pattern shifted by eight bits from the input data pattern. The measured DC bias voltage margin is $\pm 6.9\%$ at low frequency.

Fig. 7 shows test results of the on-chip high-speed test system at high frequency (10 GHz), where a trigger signal for the clock generator is applied. The data pattern into the test system is (1001 0 0000) as described in Fig. 4(b). One can see that correct operations are observed with the output data pattern of (0000 1001). The measured DC bias voltage margin is $\pm 6.9\%$ at high frequency, which is the same as the DC bias margin at low frequency. The maximum operating frequency is estimated to be 12 GHz by the DC voltage for the clock generator, which is limited by the DC bias margin of the clock generator.

IV. FEASIBILITY FOR LARGE SCALE CIRCUIT APPLICATIONS

Because we have removed the interaction between cells by reducing the inter-diffusion DC current for every combination of the cell connections, theoretical DC bias margin doesn’t depend on the circuit sizes if the timing design is carried out perfectly and parameter variations due to the fabrication process are ignored. We have listed junction counts, and simulated and tested DC bias margins of the BDD SFQ basic cells and several BDD SFQ circuits in Table I. All circuits are fabricated by using the HYPRES standard Nb process with the critical current density of $1 \text{ kA}/\text{cm}^2$. It is found from the table that the experimental DC bias margin gradually decreases with increase of the circuit size, while the simulated DC bias margin is almost constant.

In order to examine the circuit size dependence of the DC bias margin of the BDD SFQ circuit, we have implemented a 28-bit DDST shift register having several taps for the signal input and output as shown in Fig. 8. We have measured six chips but unfortunately no circuit operates perfectly. The maximum circuit that

TABLE I
A LIST OF JUNCTION COUNTS, AND SIMULATED AND TESTED DC BIAS
MARGINS OF THE BDD SFQ BASIC CELLS AND CIRCUITS

Circuit	Junction Count	DC Bias Margin	
		Simulation	Tested@1kHz
Line	2	$\pm 63\%$	$\pm 60.0\%$
Fork	3	$\pm 39\%$	$\pm 49.3\%$
Join	8	$\pm 45\%$	$\pm 42.5\%$
Bina	27	$\pm 33\%$	$\pm 30.3\%$
Data Selector	87	$\pm 34\%$	$\pm 20.9\%$
Multiplexer	116	$\pm 32\%$	$\pm 15.1\%$
4b DDST SR	210	$\pm 34\%$	$\pm 15.9\%$
8b DDST SR	502	$\pm 34\%$	$\pm 15.4\%$
12b DDST SR	735	$\pm 34\%$	$\pm 4.8\%$
On-Chip high speed test system for 8b DDST SR	563	$\pm 34\%$	$\pm 6.9\%$ @12GHz
1b ALU	730	$\pm 33\%$	$\pm 3.3\%$

Fig. 8. A layout of 28-bit DDST shift register having several taps for the signal input and output.

operates correctly with the common bias voltage was a 12-bit DDST shift register at present, though other part of the circuits operates at different bias voltage conditions. The main reason why the whole circuit doesn't operate is that there is considerable offsets in the bias voltage within the same circuit due to the local distribution of the circuit parameters. Another reason is the effect of large bias current. The number of the DC power

source necessary for our shift register to operate is just one, but it has a several taps around the circuit. We observed the variation of the DC bias margin by changing the current supply points. This means that bias current distribution affects the circuit operations. The current flowing through the ground plane possibly influences the circuit operation.

V. CONCLUSIONS

We have developed the cell-based design methodology based on the binary decision diagram for the purpose of the realization of large-scale SFQ digital circuits. In this study we have investigated the high-speed performance of the BDD SFQ circuits and examined the feasibility of large-scale circuit applications. The on-chip high-speed test demonstrated the 12 GHz operation of the DDST shift register composed of the BDD SFQ logic circuit. The circuit size dependence of the DC bias margin indicated that the theoretical DC bias margin is almost constant with increase of the circuit size, whereas experimental DC bias margin is deteriorated to several percent when circuit size approaches one thousand Josephson junctions.

ACKNOWLEDGMENT

The authors would like to thank the CONNECT cell library developing team of Nagoya University, NEC Inc., and CRL for their fruitful discussions.

REFERENCES

- [1] K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: A new Josephson-junction technology for sub-terahertz-clock frequency digital systems," *IEEE Trans. Appl. Superconductivity*, vol. 1, pp. 1–28, March 1991.
- [2] K. Gaj, Q. P. Herr, V. Adler, A. Krasniewski, E. G. Friedman, and M. J. Feldman, "Tools for the computer-aided design of multigigahertz superconducting digital circuits," *IEEE Trans. Appl. Superconductivity*, vol. 9, pp. 18–38, March 1999.
- [3] N. Yoshikawa and J. Koshiyama, "A cell-based design approach for RSFQ circuits using binary decision diagram," *Superconductor Science and Technology*, vol. 12, pp. 918–920, 1999.
- [4] N. Yoshikawa, H. Tago, and K. Yoneyama, "A new design approach for RSFQ logic circuits based on the binary decision diagram," *IEEE Trans. Appl. Superconductivity*, vol. 9, pp. 3161–3164, June 1999.
- [5] N. Yoshikawa and J. Koshiyama, "Top-down RSFQ logic design based on a binary decision diagram," *IEEE Trans. Appl. Superconductivity*, vol. 11, pp. 1098–1101, March 2001.
- [6] Z. J. Deng, N. Yoshikawa, S. R. Whiteley, and T. Van Duzer, "Data-driven self-timed RSFQ digital integrated circuit and system," *IEEE Trans. on Applied Superconductivity*, vol. 7, pp. 3634–3637, June 1997.
- [7] Z. J. Deng, N. Yoshikawa, S. R. Whiteley, and T. Van Duzer, "Data-driven self-timed RSFQ high speed test system," *IEEE Trans. Appl. Superconductivity*, vol. 7, pp. 3830–3833, December 1997.
- [8] BDD SFQ Cell library. [Online]. Available: <http://www.yoshilab.dnj.ynu.ac.jp/download/download.html>.
- [9] S. Yorozu, Y. Kameda, H. Terai, A. Fujimaki, T. Yamada, and S. Tahara, "A single flux quantum standard logic cell library," *Physica C*, vol. 378–381, pp. 1471–1474, 2002.