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Design and Implementation of SFQ Programmable Clock Generators

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Abstract

We have designed and implemented an SFQ programmable clock generator (PCG), which can generate variable length of SFQ pulses according to its internal state. PCG is composed of an SFQ ring oscillator, a control circuit, which counts up the number of SFQ pulses and stops the operation of the ring oscillator, and a decoder, which defines the initial state of the control circuit. PCG can generate the variable number of SFQ pulses ranging $2 \sim 2^N$ bits, where N is the number of T flip-flop in the control circuit. The oscillation frequency of PCG is designed to be ranging from 6.2 GHz to 18.8 GHz. In this study, we have implemented PCG generating SFQ pulses ranging $2 \sim 2^4$ bit using a cell-based design methodology and confirmed its correct functionality.

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Keywords: SFQ; RSFQ circuits; Clock generator; Ring oscillator; Cell-based design

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1. Introduction

Single Flux Quantum (SFQ) circuits are a promising technology for the application to processors [1], [2], network switches [3], AD converters and so on [4]. Among them, the applications to measurement instruments is important, because they use the strong points of the SFQ circuits: high-speed operation, low noise and high-sensitivity. A high-speed programmable clock generator (PCG), which generates the variable number of SFQ pulses, is one of the key components in such application. In the high-speed clock generators (CG) of ladder type [5], however, the area increases in proportion to the number of its bit length. CG using a ring oscillator with a control circuit is effective for reduction of the area [4], whose area increases in proportion to $\log N$ with the increase of the bit length.

In this study, we have proposed PCG, which can generate the variable number of SFQ pulses according to the initial state of the control circuit, by adapting CG proposed by Likharev and Semenov [4]. We have also designed, implemented and tested PCG, which can generate SFQ pulses of $2 \sim 2^4$ bits using a cell-based design methodology [6], [7], and confirmed its correct operation successfully. The tested DC bias margin was $-1.4\% \sim +20.7\%$ corresponding to the oscillation frequency ranging $11.9 \text{ GHz} \sim 16.7 \text{ GHz}$.

2. Design of Programmable Clock Generator

Fig. 1 shows a block diagram of PCG, which is composed of an SFQ ring oscillator, a control circuit and a decoder. The ring oscillator generates high-speed clock pulses. The control circuit counts up the number of SFQ pulses and stops the operation of the ring oscillator. The decoder defines the initial state of the control circuit. The control circuit is composed of T flip-flops (Tff) and D flip-flops (Dff). PCG can generate the variable number of SFQ pulses ranging $2 \sim$

2^N bits, where N is the number of the Tff in the control circuit. The number of SFQ pulses can be controlled by changing the initial state of the Tffs and the Dffs of the control circuit.

2.1 SFQ ring oscillator

An SFQ ring oscillator is formed with a Josephson transmission lines (JTLs), a confluence buffer (cb) and splitters (spl). An SFQ pulse circulates within the ring, during which successive SFQ pulses are generated. Fig. 2 shows a block diagram of the ring oscillator. An NDRO (ND) register cell with a nondestructive read-out function is used to stop the operation of the ring oscillator. If once the “initialize” is enabled, an SFQ pulse arriving at the clk terminal generates an SFQ pulse at its dout terminal. If once the “stop” is enabled, its internal state is reset and an SFQ pulse arriving at the clk terminal does not generate the SFQ pulse. The control circuit counts up the number of pulses outputted from the ring oscillator, and sends a “stop” pulse to the ring oscillator.

2.2. Control circuit

Fig. 3 shows a block diagram of a control circuit. The control circuit is composed of N -stage T flip-flops (Tff) and $(N-1)$ -stage D flip-flops (Dff). Compared with the control circuit of CG proposed by Likharev and Semenov [4], SFQ input taps are added to each Tff and Dff to change their internal states. The n -th Tff generates an SFQ pulse at its b0 terminal when the 2^{n-1} -th SFQ pulse from the ring oscillator arrives at its din terminal. The n -th DFF produces an SFQ pulse to its dout terminal only after $(n+1)$ -th DFF produces an output SFQ pulse. Therefore, an output pulses from the n -th Dff is obtained when the $(2^{N-1} + 2^{N-2} + \dots + 2^{n-1})$ -th SFQ pulse from the ring oscillator arrives at its clk terminal. Thus, the first DFF generates an SFQ pulse when the

(2^N-1) -th SFQ pulse from the ring oscillator arrives at the controller. This output pulse stops the operation of the ring oscillator. Because one additional SFQ pulse is generated before the ring oscillator is turned off, the total pulse count from the ring oscillator becomes 2^N .

The total number of SFQ pulses from the ring oscillator can be varied by changing the initial state of each Tff and Dff by applying SFQ pulses to the taps. The taps for the Tffs and the Dffs are named “subtract” and “divide”, respectively. S_n and D_n represent the input of the SFQ pulse to the n -th subtract and divide taps, respectively. If D_n is enabled and the internal state of the n -th Dff is set to the one state, it generates an output pulse when its clk pulse arrives for the first time. Therefore the control circuit operates as one with n -stage Tffs and generates 2^n output SFQ pulses. If S_m is enabled and the internal state of the m -th Tff is set to the one state, it generates an output pulses to the b1 terminal at first when it gets the first input pulse, resulting in the decrease of the total pulse count of the ring oscillator by 2^{m-1} . An SFQ pulse can be applied to any subtract taps $S_1 \sim S_N$ at the same time, while an SFQ pulse is applied to only one of divide taps $D_1 \sim D_{N-1}$. In this case, the total number of output pulses from the ring oscillator is represented by

$$L = 2^n - \sum_{m=1}^n S_m 2^{m-1} . \quad (1)$$

Thus PCG can generate the variable number of SFQ pulses ranging $2 \sim 2^N$.

2.3. Decoder

The decoder generates input SFQ pulses for D_n and S_m of the control circuit according to its binary input. When the control circuit is composed of N -stage Tffs, the decoder needs N -bit input. Table. 1 shows the relation between the binary input for decoder and D_n and S_m . The decoder was designed by using NOT, AND and EXOR gates.

3. Test results

At the first, the characteristic of the ring oscillator itself was examined. The frequency of the ring oscillator was estimated by measuring the average voltage of the ring oscillator and using the formula, $V = f\Phi_0$, where f is a frequency of the ring oscillator and Φ_0 is a flux quantum. Fig. 4 shows the dependence of the frequency of the ring oscillator on its DC bias current. The tested results are plotted by open circles. The simulation results using a circuit simulator are also plotted in the figure. One can see that agreement between measured and simulated results is quite well. It should be noted here that we have measured the frequency of the ring oscillator without the control circuit in this measurement, therefore obtained dependence is different from that of the ring oscillator in PCG.

We have implemented PCG, which can generate the variable number of the output pulses ranging $2 \sim 2^4$ bit. A 4-bit binary counter is connected to the output of PCG to check the number of output SFQ pulses. A binary output (Out1~Out4) from the 4-bit counter are measured, while a binary input (In1~In4) are applied to the decoder. Fig. 5 shows a mask layout of PCG. The PCG is composed of 1925 Josephson junctions, and its circuit area is $2000 \mu\text{m} \times 1240 \mu\text{m}$. It is designed using CONNECT cell library [7], and fabricated using the NEC Nb $2.5\text{kA}/\text{cm}^2$ standard process [8]. Fig. 6 shows the test results of PCG, where the binary outputs from the output counter are shown when the binary inputs for the decoder are 2, 3, 9, 10, 11 and 9. One can see that the same binary outputs are obtained. A tested margin of the DC bias current was $-1.4\% \sim +20.7\%$, which corresponds to the frequency range of $11.9 \text{ GHz} \sim 16.7 \text{ GHz}$ of the ring oscillator from the simulation.

4. Conclusion

We have proposed an SFQ programmable clock generator (PCG), which can generate the variable number of SFQ pulses. We have implemented 4-bit version of PCG using a cell-based design methodology, and confirmed its correct functionality. The frequency of the ring oscillator agrees with simulation results quite well. Its DC bias margin is found to be $-1.4\% \sim +20.7\%$.

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Figure Captions

Fig. 1. A block diagram of an SFQ programmable clock generator.

Fig. 2. A block diagram of a ring oscillator.

Fig. 3. A block diagram of a control circuit.

Fig. 4. Measured and simulated frequencies of the ring oscillator as a function of its DC bias current.

Fig. 5. A mask layout of PCG.

Fig. 6. Test results of PCG. Binary outputs from the output counter are shown when binary inputs for PCG are 2, 3, 9, 10, 11 and 9. The scale of vertical axis is 200 $\mu\text{V}/\text{div}$. The scale of horizontal axis is 10.0 ms/div.