Design and Implementation of Double Oscillator Time-to-Digital Converter using SFQ
Logic Circuits

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Abstract

We have designed, fabricated and tested a time-to-digital converter (TDC) using SFQ logic circuits. The proposed TDC consists of two sets of ring oscillators and binary counters, and a coincidence detector (CD), which detects the coincidence of the arrival of two SFQ pulses from two ring oscillators. The advantage of the proposed TDC is its simple circuit structure with wide measurement range. The time resolution of the proposed TDC is limited by the resolution of the CD, which is about 10 ps because it is made by an NDRO cell in this study. The circuits are implemented using NEC 2.5 kA/cm² Nb standard process and the CONNECT cell library. We have demonstrated the measurement of the propagation delay of a Josephson transmission line by the TDC with the time resolution of about 10 ps.

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1. Introduction

Measuring the picosecond time lag is one of the important physical measurements. This scale of time lag cannot be measured by using ordinarily available instruments. Several time-to-digital converters (TDCs) based on the semiconductor electronics have been proposed up to date, which have picosecond time resolution. The commercially available GaAs-based TDCs have 10 ps resolution.

Single Flux Quantum (SFQ) logic circuits have the advantages in its potentially high-speed operation and low power consumption [1]. The TDC based on the SFQ technology has better performance than the semiconductor TDC in terms of power dissipation and sensitivity. It is expected that the advantage of the power consumption of the SFQ TDC increases significantly when the channel number of detectors increases. Moreover, the cooling costs, which are the common impediment in superconductor-based systems, can be easily eliminated because the detectors are usually cooled into the liquid helium temperature. Owing to these advantages, several types of TDC using SFQ logic circuits have been proposed in order to use in the field of high-energy and nuclear physics [2]-[4].

The measurement of the picosecond delay of SFQ circuits is difficult because of their high-speed operation and small signal amplitude. One solution to measure the delay is to use the on-chip SFQ TDC with picosecond time resolution. In this paper, we will propose a new type of TDC based on the SFQ logic circuits in order to measure the delay of SFQ circuits. We also present the measurement results of the bias current dependence of the propagation delay of a Josephson transmission line (JTL) using the proposed TDC.

2. Design and Operation of Time-to-Digital Converter

The proposed TDC consists of two sets of NDRO-based ring oscillators [5] and T1-based binary counters [6], and a coincidence detector (CD), which detects the coincidence of SFQ outputs from two ring oscillators. A block diagram of the TDC is shown in Fig. 1. Oscillation periods T_1 and T_2 of the ring oscillator 1 (RO1) and the ring oscillator 2 (RO2) differ slightly to satisfy a relationship

$$0 < T_1 - T_2 \leq \delta, \quad (1)$$

where δ represents time resolution of the CD. The number of bits of the binary counters is determined by the maximum time lag $T_{\max}$ in the measurement.

In operation, the RO1 starts its oscillation when a “Start” signal is applied as a trigger signal. After an interval of the time lag T , the RO2 starts its oscillation when a “Stop” signal is applied. The SFQ pulses generated by the RO1 and the RO2 are sent to the binary counter 1 and 2, respectively, and each counter counts the number of output SFQ pulses. At the same time, SFQ pulses from the ring oscillators are sent to the CD, which detects the coincidence of the arrival of two inputs. If the CD detects it, an “ROstop” signal is generated from the CD, which stops the oscillation of the RO1 and the RO2. After that, a “Trg” signal is applied to two binary counters, and the value of each counter is output to shift registers nearby. Finally, a “Read” signal is applied to read out the counted results in series. The time lag T' measured by the TDC can be calculated by

$$T' = (N_1 - 1)T_1 - (N_2 - 1)T_2, \quad (2)$$

where N_1 and N_2 are the counted results in the binary counter 1 and 2, respectively.

In this study, we have designed the TDC using the CONNECT cell library [7]. Figure 2 shows a simulation result of the TDC assuming the input time lag T is 200 ps. It can be seen that SFQ pulses are generated by the RO1 and the RO2 when “Start” and “Stop” signals are applied. Since the oscillation period of the RO2 is shorter than that of the RO1, the interval between two output pulses from the ring oscillators gets closer and

finally coincide each other. The CD detects the coincidence of these two pulses. One can see that the oscillation of the RO1 and the RO2 are stopped when the CD generates a “ROstop” signal for the ring oscillators. As shown in Fig. 2, one additional SFQ pulse is output from the ring oscillator after the output of the “ROstop” signal due to the delay in stopping the ring oscillators. This is why “1” is subtracted from N_1 and N_2 in Eq (1). In Fig. 2, the numbers of SFQ pulses generated from the RO1 and the RO2 are 11 and 10, respectively. The oscillation periods of the RO1 and the RO2 are designed to be 111 ps and 100.8 ps, respectively. Using Eq. (2), the time lag T can be calculated to be 202.8 ps. As will be mentioned later, this result is within the time resolution of the TDC, 10 ps in this design.

Figure 3 shows a block diagram of the CD. The CD is the important component of the TDC because it determines the time resolution. In this design, we have used an NDRO cell. In Fig. 3, an SFQ pulse from the RO1 is applied to “din” of the NDRO cell to set the internal state. At the same time the SFQ pulse is also provided to “reset” to reset the internal state of the NDRO cell after having a short delay by a delay element “D”. Then an SFQ pulse is applied to “clk” from the RO2 to provide a clock signal to the NDRO cell. In this case, no SFQ pulse is generated from “dout” when “reset” arrives earlier than “clk”, while an SFQ pulse is generated when “clk” arrives earlier than “reset”.

In the design of the CD, we have put 10 ps delay between “din” and “reset” to improve the stability of the operation of the CD. Therefore its time resolution is about 10 ps. It is expected that the CD using a dynamic AND gate [3] gives better time resolution. Because the difference in the propagation delays from two ring oscillators to the CD also affects the time resolution of the TDC, a symmetrical design is essential to obtain good time resolution. The advantage of the proposed TDC is its simple circuit

structure, while the wide range of the time lag can be measured with the time resolution δ . In addition, accurate measurement of the time lag is possible by measuring the oscillation period of the ring oscillator separately.

3. Test results

In order to demonstrate the accurate measurement of the propagation delay of the SFQ circuits by using the proposed TDC, we have designed and implemented a test circuit using NEC 2.5 kA/cm² Nb standard process and the CONNECT cell library. Figure 4 shows a block diagram of the test circuit, which can measure the bias current dependence of the propagation delay of a 38-stage JTL. In the figure “Start” and “Stop” signals are produced by branching a common input signal “IN”, where the “Stop” signal is delayed by the JTL. Because a bias current line of the JTL is isolated from that of the TDC, its propagation delay can be changed separately by adjusting its bias current. The oscillation frequencies of two ring oscillators in the TDC were estimated by the circuit simulation. A good agreement has been obtained between the measured and calculated frequencies in the ring oscillator [5]. The circuit contains 695 Josephson junctions, occupies an area of 0.90 mm x 1.06 mm, and dissipates the power of 209.7 μ W.

Measured output waveforms of “Countout1” and “Countout2” are shown in Fig. 5, when the bias current of the JTL is in the optimal condition. The output data for “Countout1” and “Countout2” are “00111” = “7” and “00110” = “6”, respectively, which correspond to the JTL delay of 155.2 ps. In the measurement, we sometimes observed the fluctuation in the LSB of the output data. This is thought to be due to the timing jitter arising from the ring oscillators.

Figure 6 shows the bias current dependence of the delay of the JTL measured by the

TDC. Circuit simulation results are also shown in Fig. 6 for comparison. It can be seen that the test results agree well with the simulation results, which indicates that the accuracy of the time lag measurement by the proposed TDC is quite good. The difference between the simulation and measurement results are within the range from 0.4 ps to 14.2 ps, which agrees well with the time resolution of the CD $\delta \sim 10$ ps.

4. Conclusion

We have designed the TDC using SFQ logic circuits. It consists of two sets of ring oscillators and binary counters, and the CD, which detects the coincidence of two inputs. The proposed TDC has simple circuit architecture and can measure the wide range of the time lag with good time resolution. The time resolution of the TDC is determined by that of the CD. Because the CD is designed based on the NDRO cell in this study, the time resolution was limited to about 10 ps. The farther improvement is, however, possible by using other type of CDs. We have also designed and implemented a test circuit to measure the bias current dependence of the propagation delay of the JTL using the proposed TDC. A good agreement was obtained between the simulation and the measurement results.

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Figure Captions

Fig. 1. A block diagram of the proposed time-to-digital converter.

Fig. 2. Simulation results of the TDC when the time lag T of the input signals is 200 ps.

Fig. 3. A block diagram and a timing chart of the coincidence detector. “D” represents a delay element.

Fig. 4. A block diagram of the test circuit.

Fig. 5. Measured output waveforms, “Countout1” and “Countout2” when the bias current of the JTL is in the optimal condition. For the output “Read”, rising edges correspond to the input of SFQ pulses. For the output “Countout1” and “Countout2”, transitions are the output of SFQ pulses. The output data for “Countout1” and “Countout2” are “00111” = “7” and “00110” = “6”, respectively.

Fig. 6. The bias current dependence of the propagation delay of a 38-stage JTL measured by the TDC and obtained by circuit simulations. 100 % of the bias current corresponds to the optimal bias condition, 150 μA for our JTL with $I_c = 216 \mu\text{A}$.

Fig. 1

Fig. 2

Fig. 3

Fig. 4

Fig. 5

Fig. 6